DESCRIPTION

The 526 is a high speed analog comparator intended for use in systems where low propagation delay and fast recovery from common mode or differential input overdrive is required. The device is specifically designed to provide a wide input common mode range while operating from power supplies commonly found in digital logic systems.

The 526 consists of a medium gain, high frequency differential amplifier and a high speed TTL gate fabricated within a single substrate by planar and epitaxial techniques. The output gate of the 526 has voltage and current capabilities compatible with DCL, DTL and TTL. The 526 output gate has a full fan-out of 10 to standard TTL loads.

The amplifier and gate may be used independently or cascaded for applications as a voltage comparator, digital line receiver or sense amplifier. The second gate input is used to provide strobe capability when operating the amplifier and gate in cascade.

FEATURES

- **PROPAGATION DELAY** — **30ns**
- **INPUT COMMON MODE RANGE** — **+4.5V, −3.5V**
- **DIFFERENTIAL OVERDRIVE RECOVERY** — **20ns**
- **OUTPUT COMPATIBLE WITH STANDARD LOGIC FORMS**
- **OPERATES FROM STANDARD ±5V SUPPLIES**

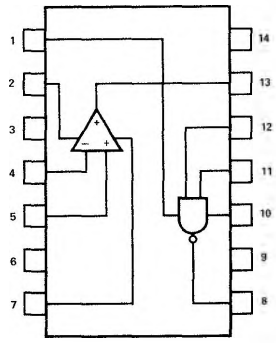
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		+7.0V
Gate Input Voltage		+6.0V
Differential Input Voltage		+5.0V
Common Mode Input Voltage		+5.0V
Gate Output Current		+100 mA
Storage Temperature		-65°C to +150°C
Operating Temperature	SE526	-55°C to +125°C
	NE526	0°C to +75°C

Absolute Maximum Ratings are limiting values above which serviceability may be impaired.

PIN CONFIGURATION

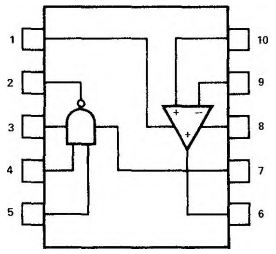
A PACKAGE



1. V_2^+
2. V_1^+
3. NC
4. V_{IN}
5. V_{IN}
6. NC
7. V^-
8. V_o
9. NC
10. Ground
11. V_{IN}
12. V_{IN}
13. e_o
14. NC

ORDER PART NOS.
SE526A/NE526A

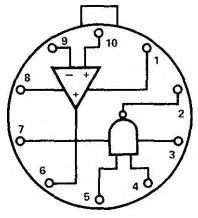
G PACKAGE



1. V_1^-
2. V_0
3. Ground
4. V_{IN}
5. V_{IN}
6. e_o
7. V_2^+
8. V_1^+
9. e_{in}
10. e_{in}

ORDER PART NOS.
SE526G/NE526G

K PACKAGE



1. V_1^-
2. V_0
3. Ground
4. V_{IN}
5. V_{IN}
6. e_o
7. V_2^+
8. V_1^+
9. e_{in}
10. e_{in}

ORDER PART NOS.
SE526K/NE526K

ELECTRICAL CHARACTERISTICS (Standard Conditions: $V_1^+ = V_2^+ = 5.0V$, $V^- = -5.0V$; Notes 1,2,3,4,13,14)

CHARACTERISTIC	SYMBOL	LIMITS				TEMPERATURE		NOTES
		MIN.	TYP.	MAX.	UNIT	SE526	NE526	
Input Offset Voltage	V_{io}		2.0	5.0	mV	−55°C	0°C	5
	V_{io}		2.0	5.0	mV	+25°C	+25°C	5
	V_{io}		2.0	5.0	mV	+125°C	+75°C	5
Input Bias Current	I_{in}		30.0	35.0	μA	−55°C	0°C	6
	I_{in}		25.0	35.0	μA	+25°C	+25°C	6
	I_{in}		22.0	35.0	μA	+125°C	+75°C	6
Input Offset Current	I_{io}		0.6	5.0	μA	−55°C	0°C	
	I_{io}		0.5	5.0	μA	+25°C	+25°C	
	I_{io}		0.4	5.0	μA	+125°C	+75°C	
Input Common Mode Range	V_{cm}	+4.2	+4.7		V	−55°C	0°C	
	V_{cm}	+4.2	+4.5		V	+25°C	+25°C	
	V_{cm}	+4.2	+4.4		V	+125°C	+75°C	
	V_{cm}	−3.2	−3.5		V	−55°C	0°C	
	V_{cm}	−3.2	−3.5		V	+25°C	+25°C	
	V_{cm}	−3.2	−3.5		V	+125°C	+75°C	
Amplifier Output Voltage	V_{ohi}	3.5			V	−55°C	0°C	
	V_{ohi}	3.5			V	+25°C	+25°C	
	V_{ohi}	3.5			V	+125°C	+75°C	
	V_{olo}			0.6	V	−55°C	0°C	
	V_{olo}			0.5	V	+25°C	+25°C	
	V_{olo}			0.4	V	+125°C	+75°C	
Amplifier Power Consumption	P_d		90	120	mV	−55°C	0°C	
	P_d		100	120	mV	+25°C	+25°C	
	P_d		110	120	mV	+125°C	+75°C	
Gate Output Voltage	$V1_o$	2.8	3.5		V	−55°C	0°C	7, 8
	$V1_o$	2.8	3.2		V	+25°C	+25°C	7, 8
	$V1_o$	2.8	3.0		V	+125°C	+75°C	7, 8
	$V0_o$		0.3	0.4	V	−55°C	0°C	7, 8
	$V0_o$		0.2	0.4	V	+25°C	+25°C	7, 8
	$V0_o$		0.3	0.4	V	+125°C	+75°C	7, 8
Gate Output Sink Current	$I0_o$	16.0			mA	+25°C	+25°C	8
Gate Output Source Current	$I1_o$	1.0			mA	+25°C	+25°C	7
Gate Input Threshold Voltage	$V1_i$	2.0			V	−55°C	0°C	9
	$V1_i$	2.0			V	+25°C	+25°C	9
	$V1_i$	2.0			V	+125°C	+75°C	9
	$V0_i$			1.0	V	−55°C	0°C	10
	$V0_i$			0.9	V	+25°C	+25°C	10
	$V0_i$			0.8	V	+125°C	+75°C	10
Gate Input Current (Input "0")	$I0_i$	−0.1	−1.2	−1.6	mA	−55°C	0°C	
	$I0_i$	−0.1	−1.4	−1.6	mA	+25°C	+25°C	
	$I0_i$	−0.1	−1.2	−1.6	mA	+125°C	+75°C	
(Input "1")	$I1_i$		5	25	μA	−55°C	0°C	
	$I1_i$		10	25	μA	+25°C	+25°C	
	$I1_i$		15	25	μA	+125°C	+75°C	
Gate Current Consumption (Output "1")	I_{CC}^1			2.00	mA	−55°C	0°C	
	I_{CC}^1			2.00	mA	+25°C	+25°C	
	I_{CC}^1			2.00	mA	+125°C	+75°C	
(Output "0")	I_{CC}^0			5.00	mA	−55°C	0°C	
	I_{CC}^0			5.00	mA	+25°C	+25°C	
	I_{CC}^0			5.00	mA	+125°C	+75°C	
Gate Input Latch Voltage Rating	BV_i			6.0	V	+25°C	+25°C	
Gate Output Short Circuit Current	I_{so}	−10.0		−70.0	mA	+25°C	+25°C	
Switching Times								
Gate Turn-On Delay	T_{on}		15	17	ns	+25°C	+25°C	11
Gate Turn-Off Delay	T_{off}		15	17	ns	+25°C	+25°C	11
Propagation Delay	$T_{pd}0$		30	42	ns	+25°C	+25°C	11
Propagation Delay	$T_{pd}1$		40	48	ns	+25°C	+25°C	11
Differential Overload Recovery	t_{dm}		30	40	ns	+25°C	+25°C	11, 12

Recommended Operating Supply Voltages ($V_1^+ = V_2^+ = 5.0V$, $V^- = -5.0V$

NOTES:

1. All measurements are referenced to the ground terminal.
2. Positive current is defined as into the pin referenced.
3. Pins not specifically referenced are left electrically open.
4. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
5. Input Offset Voltage is tested at guaranteed Input Common Mode Range voltage limits and includes the worst-case variations of voltage gain and input impedance. These are the maximum values required to drive the output down to "0" or up to "1".
6. Input Bias Current is defined as the maximum current required to bias either input.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_2^+.
9. These limits are guaranteed by Gate Output Voltage ($V0_O$) test.
10. These limits are guaranteed by Gate Output Voltage ($V1_O$) tests.
11. Load capacitance includes test fixture and probe capacitance.
12. Differential Input Voltage = 500mV for this test.
13. Acceptance Test Subgroup A-7 provides end point parameters for linear devices processed to Signetics SURE Program. See Signetics SURE Bulletin 5001.
14. Manufacturer reserves the right to make design and process changes and improvements.