2048 x 4 Diagnostic Registered PROM

53DA841
63DA841

with Asynchronous Enable and Output Initialization

Patent Pend.

Features/Benefits

- **Asynchronous output enable**
- **Programmable asynchronous output initialization**
- **Provides system diagnostic testing with system controllability and observability**
- **Shadow register eliminates shifting hazards**
- **Edge-triggered "D" registers simplifies system timing**
- **Cascadable for wide control words used in microprogramming**
- **24-pin SKINNYDIP® saves space**
- **Ti-W fusible link technology guarantees greater than 98% programming yield**
- **24 mA output drive capability**
- **Replaces embedded diagnostic code**

Applications

- **Microprogram control store with built-in system diagnostic testing**
- **Serial character generator**
- **Serial code converter**
- **Parallel in/serial out memory**
- **Cost-effective board testing**

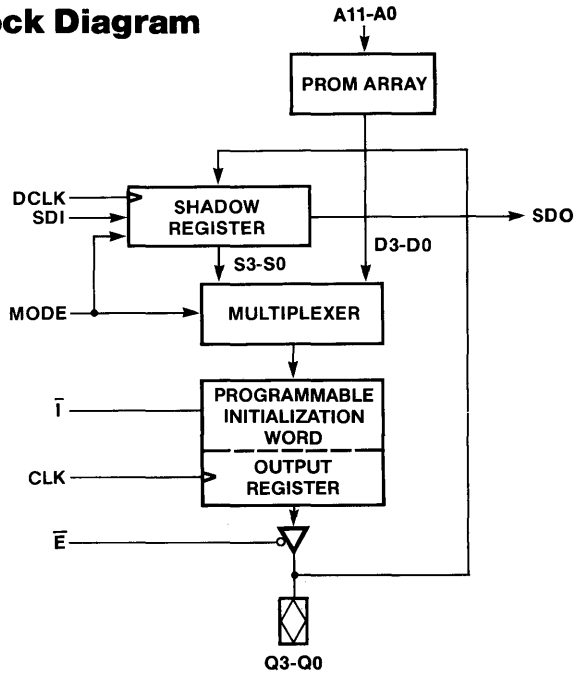
Description

The 53/63DA841 is a 2Kx4 PROM with registered three-state outputs, programmable asynchronous initialization and a shadow register for diagnostic capabilities. Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming. When exercised, the Initialization input loads the register with a user-programmable initialization word, independent of the state of CLK. This feature is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt.

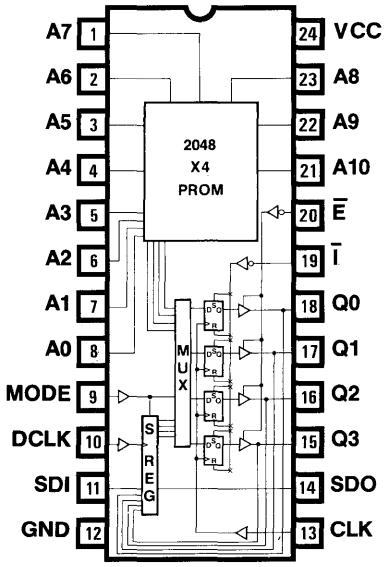
Ordering Information

MEMORY		TEMP.	PACKAGE		PART NO.
SIZE	ORG.		PINS	TYPE	
8 K	2048 x 4	Com	24	NS, JS	63DA841
		Mil	(28)	(NL),(L)	53DA841

Block Diagram



Logic Symbol



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Monolithic Memories

Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation †

* Clock must be steady or falling.

† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Definition of Signals

MODE — The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output register. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI — The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO — The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK — The clock pin loads the output register on the rising edge of CLK.

DCLK — The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 — Qn represents the data outputs of the output register. During a shadow register load these pins are the internal data inputs to the shadow register.

S3-S0 — Sn represents the internal shadow register outputs.

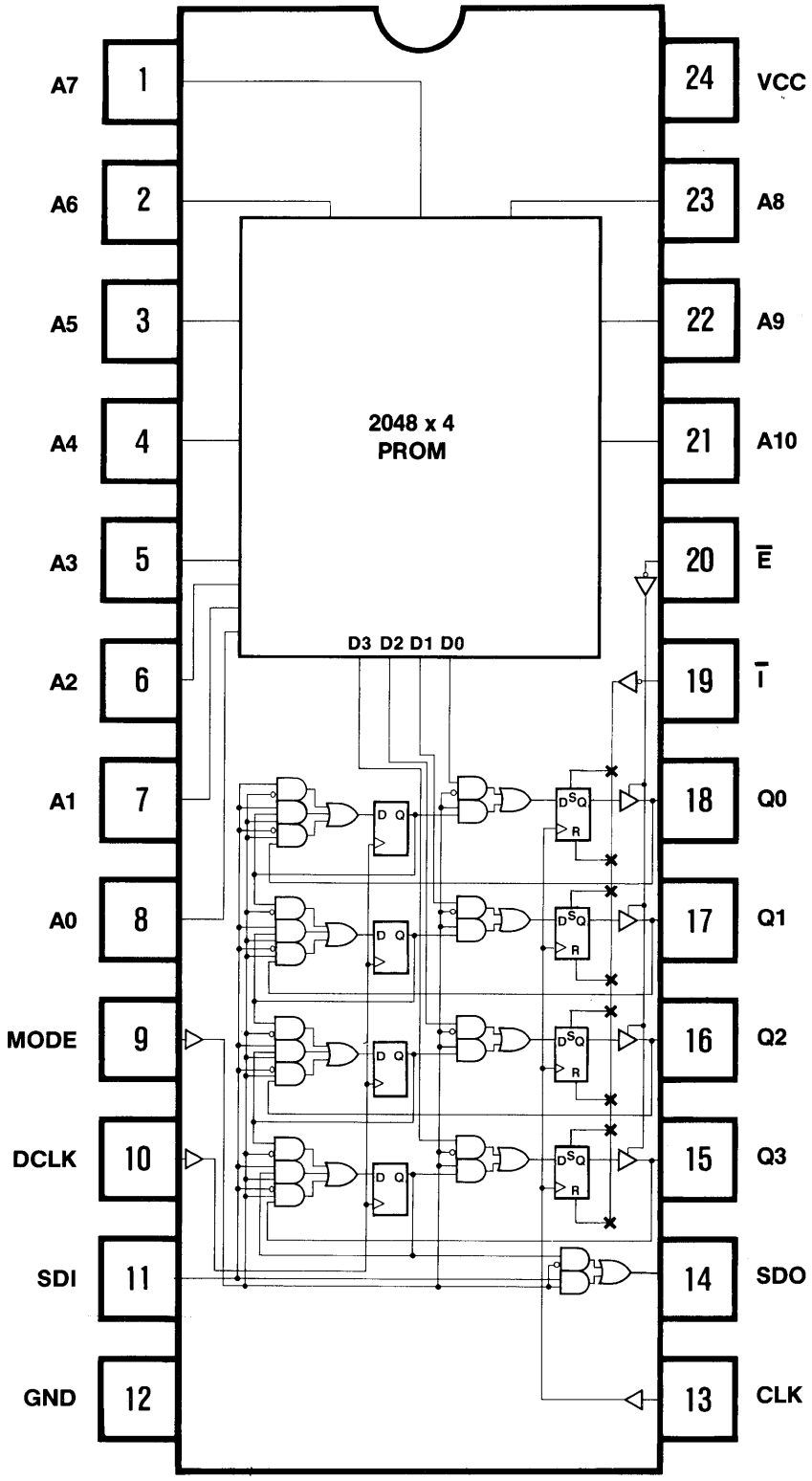
A10-A0 — An represents the address inputs to the PROM array.

$\overline{E}$ — The Output Enable pin operates independent of CLK. When $\overline{E}$ is LOW the outputs are enabled. When $\overline{E}$ is HIGH, the outputs are in the high-impedance state.

$\overline{I}$ — The asynchronous output register initialization input pin operates independent of CLK. When $\overline{I}$ is LOW, the output register is loaded with a user-programmable initialization word. Programmable initialization is a super-set of preset and clear functions, and can be used to generate any microinstruction for system reset or interrupt.

Logic Diagram

2048 x 4 Diagnostic PROM with Asynchronous Enable and Output Initialization



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150° C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Set up time from address to CLK	45	27		40	27		ns
t_h	Hold time for CLK	0	-15		0	-15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	45	15		40	15		ns
t_{sud}	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20		45	20		ns
t_{hd}	Hold time for DCLK	0	-5		0	-5		ns
t_{iw}	Initialization pulse width (LOW)	25	10		20	10		ns
t_{ir}	Initialization recovery time	45	30		40	30		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil I_{OL} = 16 mA Com I_{OL} = 24 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil I_{OH} = -2 mA Com I_{OH} = -3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-100	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V	-20		-90	mA
I_{CC}	Supply Current	V_{CC} = MAX. All outputs open.			140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

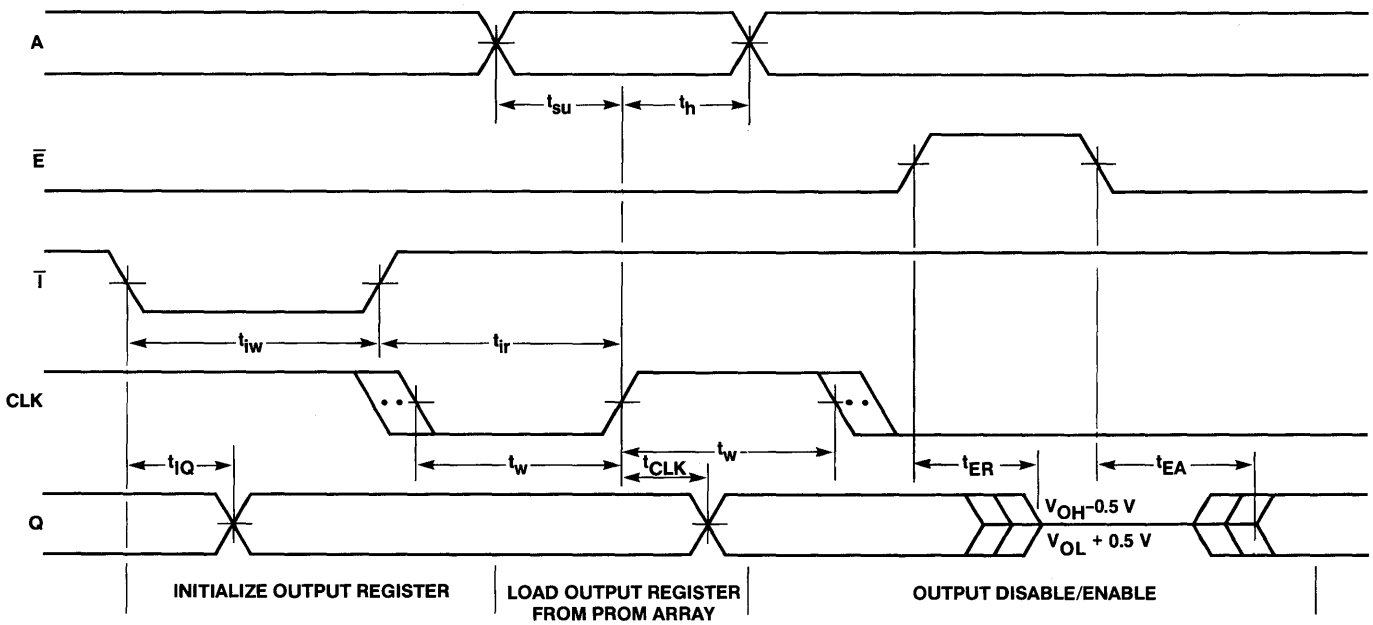
† Typical at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

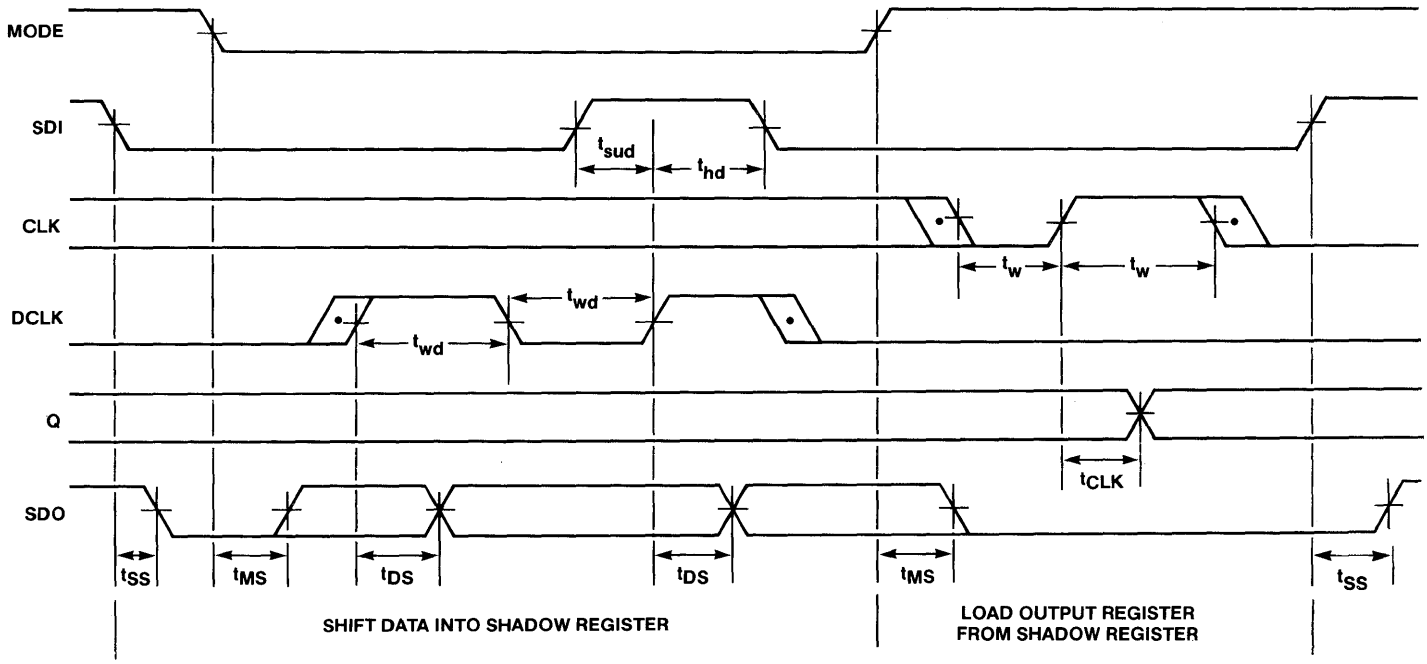
SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		13	25		13	20	ns
t_{ER}	Enable time		16	30		16	25	ns
t_{EA}	Disable time		16	30		16	25	ns
t_{IQ}	Initialization to output delay		23	40		23	35	ns
f_{MAXD}	Maximum diagnostic clock frequency	7	18		10	18		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		19	35		19	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns

† Typical at 5.0 V V_{CC} and 25°C T_A.

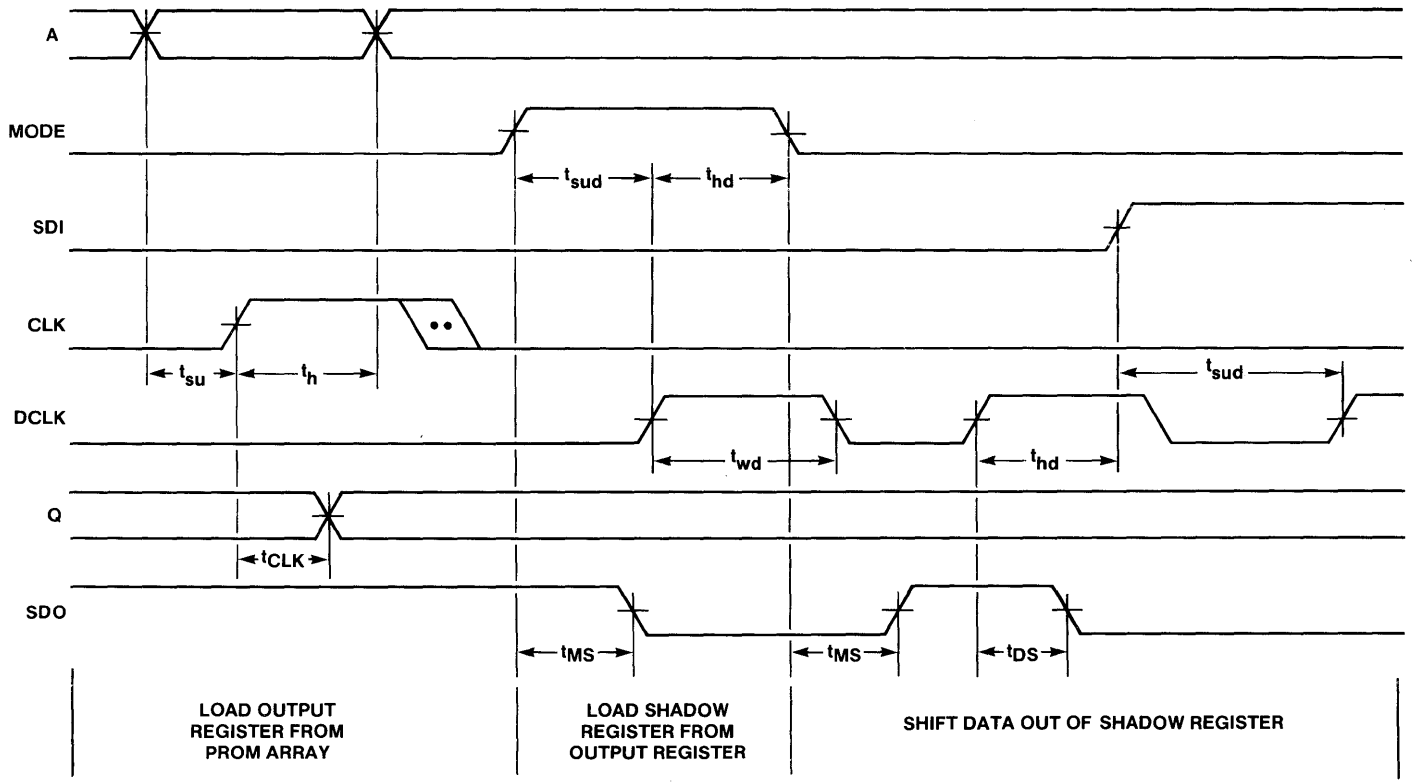
Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)

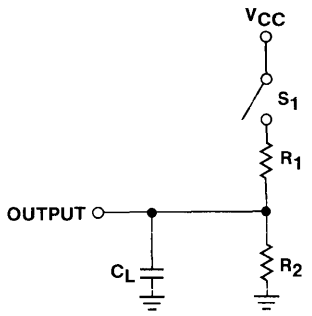


SYSTEM CONTROL



SYSTEM OBSERVATION

Switching Test Load



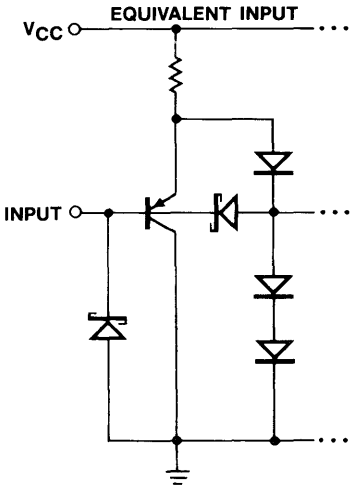
Definition of Timing Diagram

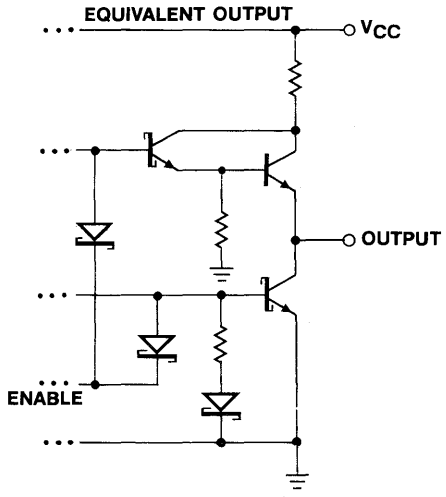
WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE	NOT APPLICABLE

NOTES:

1. For commercial operating range $R_1 = 200\Omega$ $R_2 = 390\Omega$.
   For military operating range $R_1 = 300\Omega$ $R_2 = 600\Omega$.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
4. Input access measured at the 1.5 V level.
5. Data delay is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
6. t_{EA} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test.
   t_{ER} is measured C_L = 5pF. S_1 is open for "1" to high-impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} +0.5 V output level.

Schematic of Inputs and Outputs





53/63DA841
Programming Instructions

Device Description

All of the High Performance Generic Ti-W PROM Families are manufactured with all outputs LOW in all PROM array storage locations. To product a HIGH at a particular word, a Titanium-Tungsten Fusible-Link must be changed from a low resistance to a high resistance. This procedure is called programming.

The output register initialization word is manufactured with all outputs HIGH and must be programmed to produce a LOW at a particular output.

Programming Description

To program a particular bit normal TTL levels are applied to all inputs. Programming occurs when:

1. V_{CC} is raised to an elevated level.
2. The output to be programmed is raised to an elevated level.
3. $\overline{I}$ is lowered to V_{IL}.

In order to avoid misprogramming the PROM only one output at a time is to be programmed. Outputs not being programmed should be connected to V_{CC} via 5KΩ resistors.

Unless specified, inputs to V_{IL}.

Programming Sequence

The sequence of programming conditions is critical and must occur in the following order:

1. Select the appropriate address with SDI = HIGH for array programming, or set SDI = LOW for initialize programming.
2. Increase V_{CC} to programming voltage
3. Increase appropriate output voltage to programming voltage
4. Lower $\overline{I}$ to V_{IL} for programming pulse width
5. Decrease V_{OUT} and V_{CC} to normal levels

Programming Timing

In order to insure the proper sequence, a delay of 100ns or greater must be allowed between steps. The enabling pulse must not occur less than 100ns after the output voltage reaches programming level. The rise time of the voltage on V_{CC} and the output must be between 1 and 10 V/μs.

Verification

After each programming pulse, verification of the programmed bit should be made with both low and high V_{CC} and the outputs enabled. The loading of the output is not critical and any loading within the DC specifications of the part is satisfactory.

Additional Pulses

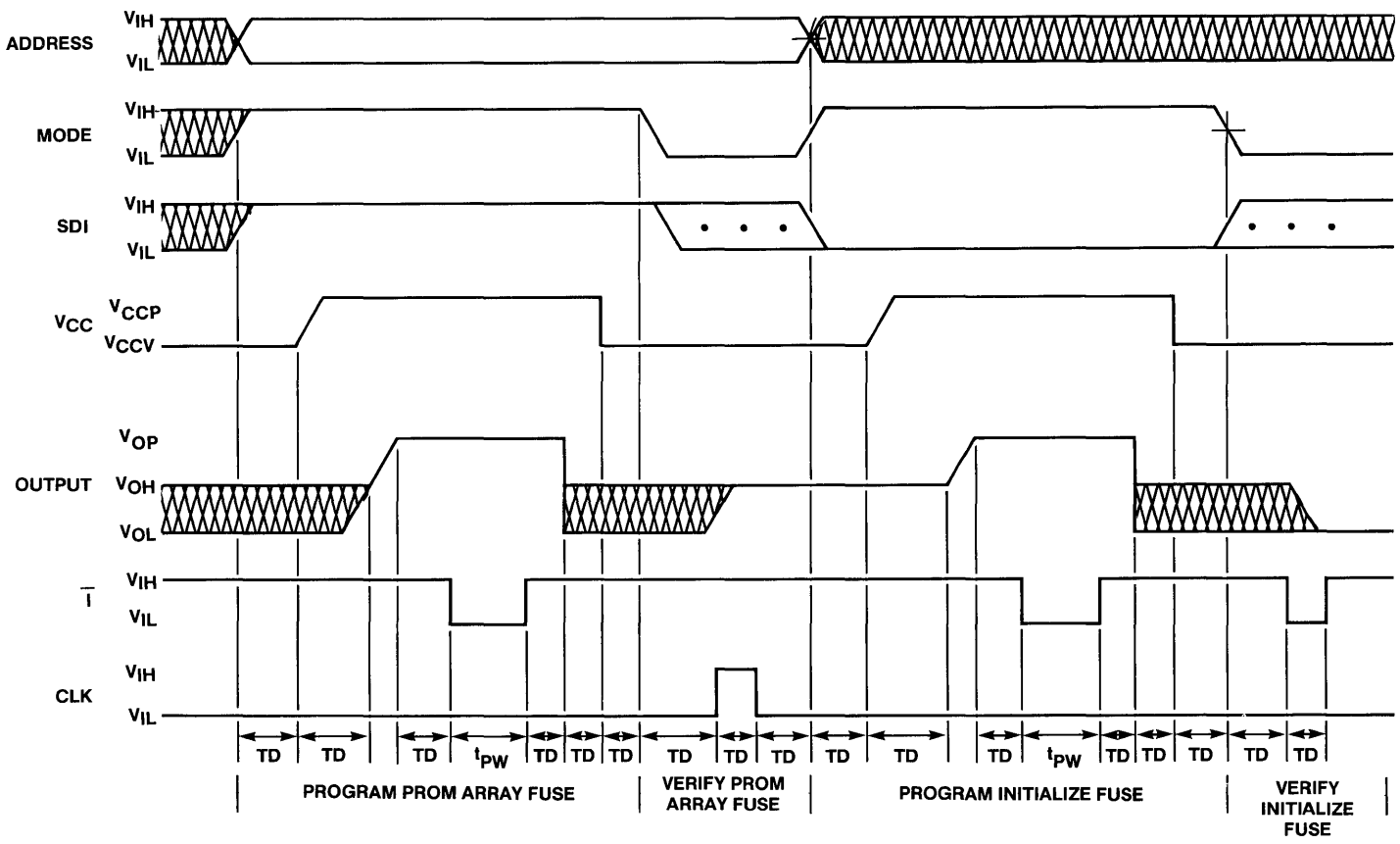
Up to 10 programming pulses should be applied until verification indicates that the bit has programmed. Following verification, apply five additional programming pulses to the bit being programmed.

Programming Parameters

Do not test these parameters or you may program the device.

SYMBOL	PARAMETER	MIN	RECOMMENDED VALUE	MAX	UNIT
V_{CCP}	Required V_{CC} for programming	11.5	11.75	12.0	V
V_{OP}	Required output voltage for programming	10.5	11.0	11.5	V
t_R	Rise time of V_{CC} or V_{OUT}	1.0	5.0	10.0	V/μs
I_{CCP}	Current limit of V_{CCP} supply	800	1200	—	mA
I_{OP}	Current limit of V_{OP} supply	15	20	—	mA
t_{PW}	Programming pulse width (enabled)	9	10	11	μs
V_{CC}	Low V_{CC} for verification	4.2	4.3	4.4	V
V_{CC}	High V_{CC} for verification	5.8	6.0	6.2	V
MDC	Maximum duty cycle of V_{CCP}	—	25	25	%
t_D	Delay time between programming steps	100	120	—	ns
V_{IL}	Input low level	0	0	0.5	V
V_{IH}	Input high level	2.4	3.0	5.5	V

Programming Waveforms



Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

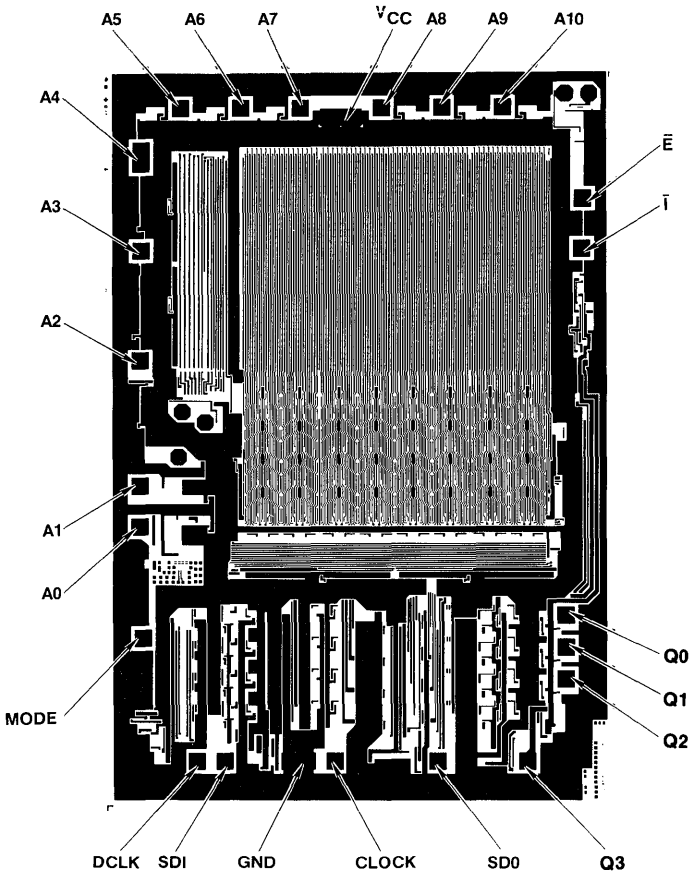
Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltage must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

MANUFACTURER	PROGRAMMER TYPE	PROGRAMMING MODULE	SOCKET CONFIGURATION
Data I/O*	Unipack Rev V07 Unipack 2 Rev V05	Family Code AA	Pinout Code AD

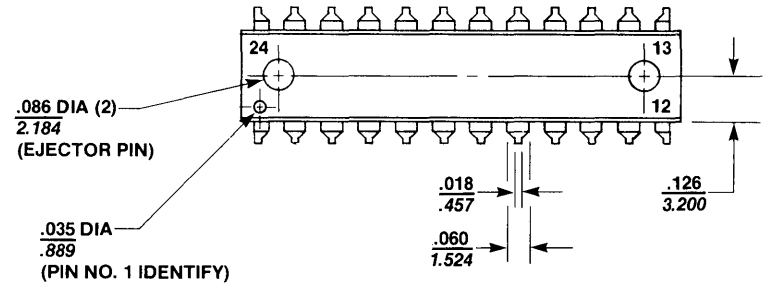
* Use socket adapter 351A-073 Rev. A.

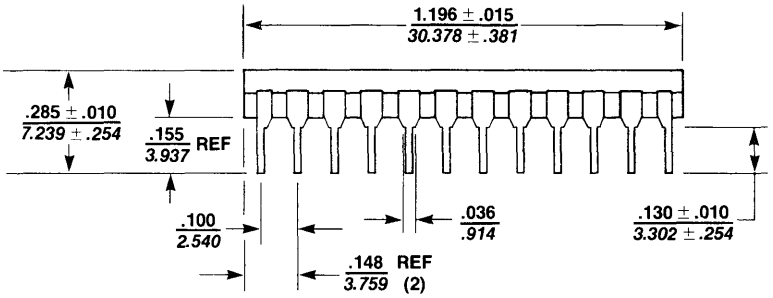
Metal Mask Layout

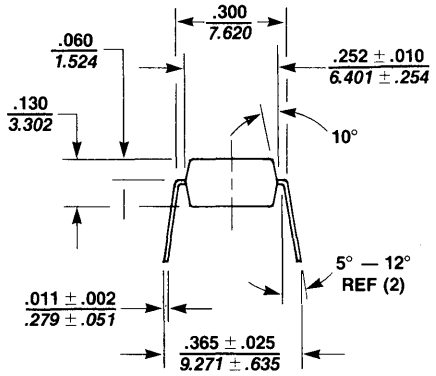


Package Drawings

N24S Molded SKINNYDIP

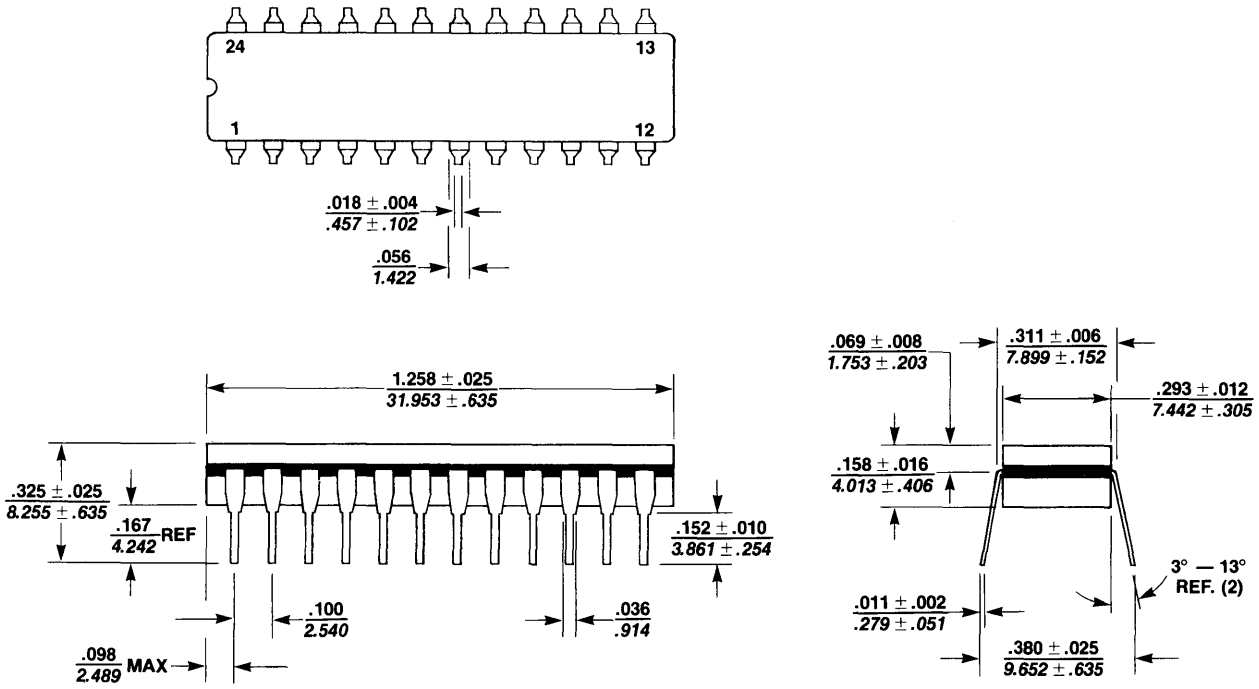




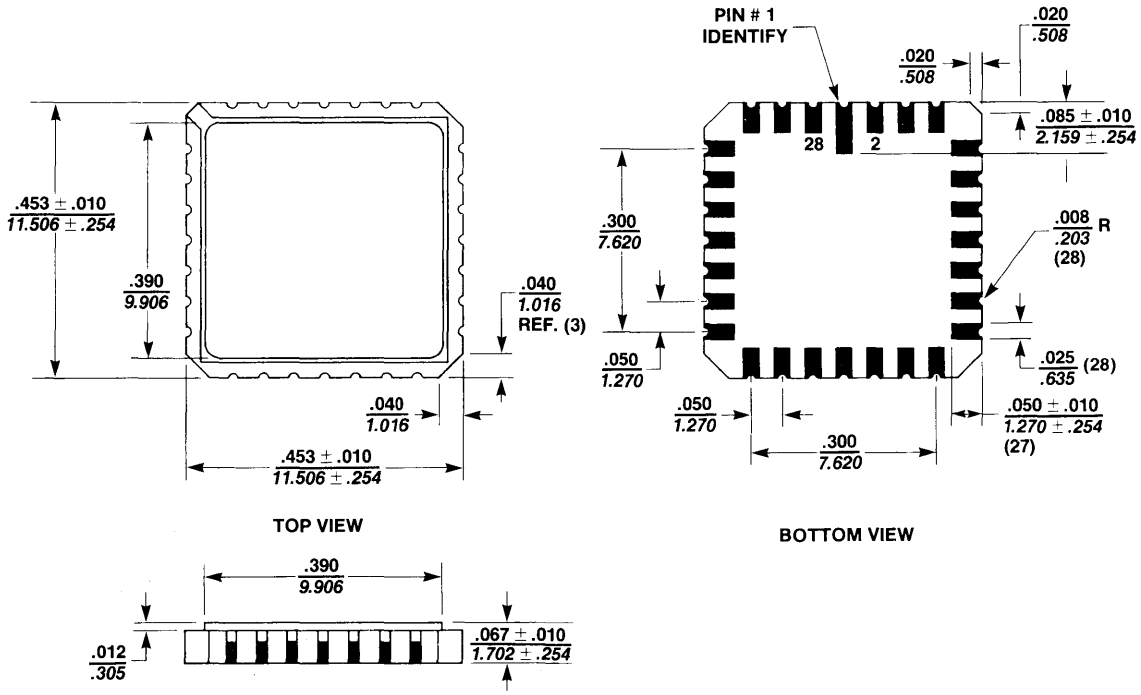


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

J24S Ceramic SKINNYDIP



L28 Leadless Chip Carrier



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