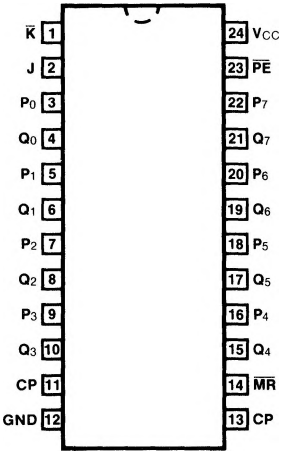
54/74199

8-BIT PARALLEL I/O SHIFT REGISTER

DESCRIPTION — The '199 is a parallel in, parallel out register featuring synchronous parallel load, shift right and hold modes. State changes are initiated by the rising edge of the clock. Serial entry into the first stage is via J and $\overline{K}$ inputs for maximum flexibility. Two clock inputs are provided and it is possible to use one as an inhibit. An asynchronous Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register.

- **PARALLEL IN/PARALLEL OUT**
- **SYNCHRONOUS PARALLEL LOAD**
- **ASYNCHRONOUS OVERRIDING CLEAR**
- **J$\overline{K}$ ENTRY TO FIRST STAGE**

CONNECTION DIAGRAM
PINOUT A



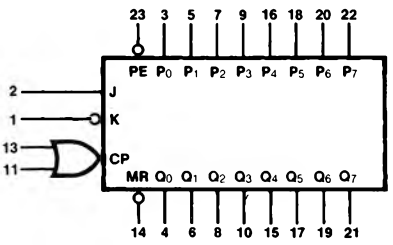
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74199PC		9N
Ceramic DIP (D)	A	74199DC	54199DM	6N
Flatpak (F)	A	74199FC	54199FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{K}$	Serial Data Input (Active LOW)	1.0/1.0
J	Serial Data Input (Active HIGH)	1.0/1.0
P_0 — P_7	Parallel Data Inputs	1.0/1.0
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0
Q_0 — Q_7	Flip-flop Outputs	20/10

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

FUNCTIONAL DESCRIPTION — The '199 contains eight edge-triggered D-type flip-flops and the interstage gating required to perform synchronous parallel load and shift right operations. Parallel input data is applied to the P_0 — P_7 inputs, while serial entry to Q_0 is via J and $\overline{K}$. State changes are initiated by the rising edge of the clock. The J, $\overline{K}$, P_0 — P_7 and $\overline{PE}$ inputs can change while the clock is in either state, provided only that the recommended setup and hold times are observed.

Either CP input can be used as the clock; if one is not used it must be tied LOW. One CP input can be used to inhibit the other by applying a HIGH signal, but this should only be done while the other CP is in the HIGH state or else false triggering may result. A LOW signal on $\overline{MR}$ overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	$\overline{PE}$	CP_1*	CP_2*	
L	X	X	X	Asynchronous Reset; Outputs = LOW
H	X	H	X	Hold
H	X	X	H	
H	L	L	↓	Parallel Load; $P_n \longrightarrow Q_n$
H	L	↓	L	
H	H	L	↓	Shift Right, $Q_0 \longrightarrow Q_1$, $Q_1 \longrightarrow Q_2$, etc.
H	H	↓	L	

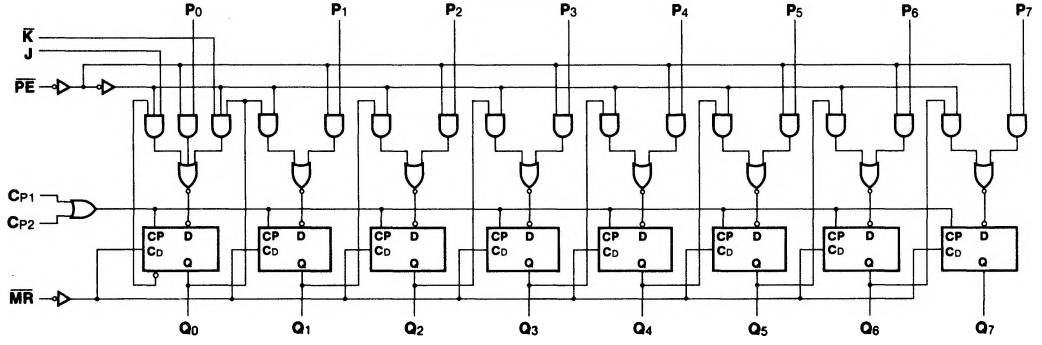
*See discussion for precautions on CP changes
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SERIAL ENTRY TABLE
($\overline{MR}$ = $\overline{PE}$ = HIGH)

INPUTS		Q_0 at t_{n+1}*
J	$\overline{K}$	
L	L	L
L	H	Q_0 at t_n (No Change)
H	L	$\overline{Q}_0$ at t_n (Toggles)
H	H	H

*t_n, t_{n+1} = time before, after rising CP edge

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XC		116	mA	V_{CC} = Max; J, $\overline{K}$, P_n = 4.5 V CP_1 = ⎍⎍ CP_2, $\overline{MR}$, $\overline{PE}$ = Gnd
		XM		104		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_1 or CP_2 to Q_n		26 30	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		35	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n, $\overline{K}$, J to CP	20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n, $\overline{K}$, J to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP	30 30		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{PE}$ to CP	0 0		ns	
t_w (H)	CP Pulse Width HIGH	20		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16