

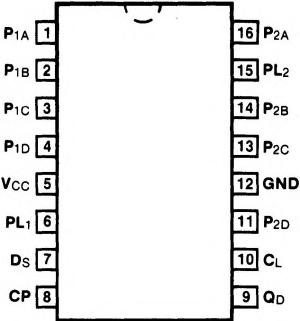
54/7494 4-BIT SHIFT REGISTER

DESCRIPTION — The '94 contains four dc coupled RS master/slave flip-flops with serial data entry into the first stage for synchronous Serial-in-/Serial-out operation, and with a common asynchronous Clear and two sets of individual asynchronous Preset inputs. Preset inputs P_{1x} are enabled by a HIGH signal on PL₁ and Preset inputs P_{2x} are enabled by a HIGH signal on PL₂. The normal procedure for parallel entry of data consists of re-setting the flip-flops by applying a momentary HIGH signal to CL, followed by a HIGH signal on either PL₁, or PL₂, depending on which set of parallel data is desired. For serial operation the CL and both PL inputs must be LOW. Serial transfer is initiated by the rising edge of the clock.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	7494PC		9B
Ceramic DIP (D)	A	7494DC	5494DM	7B
Flatpak (F)	A	7494FC	5494FM	4L

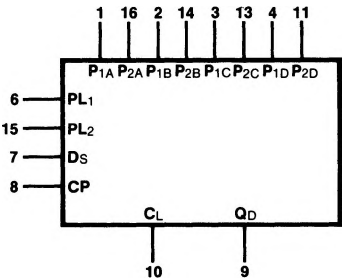
CONNECTION DIAGRAM PINOUT A



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
P _{1A} — P _{1D}	Source 1 Parallel Data Inputs	1.0/1.0
P _{2A} — P _{2D}	Source 2 Parallel Data Inputs	1.0/1.0
PL ₁	Asynchronous Parallel Load Input (Source 1)	4.0/4.0
PL ₂	Asynchronous Parallel Load Input (Source 2)	4.0/4.0
D _S	Serial Data Input	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
CL	Asynchronous Clear Input (Active HIGH)	1.0/1.0
Q _D	Serial Data Output	10/10

LOGIC SYMBOL



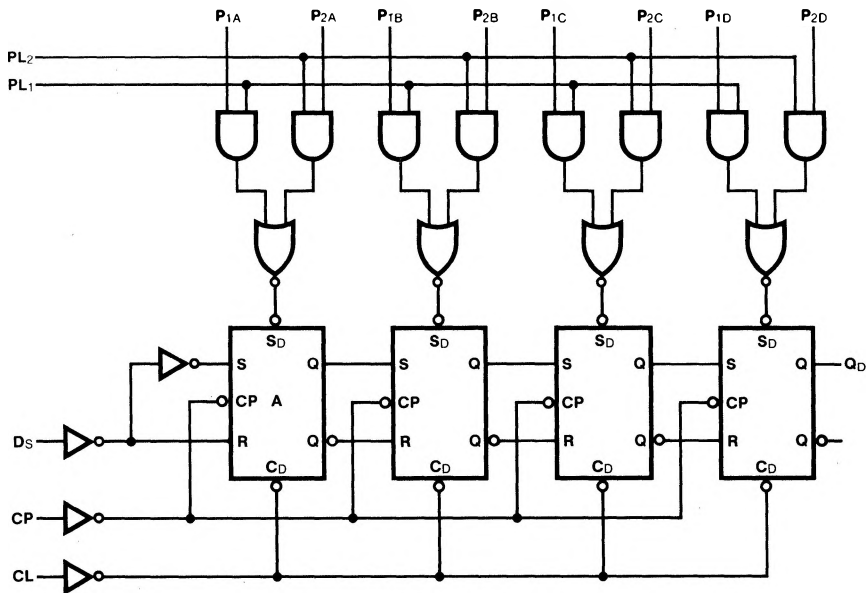
V_{CC} = Pin 5
GND = Pin 12

TRUTH TABLE

INPUTS				OUTPUTS	RESPONSE
CP	CL	PL ₁ • P _{1D}	PL ₂ • P _{2D}	Q _D	
X	H	L	L	L	Clear
X	L	H	X	H	Preset
X	L	X	H	H	Preset
X	H	H	X	H	Indeterminate
X	H	X	H	H	Indeterminate
✓	L	L	L	Q _C	Shift Right

NOTE: All four flip-flops respond in a similar manner.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
I _{CC}	Power Supply Current	XM	50	mA	V _{CC} = Max
		XC	58		

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		CL = 15 pF RL = 400 Ω			
		Min	Max		
fmax	Maximum Shift Frequency	10		MHz	Figs. 3-1, 3-8
tPLH tPHL	Propagation Delay CP to QD	40 40		ns	Figs. 3-1, 3-8
tPLH	Propagation Delay, PLn to QD	35		ns	Figs. 3-1, 3-17
tPHL	Propagation Delay, CL to QD	40			

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
t _s (H)	Setup Time HIGH, D _S to CP	35		ns	Fig. 3-6
t _h (H)	Hold Time HIGH, D _S to CP	0		ns	
t _s (L)	Setup Time LOW, D _S to CP	25		ns	Fig. 3-6
t _h (L)	Hold Time LOW, D _S to CP	0		ns	
t _w (H)	CP Pulse Width HIGH	35		ns	Fig. 3-8
t _w (H)	CL Pulse Width HIGH	30		ns	Fig. 3-16
t _w (H)	PL _n Pulse Width HIGH	30		ns	Fig. 3-16