54ABT16244

54ABT16244 16-Bit Buffer/Line Driver with TRI-STATE Outputs

Literature Number: SNOS050A

National Semiconductor

54ABT16244

OBSOLETE
September 10, 2009

16-Bit Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'ABT16244 contains sixteen non-inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

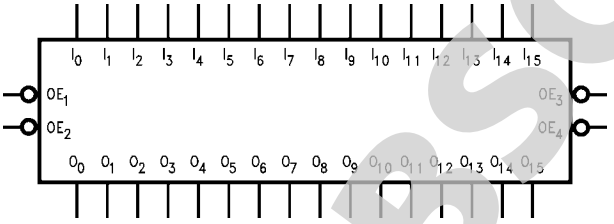
Features

- Separate control logic for each nibble
- 16-bit version of the 'ABT244
- Outputs sink capability of 48 mA, source capability of 24 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9317402

Ordering Code

Military	Package Number	Package Description
54ABT16244W-QML	WA48A	48-Lead Cerpack

Logic Symbol



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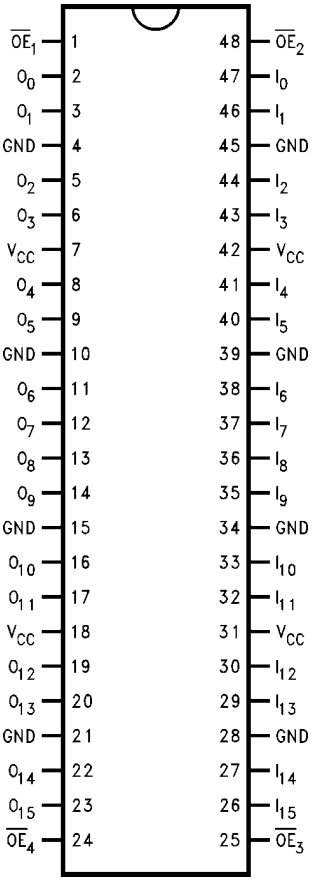
Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

Connection Diagram

Pin Assignment for Cerpack



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Functional Description

The 'ABT16244 contains sixteen non-inverting buffers with TRI-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Table

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

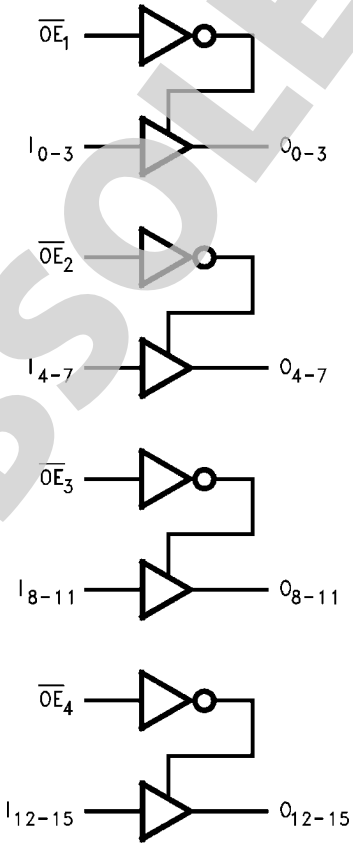
Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



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Absolute Maximum Ratings (*Note 1*)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (*Note 2*)	−0.5V to +7.0V
Input Current (*Note 2*)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		ABT16244 Min	ABT16244 Typ	ABT16244 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −24 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (*Note 3*)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (*Note 3*)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V All Other Pins GND
I_{CCH}	Power Supply Current				2.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				2.0	mA	Max	$\overline{OE}_n$ = V_{CC} All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			50	μA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (*Note 3*)	No Load			0.1	mA/MHz	Max	Outputs Open, $\overline{OE}_n$ = GND One Bit Toggling, 50% Duty Cycle

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Note 3: Guaranteed but not tested.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		1.1	V	5.0	T_A = 25°C (*Note 4*)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		-0.45	V	5.0	T_A = 25°C(*Note 4*)

Note 4: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW.

AC Electrical Characteristics

Symbol	Parameter	54ABT T_A = –55°C to +125°C V_{CC} = 4.5V–5.5V C_L = 50 pF		Units	Fig. No.
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Outputs	0.5 0.5	5.3 5.9	ns	*Figure 2*
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5	6.8 7.0	ns	*Figure 5*
t_{PHZ} t_{PLZ}	Output Disable Time	1.5 1.5	7.7 6.5	ns	*Figure 5*

Capacitance

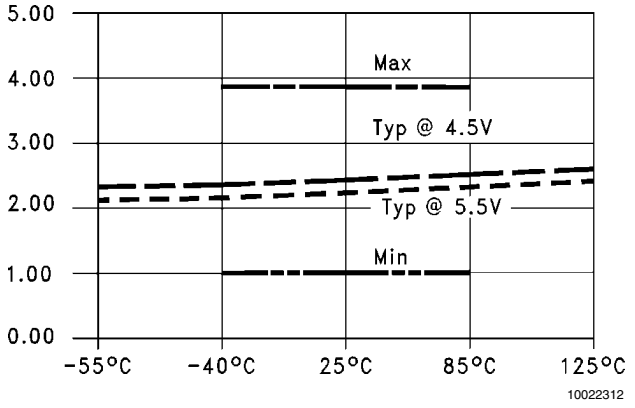
Symbol	Parameter	Typ	Units	Conditions T_A = 25°C
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 5.0V
C_{OUT} (*Note 5*)	Output Capacitance	9.0	pF	V_{CC} = 5.0V

Note 5: C_{OUT} is measured at frequency f = 1 MHz; per MIL STD-883B, Method 3012.

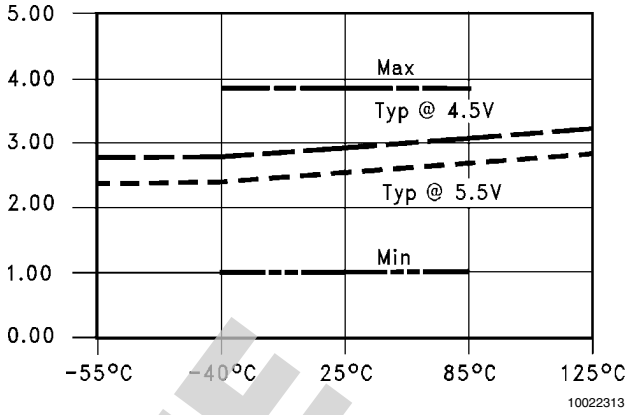
Capacitance

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

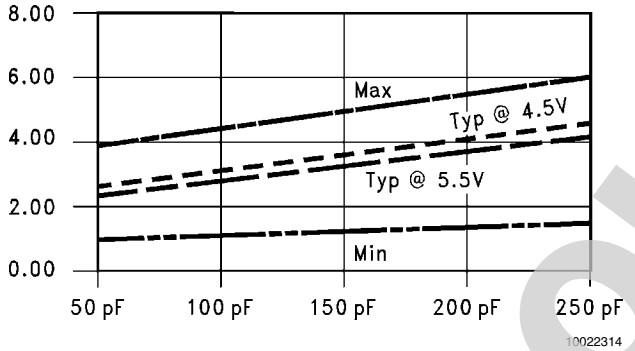
t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



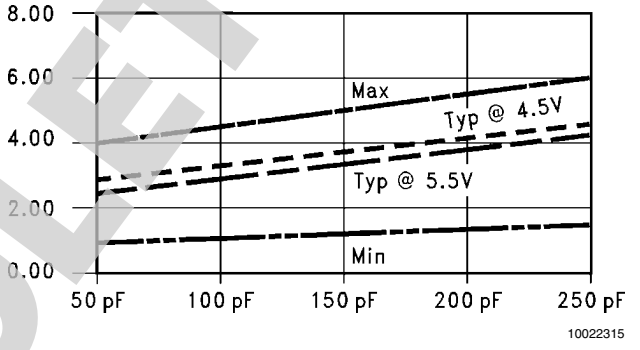
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



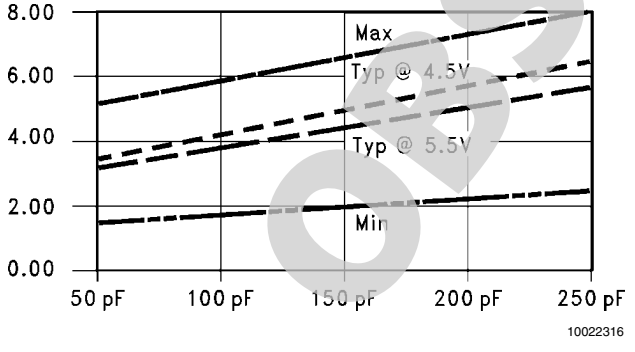
t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C



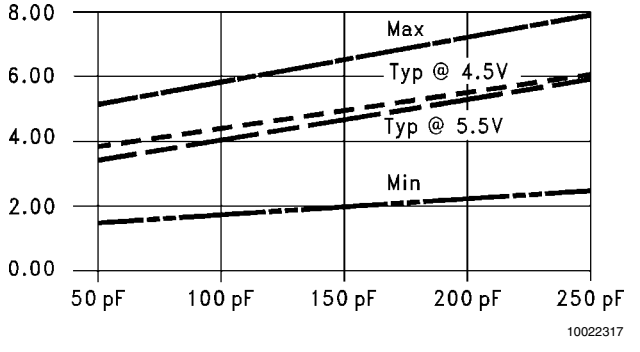
t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C



t_{PLH} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



t_{PHL} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



Note: Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

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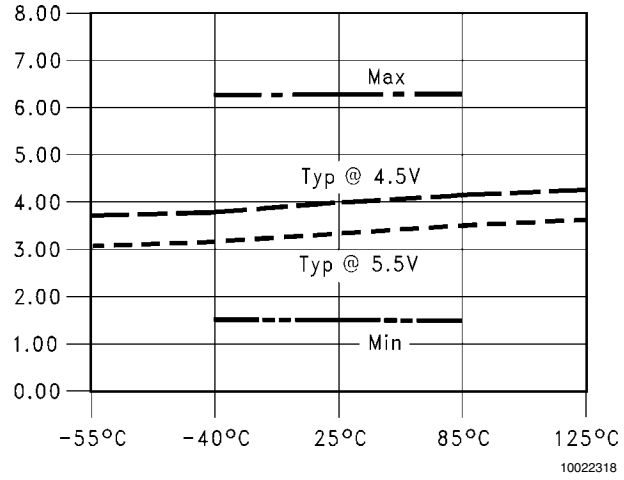
t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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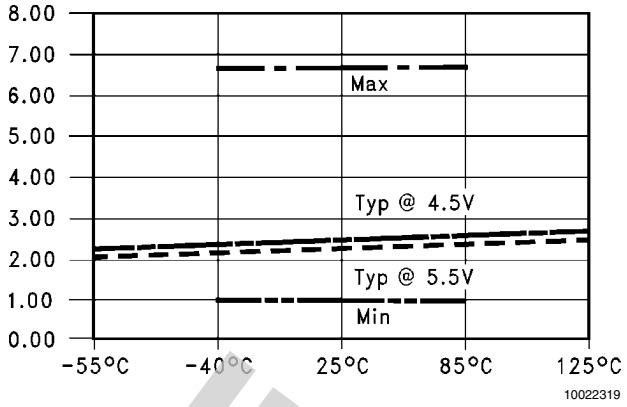
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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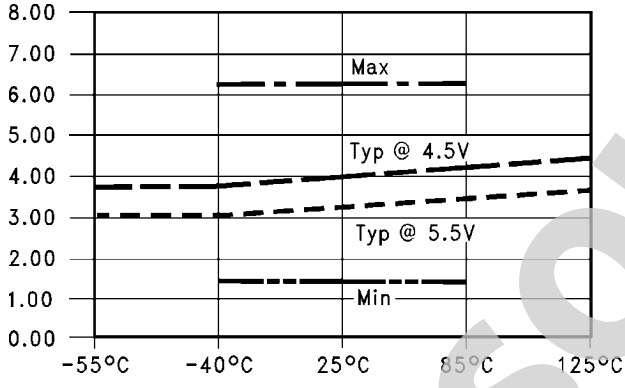
t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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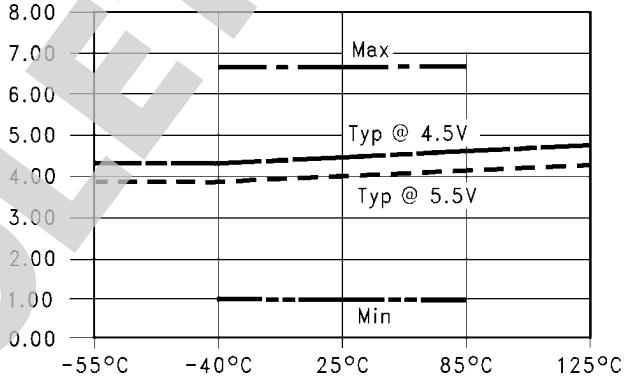
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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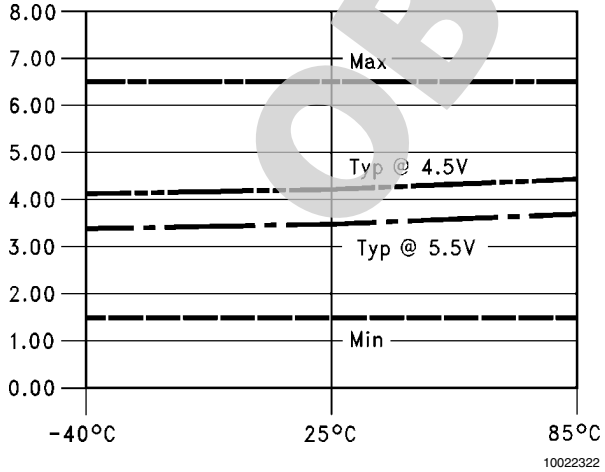
t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



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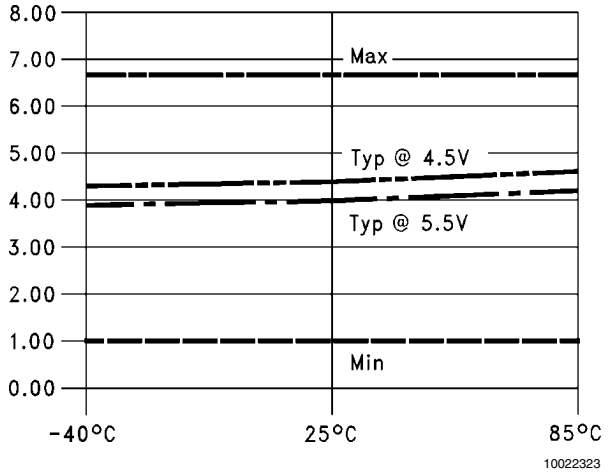
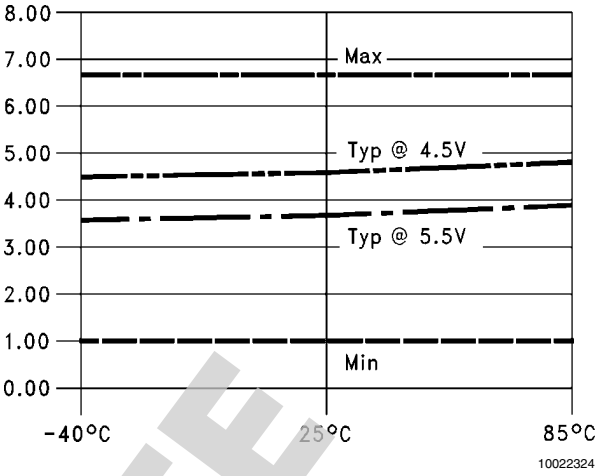
Note: Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

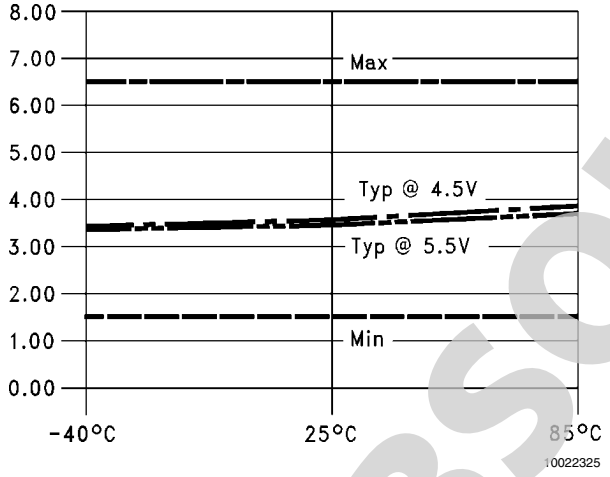
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



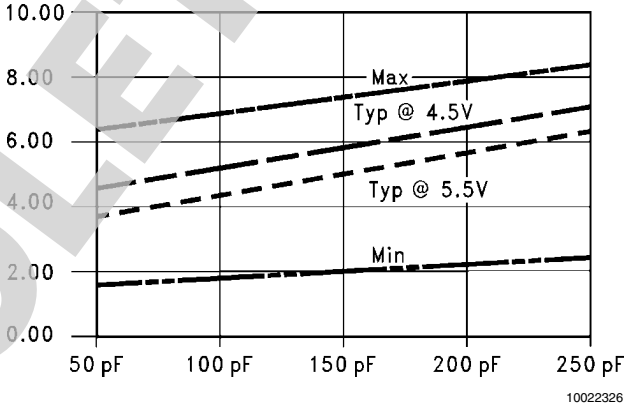
t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



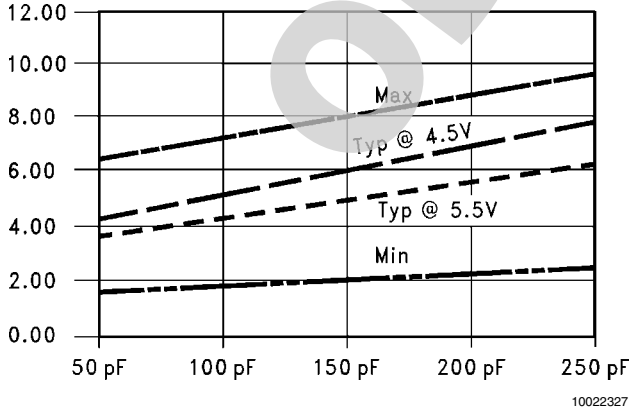
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



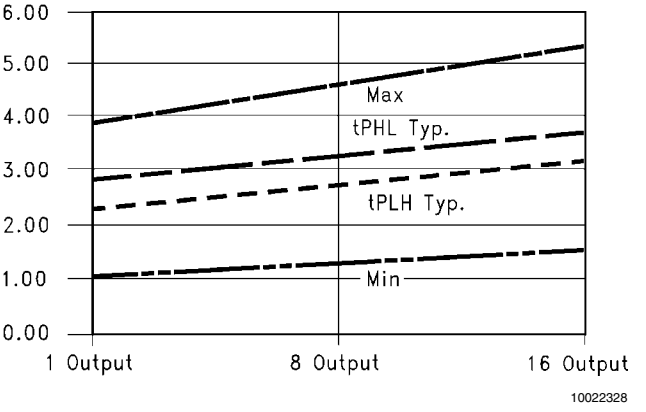
t_{PZL} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



t_{PZH} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



t_{PLH} and t_{PHL} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



Note: Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

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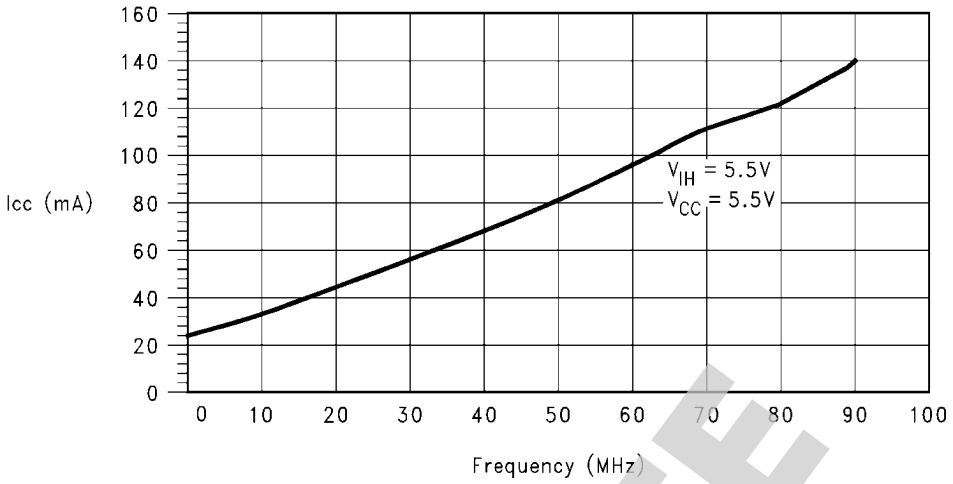
I_{CC} vs Frequency Average,
T_A = 25°C, V_{CC} = 5.5V



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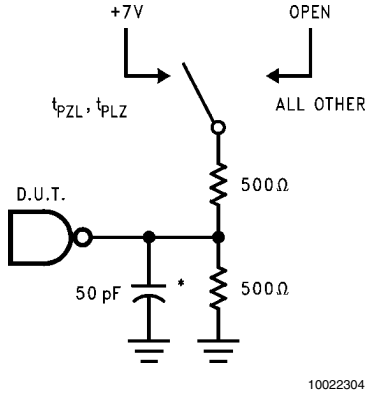
Note: Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

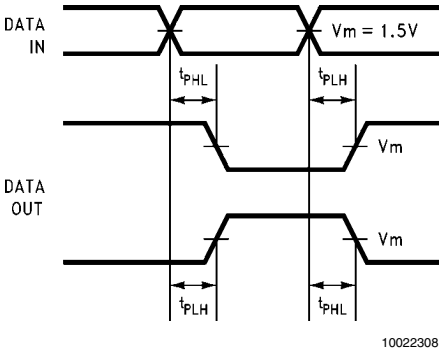


FIGURE 2. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

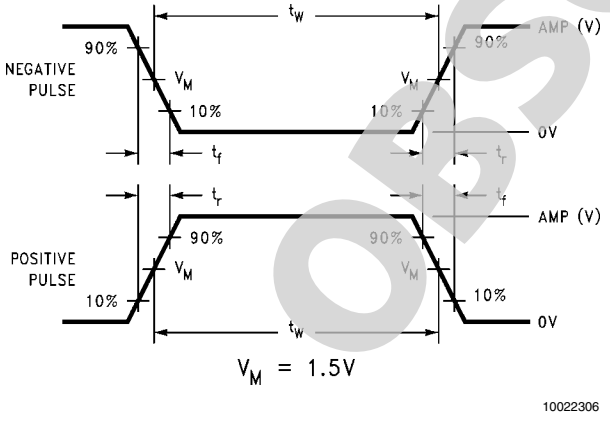


FIGURE 3. Test Input Pulse Requirements

Amplitude	Rep Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 4. Test Input Signal Requirements

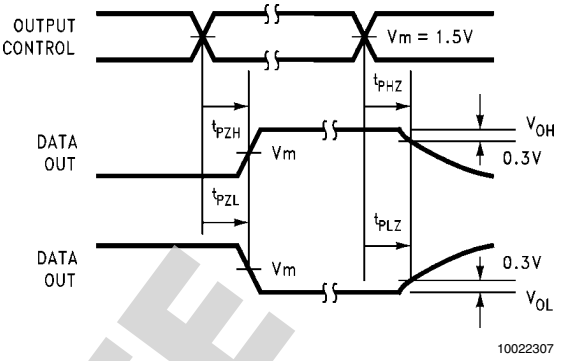


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

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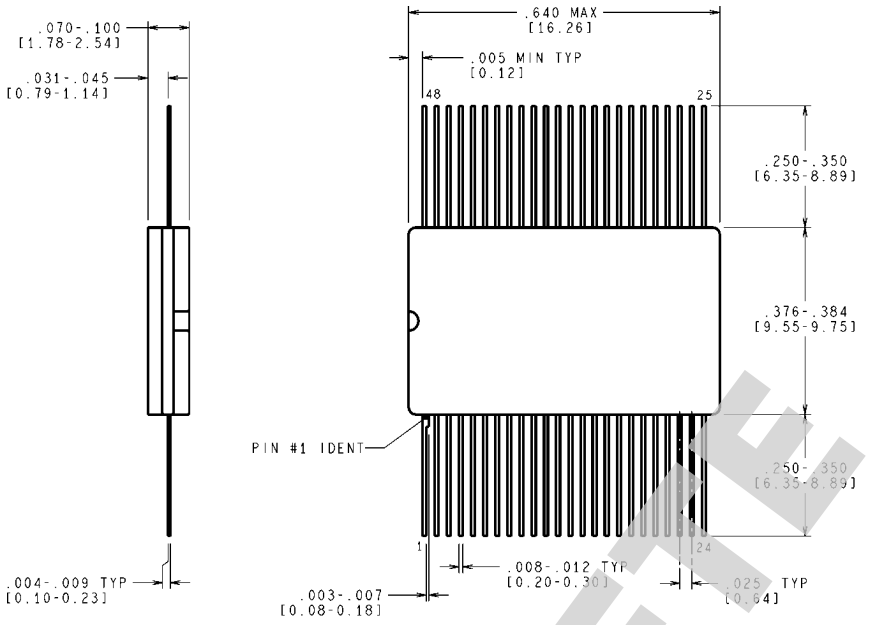
Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

WA48A (Rev B)

48-Lead Cerpack
NS Package Number WA48A

Notes

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Notes

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
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Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

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