54AC158 • 54ACT158 Quad 2-Input Multiplexer

Check for Samples: 54AC158, 54ACT158

FEATURES

- **I_{CC} reduced by 50%**
- **Outputs source/sink 24 mA**
- **'ACT158 has TTL-compatible inputs**
- **Standard Microcircuit Drawing (SMD)**
  - **'AC158: 5962-89729**
  - **'ACT158: 5962-88755**

DESCRIPTION

The 'AC/'ACT158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 'AC/'ACT158 can also be used as a function generator.

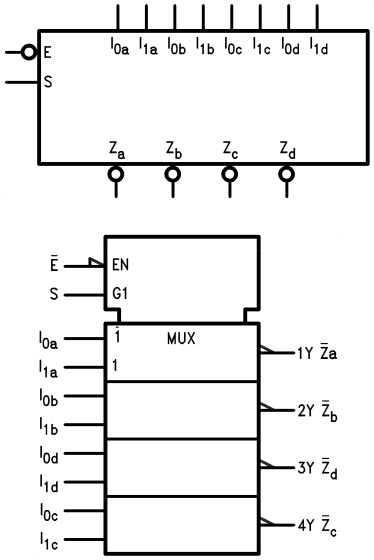


Figure 1. IEE/IEC

Connection Diagram

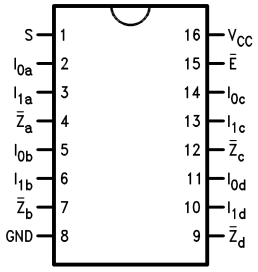


Figure 2. Pin Assignment for DIP and Flatpak

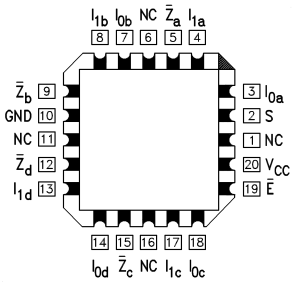


Figure 3. Pin Assignment for LCC

Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
$\overline{Z}_a$–$\overline{Z}_d$	Inverted Outputs

Functional Description

The 'AC/'ACT158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs. The 'AC/'ACT158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

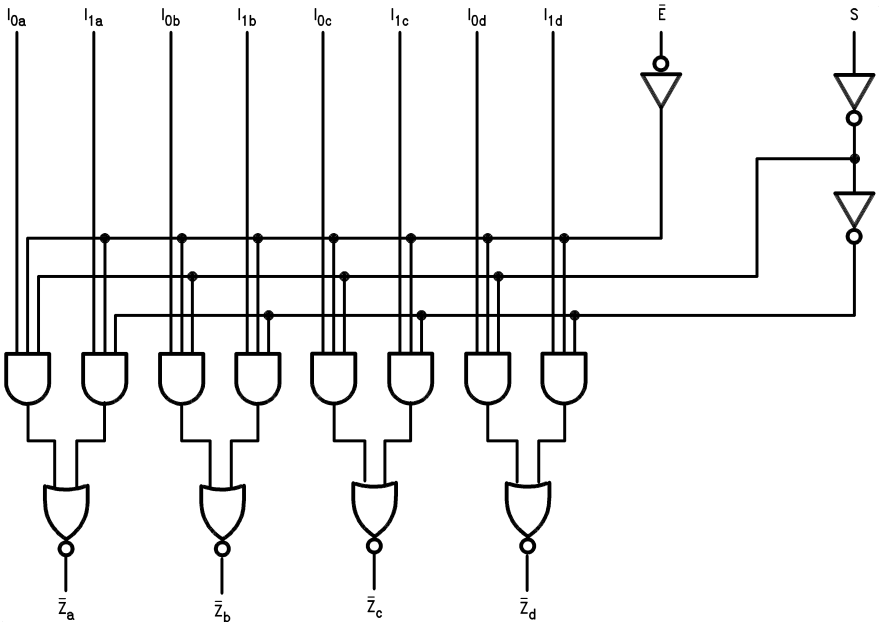
A common use of the 'AC/'ACT158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'AC/'ACT158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table
(1)

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

(1) H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended OperatingConditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V

Recommended OperatingConditions (continued)

Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

			54AC		
Symbol	**Parameter**	**V_{CC}**	**T_A =**	**Units**	**Conditions**
		(V)	**−55°C to +125°C**		
			Guaranteed Limits		
V_{IH}	Minimum High Level	3.0	2.1		V_{OUT} = 0.1V
	Input Voltage	4.5	3.15	V	or V_{CC} − 0.1V
		5.5	3.85		
V_{IL}	Maximum Low Level	3.0	0.9		V_{OUT} = 0.1V
	Input Voltage	4.5	1.35	V	or V_{CC} − 0.1V
		5.5	1.65		
V_{OH}	Minimum High Level	3.0	2.9		I_{OUT} = −50 µA
	Output Voltage	4.5	4.4	V	
		5.5	5.4		
					(1) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4		I_{OH} = −12 mA
		4.5	3.7	V	I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level	3.0	0.1		I_{OUT} = 50 µA
	Output Voltage	4.5	0.1	V	
		5.5	0.1		
					(1) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50		I_{OL} = 12 mA
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input	5.5	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current				
I_{OLD}	Minimum Dynamic Output Current (2)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	80.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices

			54ACT		
Symbol	**Parameter**	**V_{CC}**	**T_A =**	**Units**	**Conditions**
		(V)	**−55°C to +125°C**		
			Guaranteed Limits		
V_{IH}	Minimum High Level	4.5	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level	4.5	0.8	V	V_{OUT} = 0.1V
	Input Voltage	5.5	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5	4.4	V	I_{OUT} = −50 µA
	Output Voltage	5.5	5.4		
					(1) V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Level	4.5	0.1	V	I_{OUT} = 50 µA
	Output Voltage	5.5	0.1		
					(1) V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input	5.5	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current				
I_{CCT}	Maximum	5.5	1.6	mA	V_I = V_{CC} − 2.1V
	I_{CC}/Input				
I_{OLD}	Minimum Dynamic Output Current (2)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	80.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

			54AC			
		V_{CC}	T_A = −55°C			Fig.
Symbol	Parameter	(V)	to +125°C		Units	No.
		(1)	C_L = 50 pF			
			Min	Max		
t_{PLH}	Propagation Delay	3.3	1.0	14.0	ns	
	S to $\overline{Z}_n$	5.0	1.0	11.0		
t_{PHL}	Propagation Delay	3.3	1.0	14.0	ns	
	S to $\overline{Z}_n$	5.0	1.0	11.0		
t_{PLH}	Propagation Delay	3.3	1.0	15.0	ns	
	$\overline{E}$ to $\overline{Z}_n$	5.0	1.0	12.0		
t_{PHL}	Propagation Delay	3.3	1.0	14.0	ns	
	$\overline{E}$ to $\overline{Z}_n$	5.0	1.0	10.0		
t_{PLH}	Propagation Delay	3.3	1.0	11.0	ns	
	I_n to $\overline{Z}_n$	5.0	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.0	10.0	ns	
	I_n to $\overline{Z}_n$	5.0	1.0	7.5		

(1) Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

			54ACT			
		V_{CC}	T_A = −55°C			Fig.
Symbol	Parameter	(V)	to +125°C		Units	No.
		(1)	C_L = 50 pF			
			Min	Max		
t_{PLH}	Propagation Delay	5.0	1.0	12.0	ns	
	S to $\overline{Z}_n$					
t_{PHL}	Propagation Delay	5.0	1.0	11.5	ns	
	S to $\overline{Z}_n$					
t_{PLH}	Propagation Delay	5.0	1.0	11.0	ns	
	$\overline{E}$ to $\overline{Z}_n$					
t_{PHL}	Propagation Delay	5.0	1.0	11.0	ns	
	$\overline{E}$ to $\overline{Z}_n$					
t_{PLH}	Propagation Delay	5.0	1.0	9.5	ns	
	I_n to $\overline{Z}_n$					
t_{PHL}	Propagation Delay	5.0	1.0	8.0	ns	
	I_n to $\overline{Z}_n$					

(1) Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation	45.0	pF	V_{CC} = 5.0V
	Capacitance			

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