54AC174/54ACT174 Hex D Flip-Flop with Master Reset

Check for Samples: 54AC174, 54ACT174

FEATURES

- **I_{CC} reduced by 50%**
- **Outputs source/sink 24 mA**
- **'ACT174 has TTL-compatible inputs**
- **Standard Microcircuit Drawing (SMD)**
  - **54AC174: 5962-87626**
  - **54ACT174: 5962-87757**
- **54AC174 now qualified to 300Krad RHA designation, refer to the SMD for more information**

DESCRIPTION

The 'AC/'ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

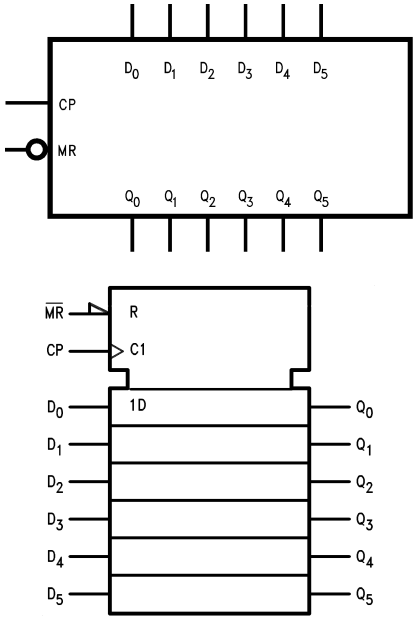


Figure 1. IEEE/IEC

Pin Names	Description
D_0–D_5	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_5	Outputs

Connection Diagram

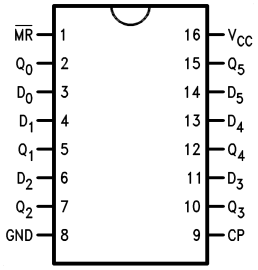


Figure 2. Pin Assignment for DIP and Flatpak

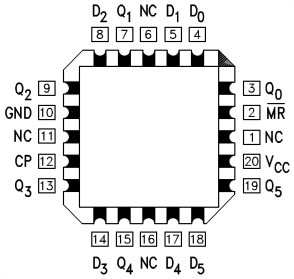


Figure 3. Pin Assignment for LCC

Functional Description

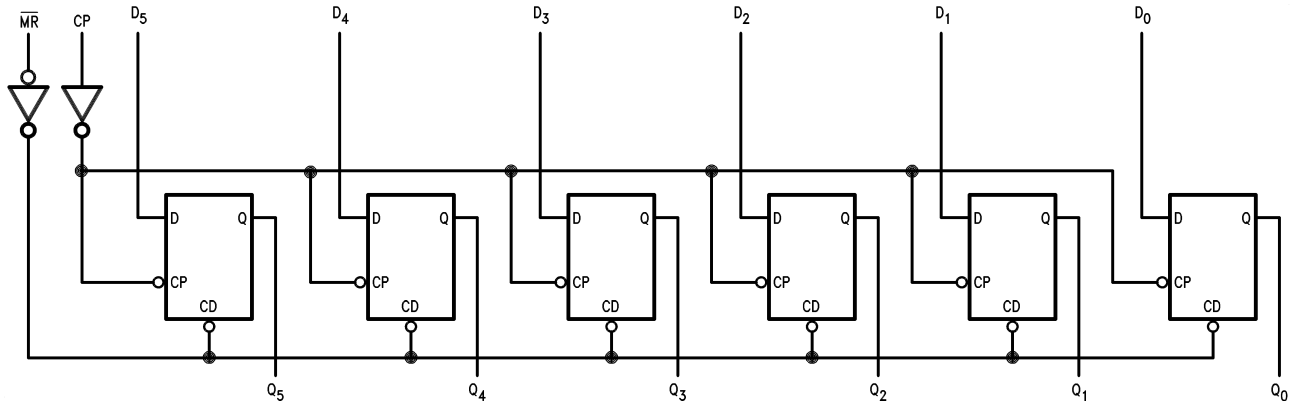
The 'AC/'ACT174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The 'AC/'ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table
(1)

Inputs			Output
$\overline{MR}$	CP	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	Q

(1) H = HIGH Voltage Level
L = LOW Voltage Level
= LOW-to-HIGH Transition
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended OperatingConditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	

Recommended OperatingConditions (continued)

V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

			54AC		
Symbol	**Parameter**	**V_{CC}**	**T_A =**	**Units**	**Conditions**
		(V)	**−55°C to +125°C**		
			Guaranteed Limits		
V_{IH}	Minimum High Level	3.0	2.1		V_{OUT} = 0.1V
	Input Voltage	4.5	3.15	V	or V_{CC} − 0.1V
		5.5	3.85		
V_{IL}	Maximum Low Level	3.0	0.9		V_{OUT} = 0.1V
	Input Voltage	4.5	1.35	V	or V_{CC} − 0.1V
		5.5	1.65		
V_{OH}	Minimum High Level	3.0	2.9		I_{OUT} = −50 µA
	Output Voltage	4.5	4.4	V	
		5.5	5.4		
					(1) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4		I_{OH} = −12 mA
		4.5	3.7	V	I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level	3.0	0.1		I_{OUT} = 50 µA
	Output Voltage	4.5	0.1	V	
		5.5	0.1		
					(1) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50		I_{OL} = 12 mA
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input	5.5	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current				
I_{OLD}	Minimum Dynamic Output Current (2)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	80.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices

			54ACT		
Symbol	**Parameter**	**V_{CC}**	**T_A =**	**Units**	**Conditions**
		(V)	**−55°C to +125°C**		
			Guaranteed Limits		
V_{IH}	Minimum High Level	4.5	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level	4.5	0.8	V	V_{OUT} = 0.1V
	Input Voltage	5.5	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5	4.4	V	I_{OUT} = −50 µA
	Output Voltage	5.5	5.4		
					(1) V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Level	4.5	0.1	V	I_{OUT} = 50 µA
	Output Voltage	5.5	0.1		
					(1) V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input	5.5	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current				
I_{CCT}	Maximum	5.5	1.6	mA	V_I = V_{CC} − 2.1V
	I_{CC}/Input				
I_{OLD}	Minimum Dynamic Output Current (2)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	80.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (1)	54AC T_A = −55°C to +125°C C_L = 50 pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Clock	3.3	65		MHz	
	Frequency	5.0	90			
t_{PLH}	Propagation Delay	3.3	1.0	14.0	ns	
	CP to Q_n	5.0	1.5	10.5		
t_{PHL}	Propagation Delay	3.3	1.0	13.0	ns	
	CP to Q_n	5.0	1.5	10.0		
t_{PHL}	Propagation Delay	3.3	1.0	13.5	ns	
	$\overline{MR}$ to Q_n	5.0	1.5	11.0		

(1) Voltage Range 3.3 is 3.3V ±0.3VVoltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

			54AC		
		V_{CC}	T_A = −55°C		Fig.
Symbol	Parameter	(V)	to +125°C	Units	No.
		(1)	C_L = 50 pF		
			Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW	3.3	7.5	ns	
	D_n to CP	5.0	5.5		
t_h	Hold Time, HIGH or LOW	3.3	3.0	ns	
	D_n to CP	5.0	3.0		
t_w	$\overline{MR}$ Pulse Width, LOW	3.3	7.0	ns	
		5.0	5.0		
t_w	CP Pulse Width	3.3	7.0	ns	
		5.0	5.0		
t_{rec}	Recovery Time	3.3	3.0	ns	
	$\overline{MR}$ to CP	5.0	2.0		

(1) Voltage Range 3.3 is 3.3V ±0.3VVoltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (1)	54ACT T_A = −55°C to +125°C, C_L = 50 pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Clock	5.0	95		MHz	
	Frequency					
t_{PLH}	Propagation Delay	5.0	1.5	12.5	ns	
	CP to Q_n					
t_{PHL}	Propagation Delay	5.0	1.5	13.0	ns	
	CP to Q_n					
t_{PHL}	Propagation Delay	5.0	1.5	12.0	ns	
	$\overline{MR}$ to Q_n					

(1) Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

			54ACT		
		V_{CC}	T_A = −55°C		Fig.
Symbol	Parameter	(V)	to +125°C	Units	No.
		(1)	C_L = 50 pF		
			Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW	5.0	3.0	ns	
	D_n to CP				
t_h	Hold Time, HIGH or LOW	5.0	2.0	ns	
	D_n to CP				
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	5.0	ns	
t_w	CP Pulse Width, HIGH OR LOW	5.0	5.0	ns	
t_{rec}	Recovery Time	5.0	1.0	ns	
	$\overline{MR}$ to CP				

(1) Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation	85.0	pF	V_{CC} = 5.0V
	Capacitance			

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