National Semiconductor

# 54ACQ/74ACQ153 • 54ACTQ/74ACTQ153
# Quiet Series Dual 4-Input Multiplexer

## General Description

The 'ACQ/'ACTQ153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'ACQ/'ACTQ153 can act as a function generator and generate any two functions of three variables.

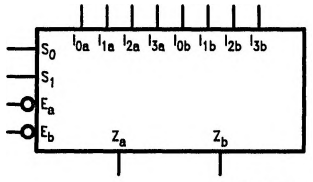
## Features

- Outputs source/sink 24 mA
- 'ACTQ153 has TTL-compatible inputs
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity

**The information for the 'ACQ153 is advanced information only.**

## Ordering Code: See Section 8

## Logic Symbols

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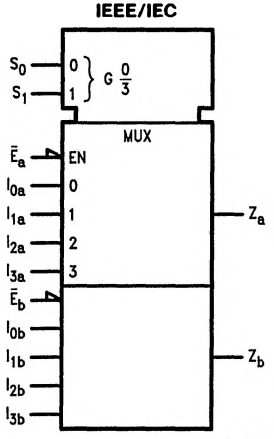


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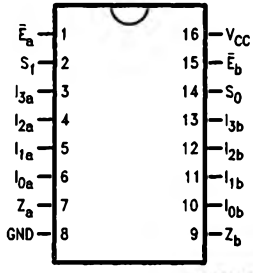
| Pin Names | Description |
|---|---|
| $I_{0a}$–$I_{3a}$ | Side A Data Inputs |
| $I_{0b}$–$I_{3b}$ | Side B Data Inputs |
| $S_0$, $S_1$ | Common Select Inputs |
| $\bar{E}_a$ | Side A Enable Input |
| $\bar{E}_b$ | Side B Enable Input |
| $Z_a$ | Side A Output |
| $Z_b$ | Side B Output |

## Connection Diagrams

**Pin Assignment for DIP, Flatpak and SOIC**

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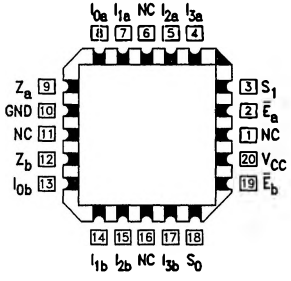
**Pin Assignment for LCC**

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## Functional Description

The 'ACQ/'ACTQ153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs ($S_0$, $S_1$). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($Z_a$, $Z_b$) are forced LOW. The 'ACQ/'ACTQ153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

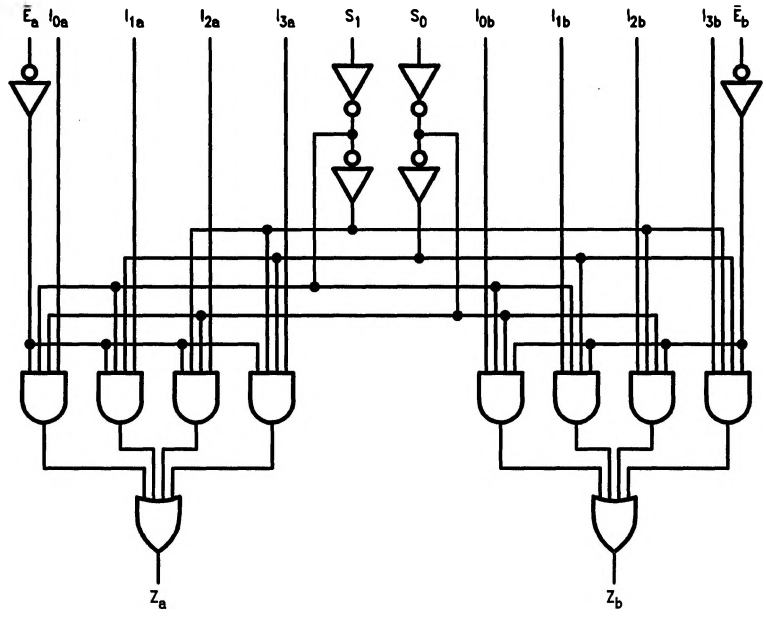
$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

## Truth Table

| Select Inputs | | Inputs (a or b) | | | | | Output |
|---|---|---|---|---|---|---|---|
| $S_0$ | $S_1$ | $\overline{E}$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | Z |
| X | X | H | X | X | X | X | L |
| L | L | L | L | X | X | X | L |
| L | L | L | H | X | X | X | H |
| H | L | L | X | L | X | X | L |
| H | L | L | X | H | X | X | H |
| L | H | L | X | X | L | X | L |
| L | H | L | X | X | H | X | H |
| H | H | L | X | X | X | L | L |
| H | H | L | X | X | X | H | H |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

## Logic Diagram

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to to $V_{CC}$ + 0.5V |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| DC Latch-Up Source or Sink Current | ±300 mA |
| Junction Temperature ($T_J$) | |
| CDIP | 175°C |
| PDIP | 140°C |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| 'ACQ | 2.0V to 6.0V |
| 'ACTQ | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | |
| 74ACQ/ACTQ | −40°C to +85°C |
| 54ACQ/ACTQ | −55°C to +125°C |
| Minimum Input Edge Rate ΔV/Δt 'ACQ Devices $V_{IN}$ from 30% to 70% of $V_{CC}$ $V_{CC}$ @3.0V, 4.5V, 5.5V | 125 mV/ns |
| Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices $V_{IN}$ from 0.8V to 2.0V $V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

## DC Characteristics for 'ACT Family Devices

| Symbol | Parameter | $V_{CC}$ (V) | 74ACTQ $T_A$ = +25°C | | 54ACTQ $T_A$ = −55°C to +125°C | 74ACTQ $T_A$ = −40°C to +85°C | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | | |
| $V_{IH}$ | Minimum High Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | 2.0 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| | | 5.5 | 1.5 | 2.0 | 2.0 | 2.0 | | |
| $V_{IL}$ | Maximum Low Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | 0.8 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| | | 5.5 | 1.5 | 0.8 | 0.8 | 0.8 | | |
| $V_{OH}$ | Minimum High Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | 4.4 | | $I_{OUT}$ = −50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | 5.4 | | |
| | | 4.5 | | 3.86 | 3.70 | 3.76 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$ $I_{OH}$ −24 mA |
| | | 5.5 | | 4.86 | 4.70 | 4.76 | | $I_{OH}$ −24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | 0.1 | | $I_{OUT}$ = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | 0.1 | | |
| | | 4.5 | | 0.36 | 0.50 | 0.44 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$ $I_{OL}$ 24 mA |
| | | 5.5 | | 0.36 | 0.50 | 0.44 | | $I_{OL}$ 24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'ACT Family Devices (Continued)

| Symbol | Parameter | $V_{CC}$ (V) | 74ACTQ $T_A = +25°C$ | | 54ACTQ $T_A = -55°C$ to $+125°C$ | 74ACTQ $T_A = -40°C$ to $+85°C$ | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | Typ | | Guaranteed Limits | | | |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ |
| $I_{OLD}$ | †Minimum Dynamic Output Current | 5.5 | | | 50 | 75 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{IHD}$ | | 5.5 | | | −50 | −75 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ | Maximum Quiescent Supply Curent | 5.5 | | 8.0 | 160.0 | 80.0 | μA | $V_{IN} = V_{CC}$ or GND (Note 1) |
| $V_{OLP}$ | Maximum High Level Output Noise | 5.0 | 1.1 | 1.5 | | | V | *Figures 1, 2* (Note 2, 3) |
| $V_{OLV}$ | Maximum Low Level Output Noise | 5.0 | −0.6 | −1.2 | | | V | *Figures 1, 2* |
| $V_{IHD}$ | Maximum High Level Dynamic Input Voltage | 5.0 | 1.9 | 2.2 | | | V | (Notes 2, 4) |
| $V_{ILD}$ | †Maximum Low Level Dynamic Input Voltage | 5.0 | 1.2 | 0.8 | | | V | (Notes 2, 4) |

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** $I_{CC}$ for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

**Note 2:** Worst case package.

**Note 3:** Max number of Data Inputs defined as (n). n − 1 Data Inputs are driven 0V to 5V. One Data Input @ $V_{IN}$ = GND.

**Note 4:** Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 5V ('ACTQ). Input-under-test switching: 5V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Waveforms

| Symbol | Parameter | $V_{CC}$* (V) | 74ACTQ $T_A = +25°C$, $C_L = 50$ pF | | | 54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF | | 74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation Delay $S_n$ to $Z_n$ | 5.0 | 3.0 | 7.0 | 11.5 | | | 2.0 | 13.5 | ns | 2-3, 4 |
| $t_{PHL}$ | Propagation Delay $S_n$ to $Z_n$ | 5.0 | 3.0 | 7.0 | 11.5 | | | 2.5 | 13.5 | ns | 2-3, 4 |
| $t_{PLH}$ | Propagation Delay $\overline{E}_n$ to $Z_n$ | 5.0 | 2.0 | 6.5 | 10.5 | | | 2.0 | 12.5 | ns | 2-3, 4 |
| $t_{PHL}$ | Propagation Delay $\overline{E}_n$ to $Z_n$ | 5.0 | 3.0 | 6.0 | 9.5 | | | 2.5 | 11.0 | ns | 2-3, 4 |
| $t_{PLH}$ | Propagation Delay $I_n$ to $Z_n$ | 5.0 | 2.5 | 5.5 | 9.5 | | | 2.0 | 11.0 | ns | 2-3, 4 |
| $t_{PHL}$ | Propagation Delay $I_n$ to $Z_n$ | 5.0 | 2.0 | 5.5 | 9.5 | | | 2.0 | 11.0 | ns | 2-3, 4 |

*Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0V |
| $C_{PD}$ | Power Dissipation Capacitance | 65.0 | pF | $V_{CC}$ = 5.0V |