

# 54ACTQ841

*54ACTQ841 Quiet Series 10-Bit Transparent Latch with TRI-STATE Outputs*



Literature Number: SNOS070

# 54ACTQ841

## Quiet Series 10-Bit Transparent Latch with TRI-STATE® Outputs

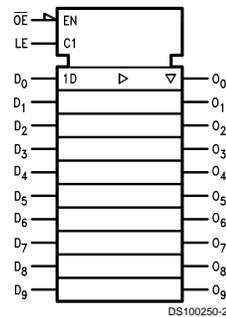
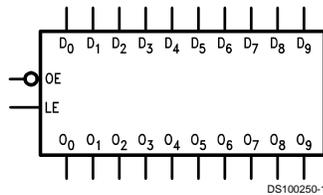
### General Description

The 'ACTQ841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The '841 is a 10-bit transparent latch, a 10-bit version of the '373. The 'ACTQ841 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

### Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Improved latch-up immunity
- Outputs source/sink 24 mA
- 'ACTQ841 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD) 5962-92200

### Logic Symbols

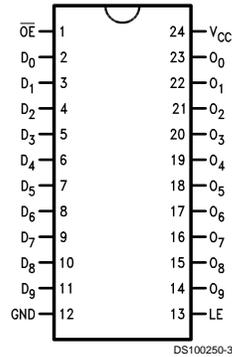


Pin Names	Description
D <sub>0</sub> -D <sub>9</sub>	Data Inputs
O <sub>0</sub> -O <sub>9</sub>	TRI-STATE Outputs
OE	Output Enable
LE	Latch Enable

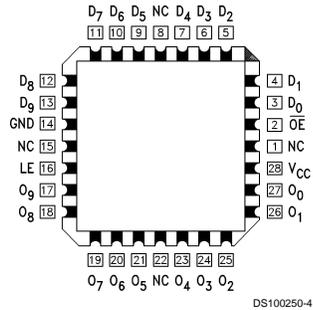
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## Connection Diagrams

Pin Assignment  
for DIP and Flatpack



Pin Assignment  
for LCC



## Functional Description

The 'ACTQ841 consists of ten D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

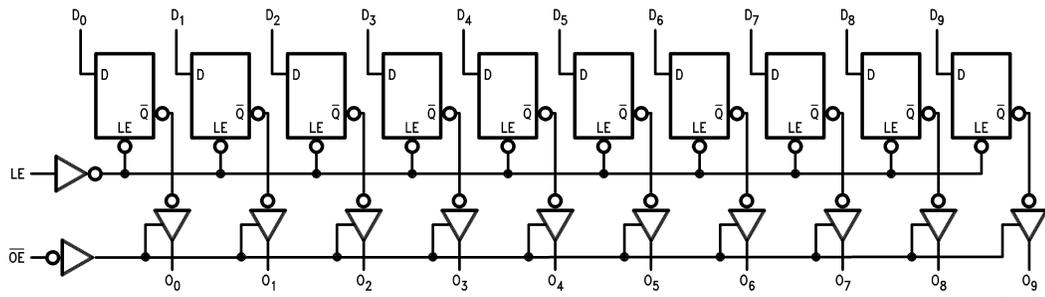
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state.

## Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
X	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance  
NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C

DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature ( $T_J$ )	
CDIP	175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'ACTQ	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54ACTQ	-55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

## DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54ACTQ	Units	Conditions
			$T_A =$ -55°C to +125°C		
			Guaranteed Limits		
$V_{IH}$	Minimum High Level Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
$V_{IL}$	Maximum Low Level Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8		
$V_{OH}$	Minimum High Level Output Voltage	4.5	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.4		
		4.5	3.70	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 mA$ $I_{OH} = -24 mA$
		5.5	4.70		
$V_{OL}$	Maximum Low Level Output Voltage	4.5	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.50	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = -24 mA$ $I_{OL} = -24 mA$
		5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, GND$
$I_{OZ}$	Maximum TRI-STATE Leakage Current	5.5	±10.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$
$I_{CCT}$	Maximum $I_{CC}/Input$	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$

## DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	54ACTQ		Units	Conditions
			T <sub>A</sub> = -55°C to +125°C			
			Guaranteed Limits			
I <sub>OLD</sub>	Minimum Dynamic Output Current (Note 4)	5.5	50		mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>		5.5	-50		mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	160.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 5)
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.5		V	(Note 6)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-1.2		V	(Note 6)

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:** I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

**Note 6:** Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 7)	54ACTQ		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
t <sub>PLH</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	5.0	2.0	9.5	ns	Figure 4
t <sub>PHL</sub>			2.0	11.0		
t <sub>PLH</sub>	Propagation Delay LE to O <sub>n</sub>	5.0	2.0	11.0	ns	Figure 4
t <sub>PHL</sub>			2.0	11.0		
t <sub>PZH</sub>	Output Enable Time $\overline{OE}$ to O <sub>n</sub>	5.0	1.5	11.0	ns	Figure 5
t <sub>PZL</sub>			1.5	13.0		
t <sub>PHZ</sub>	Output Disable Time $\overline{OE}$ to O <sub>n</sub>	5.0	1.5	8.5	ns	Figure 5
t <sub>PLZ</sub>			1.5	5.5		

**Note 7:** Voltage Range 5.0 is 5.0V ±0.5V.

**Note 8:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design. Not tested.

## AC Operating Requirements

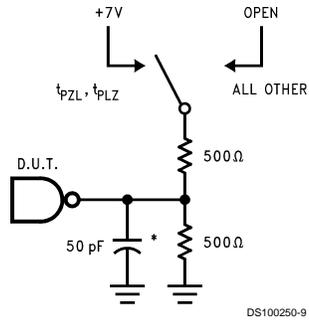
Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	54ACTQ		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Guaranteed Minimum			
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to LE	5.0	3.0		ns	Figure 7
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to LE	5.0	1.5		ns	Figure 7
t <sub>W</sub>	LE Pulse Width, HIGH	5.0	4.0		ns	Figure 6

**Note 9:** Voltage Range 5.0 is 5.0V ±0.5V.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = OPEN$
$C_{PD}$	Power Dissipation Capacitance	85.0	pF	$V_{CC} = 5.0V$

## AC Loading



\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

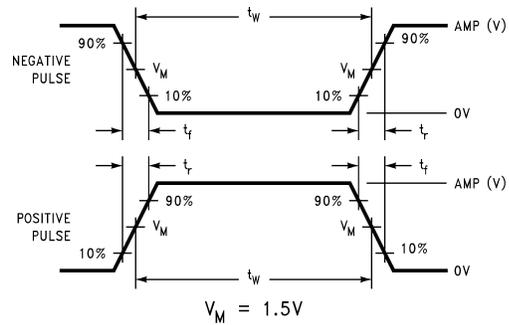


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

## AC Waveforms

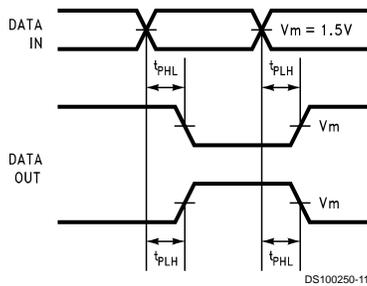


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

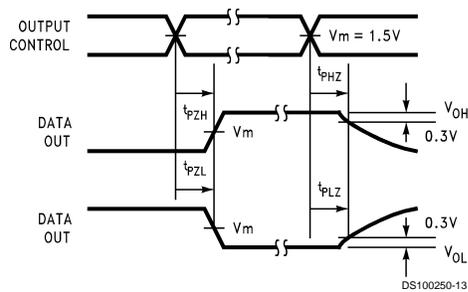
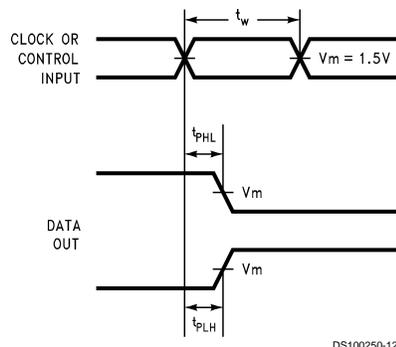
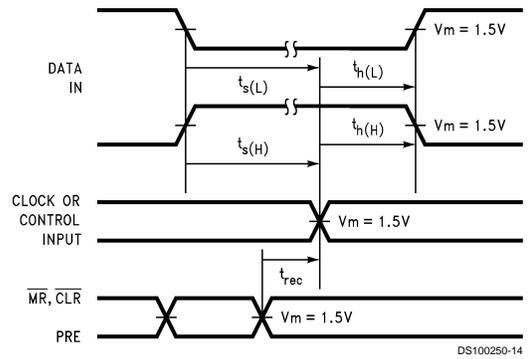


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Time

**AC Waveforms** (Continued)

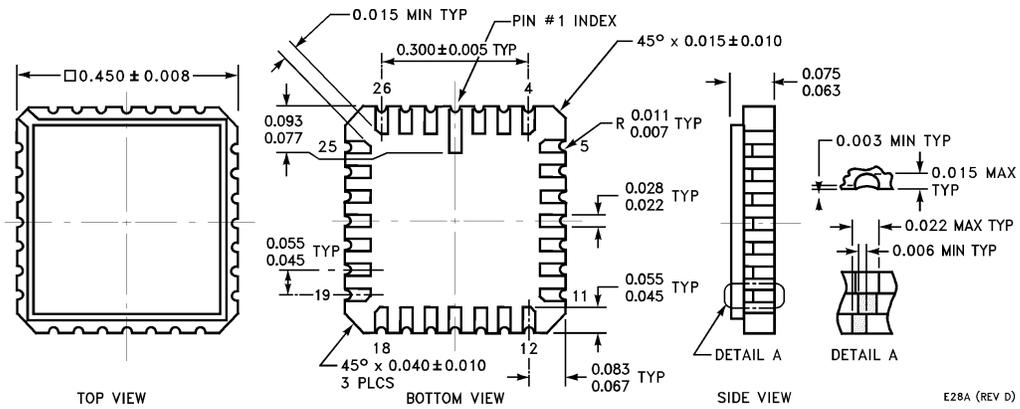


**FIGURE 6. Propagation Delay, Pulse Width Waveforms**

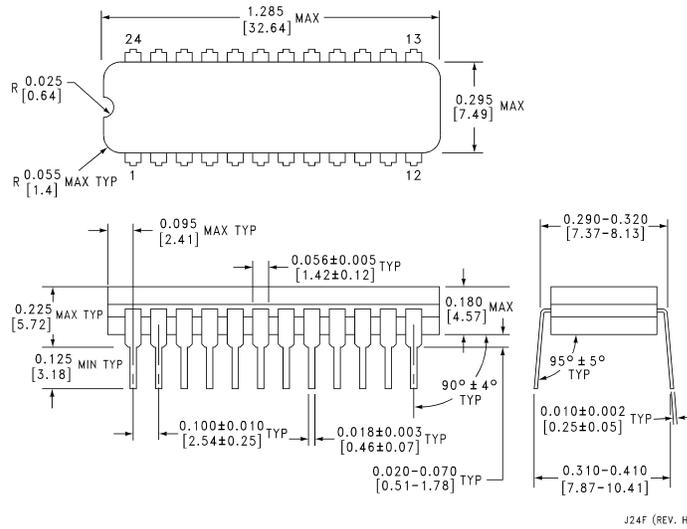


**FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms**

**Physical Dimensions** inches (millimeters) unless otherwise noted

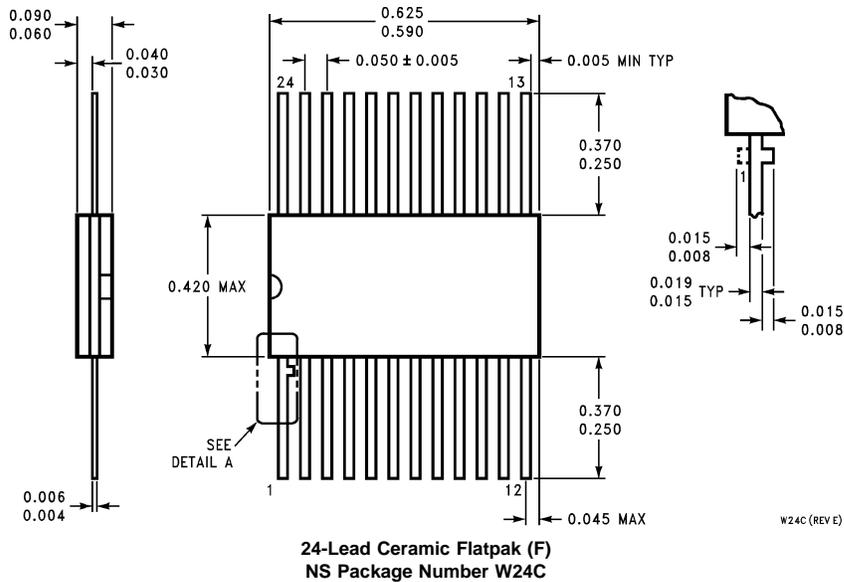


**28-Terminal Ceramic Leadless Chip Carrier (L)  
NS Package Number E28A**



**24-Lead Slim (0.300" Wide) Ceramic Dual-In-Line Package (SD)  
NS Package Number J24F**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



W24C (REV E)

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