National Semiconductor

54FCT/74FCT273
Octal D Flip-Flop

General Description

The 'FCT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

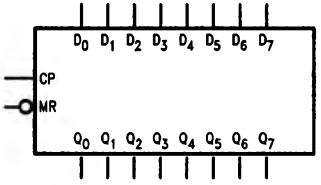
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- TTL input and output level compatible
- TTL levels accept CMOS levels
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- NSC 54/74FCT273 is pin and functionally equivalent to IDT 54/74FCT273

Ordering Code: See Section 8

Logic Symbols



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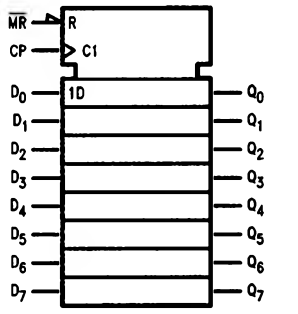
IEEE/IEC



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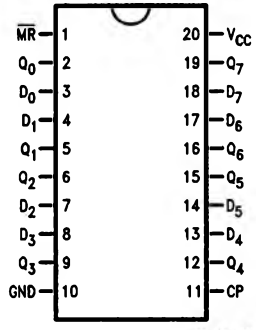
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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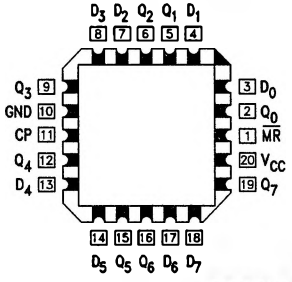
Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

Pin Assignment for LCC



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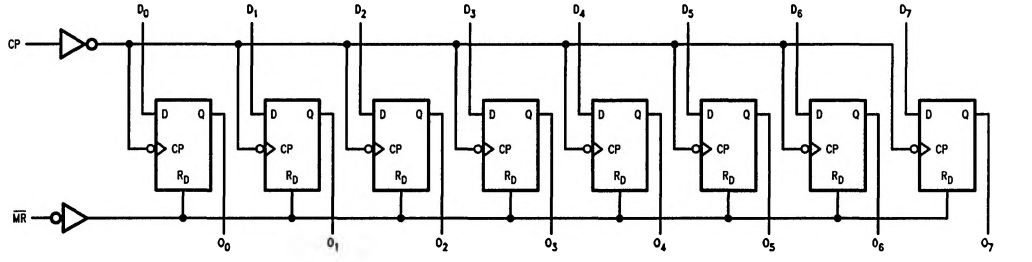
Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5 to +7.0V
- 74FCT: −0.5 to +7.0V

Temperature Under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75 to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	V_I = V_{CC} V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	54FCT/74FCT			Units	Conditions	
		Min	Typ	Max			
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min	I_{OL} = 300 μA
			0.3	0.5		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA (Mil)
			0.3	0.5			I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max V_{IN} ≥ V_{HC}, V_{IN} ≤ 0.2V f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	V_{CC} Max Outputs Open $\overline{MR}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} ≥ V_{HC} V_{IN} ≤ 0.2V V_{IN} ≤ 0.2V
V_H	Input Hysteresis on Clock Only		200		mV		
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open $\overline{MR}$ = V_{CC}	V_{IN} ≥ V_{CC} V_{IN} ≤ 0.2V
			1.8	6.0		f_I = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open $\overline{MR}$ = V_{CC}	V_{IN} ≥ V_{HC} V_{IN} ≤ 0.2V
			5.0	16.8		f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Curent for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		$T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$			
		Typ	Min	Max	Min	Max		
t_{PHL} t_{PLH}	Propagation Delay Clock to Output	7.0	2.0	13.0			ns	2-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output	8.0	2.0	13.0			ns	2-8
t_{SU}	Setup Time HIGH or LOW Data to CP	3.0	3.0				ns	2-10
t_h	Hold Time HIGH or LOW Data to CP	1.0	2.0				ns	2-10
t_w	Clock Pulse Width HIGH or LOW	4.0	7.0				ns	2-9
t_w	$\overline{MR}$ Pulse Width HIGH or LOW	4.0	7.0				ns	2-9
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.0	4.0				ns	2-10

Note 1: Minimum limits are guaranteed but not tested on Propagation Delays.

Capacitance $T_A = 25°C, f = 1.0\ MHz$

Symbol	Parameter	Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

Note: This parameter is guaranteed by characterization data and not tested.