National Semiconductor

54FCT/74FCT899A
9-Bit Latchable Transceiver with Parity Generator/Checker

General Description

The 'FCT899A is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. It has a guaranteed current sinking capability of 24 mA at the A-bus and 64 mA at the B-bus.

The 'FCT899A features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

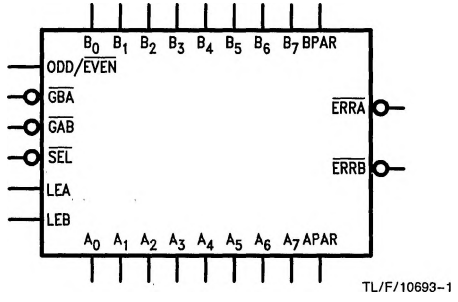
FACT FCTA features undershoot correction and split ground bus for superior performance.

Features

- Latchable transceiver with output sink of 24 mA at the A-bus and 64 mA at the B-bus
- Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- Independent latch enables for A-to-B and B-to-A directions
- Select pin for ODD/$\overline{\text{EVEN}}$ parity
- $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ output pins for parity checking
- Ability to simultaneously generate and check parity
- CMOS power levels
- Guaranteed 4000V min ESD protection

Ordering Code: See Section 8

Logic Symbol



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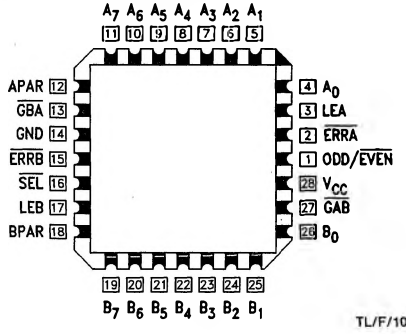
Connection Diagram

Pin Assignment for PCC



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Pin Names	Description
A_0–A_7	A Bus Data Inputs/Data Outputs
B_0–B_7	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs
ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ Parity Select, Active LOW for EVEN Parity
$\overline{\text{GBA}}$, $\overline{\text{GAB}}$	Output Enables for A or B Bus, Active LOW
$\overline{\text{SEL}}$	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

Functional Description

The 'FCT899A has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

— Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select ($\overline{\text{SEL}}$) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by $\overline{\text{ERRB}}$ ($\overline{\text{ERRA}}$).

— Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is HIGH. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).

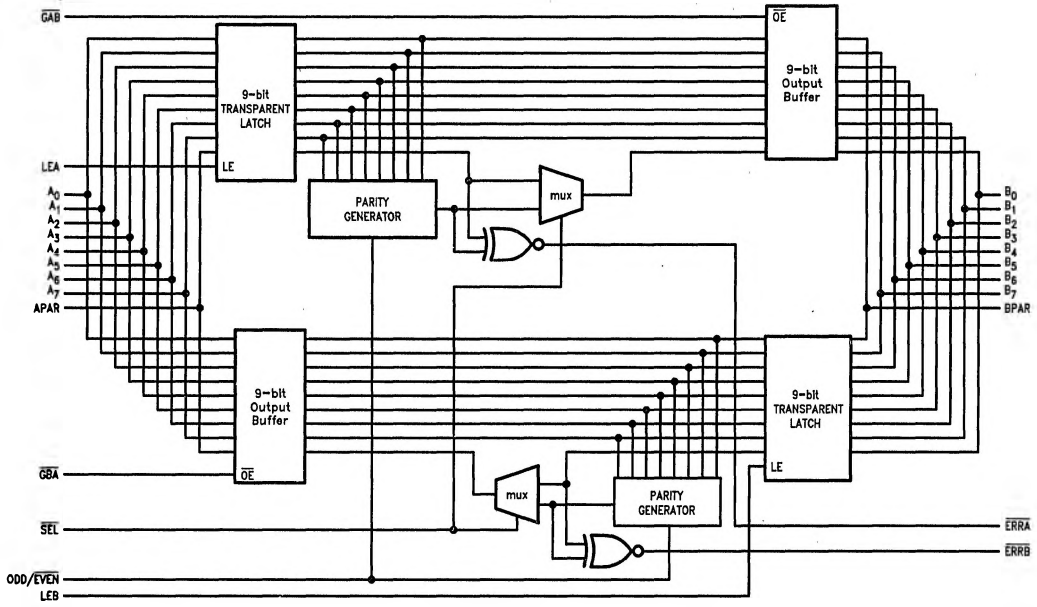
— Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table below).

Function Table

Inputs					Operation
$\overline{\text{GAB}}$	$\overline{\text{GBA}}$	$\overline{\text{SEL}}$	LEA	LEB	
H	H	X	X	X	Busses A and B are TRI-STATE®.
H	L	L	L	H	Generates parity from B[0:7] based on O/$\overline{\text{E}}$ (Note 1). Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	L	H	H	Generates parity from B[0:7] based on O/$\overline{\text{E}}$. Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
H	L	L	X	L	Generates parity from B latch data based on O/$\overline{\text{E}}$. Generated parity → APAR. Generated parity checked against latched BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	X	H	BPAR/B[0:7] → APAR/A0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	H	H	BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
L	H	L	H	L	Generates parity for A[0:7] based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	L	H	H	Generates parity from A[0:7] based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.
L	H	L	L	X	Generates parity from A latch data based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against latched APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	L	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	H	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Note 1: O/$\overline{\text{E}}$ = ODD/$\overline{\text{EVEN}}$

Functional Block Diagram



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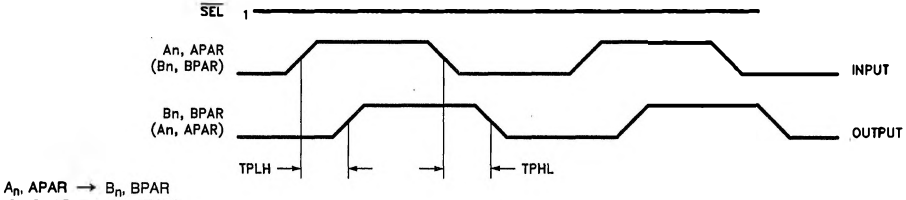
AC Path



A_n, APAR → B_n, BPAR
(B_n, BPAR → A_n, APAR)

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FIGURE 1

AC Path (Continued)

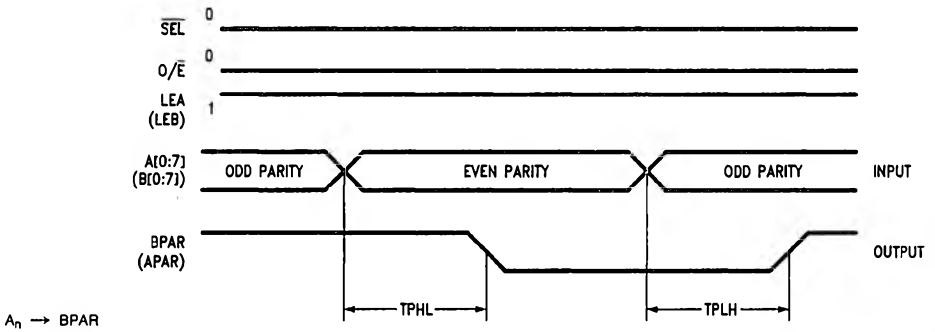


FIGURE 2

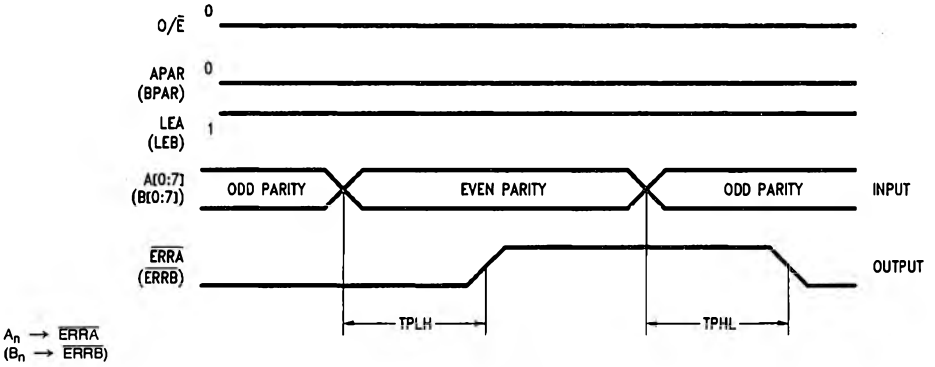


FIGURE 3

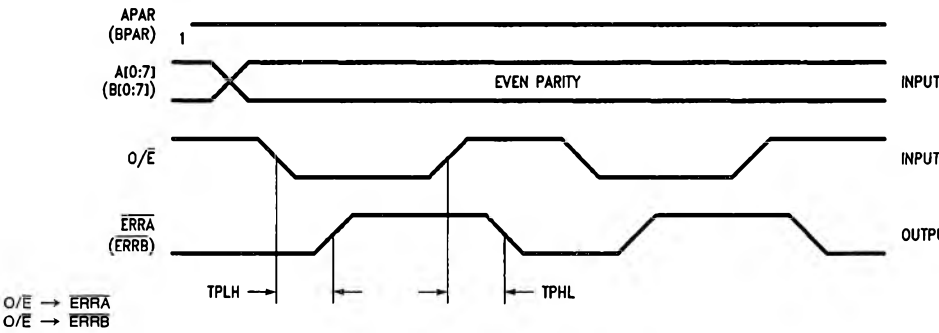


FIGURE 4

AC Path (Continued)

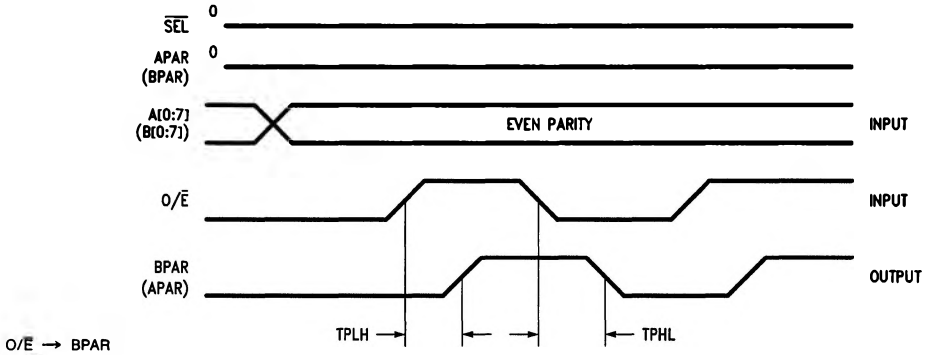


FIGURE 5

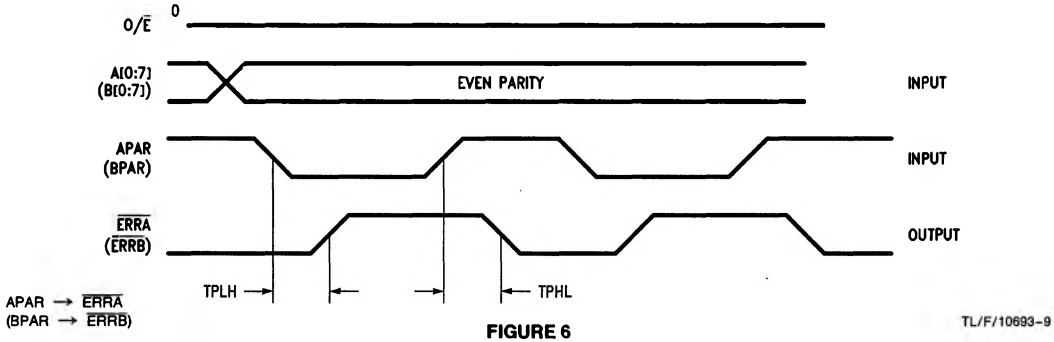


FIGURE 6

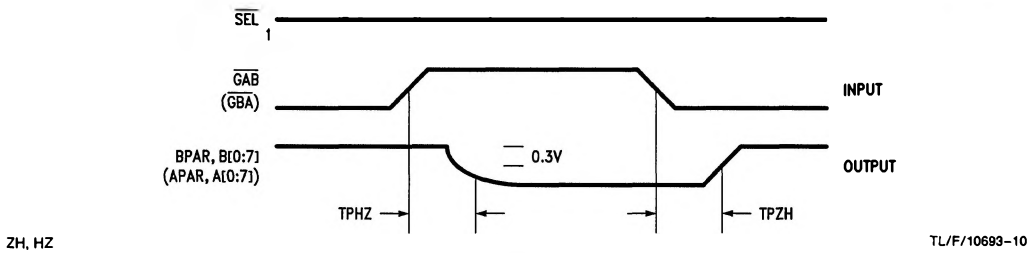
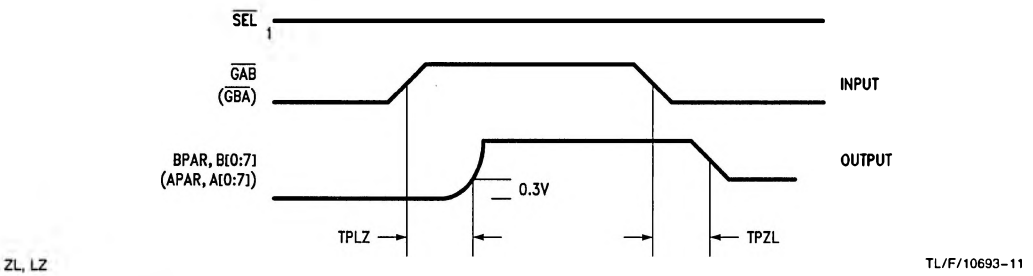


FIGURE 7

AC Path (Continued)



ZL, LZ

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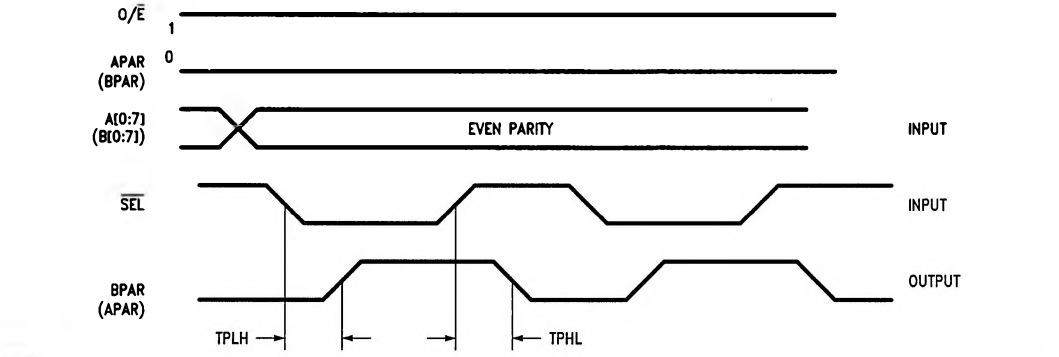
FIGURE 8



SEL → BPAR
(SEL → APAR)

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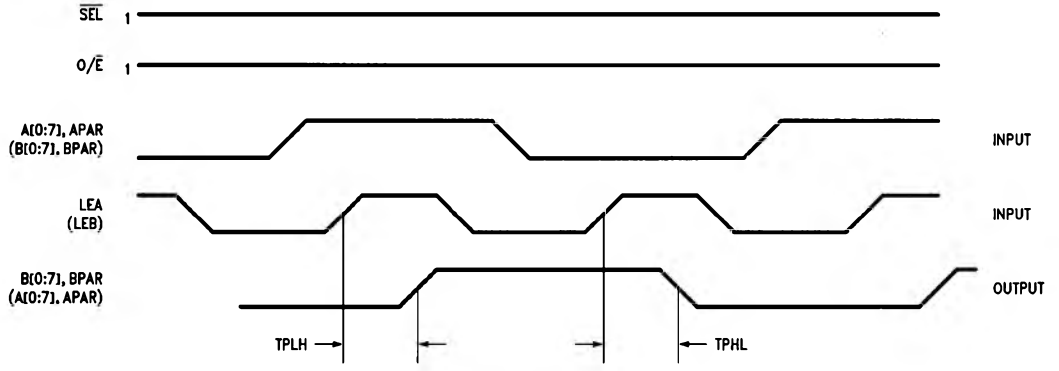
FIGURE 9



LEA → BPAR, B[0:7]
(LEB → APAR, A[0:7])

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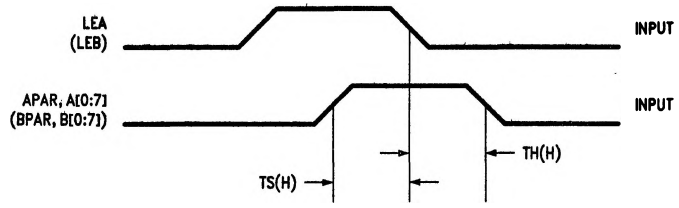
FIGURE 10

AC Path (Continued)



TS(H), TH(H)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

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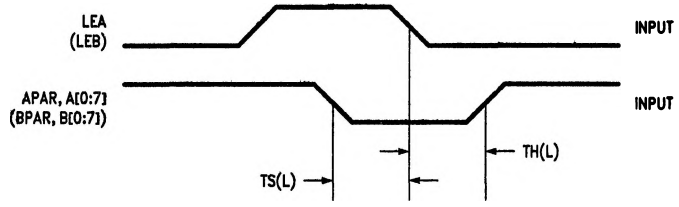
FIGURE 11



TS(L), TH(L)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

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FIGURE 12

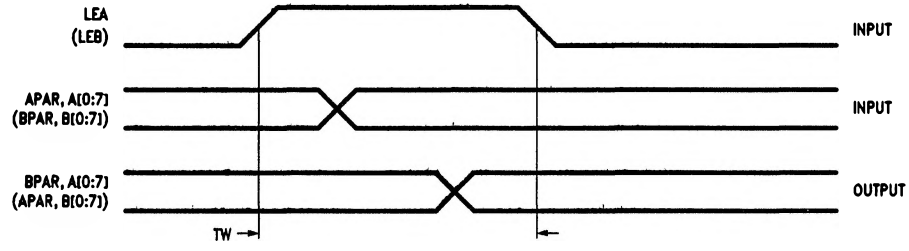

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FIGURE 13

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to +7.0V
- 74FCTA: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} 5.0V ±10% T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCTA/74FCTA Min	54FCTA/74FCTA Typ	54FCTA/74FCTA Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2) V_I = 0.5V (Note 2) V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8 V_{HC} 2.4 2.4	3.0 V_{CC} 4.3 4.3		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND GND 0.3 0.3	0.2 0.2 0.55 0.55	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ $f_I = 0$	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C, V_{HC} = V_{CC} −0.2V (Continued)

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	V_{CC} = Max Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq$ 0.2V
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open f_i = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq$ 0.2V
			1.8	5.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	6.5		(Note 5) V_{CC} = Max Outputs Open f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq$ 0.2V
			5.0	14.5			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All Currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50$ pF		$T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50$ pF			
		Typ	Min	Max	Min	Max		
t_{PHL} t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	10.0	2.5	11.0			ns	1
t_{PHL} t_{PLH}	Propagation Delay APAR to BPAR or BPAR to APAR	11.0	1.5	8.0			ns	1
t_{PHL} t_{PLH}	Propagation Delay A to BPAR or B to APAR $\overline{SEL} = 0$	13.0	2.5	11.5			ns	2
t_{PHL} t_{PLH}	Propagation Delay A to $\overline{ERRA}$ or B to $\overline{ERRB}$	13.0	2.0	11.0			ns	3
t_{PHL} t_{PLH}	Propagation Delay ODD/$\overline{EVEN}$ to ERRA, ERRB or APAR, BPAR	13.0	2.0	11.0			ns	4, 5
t_{PHL} t_{PLH}	Propagation Delay $\overline{SEL}$ to APAR or BPAR	10.5	1.5	8.5			ns	9
t_{PHL} t_{PLH}	Propagation Delay LEA/LEB to B/A or BPAR/APAR	11.0	2.0	11.0			ns	10, 11
t_{PZL} t_{PZH}	Output Enable Delay	9.5	1.5	10.0			ns	7, 8
t_{PHZ} t_{PLZ}	Output Disable Enable	11.0	1.5	8.5			ns	7, 8
t_{SET}	Setup Time A to LEA or B to LEB	3.0	3.0				ns	11, 12
t_{HOLD}	Hold Time A to LEA, B to LEB	1.5	1.5				ns	11, 12
t_W	Pulse Width LEA or LEB	5.0	4.0				ns	13