National Semiconductor

54LS160A/DM74LS160A, 54LS162A/DM74LS162A Synchronous Presettable BCD Decade Counters

General Description

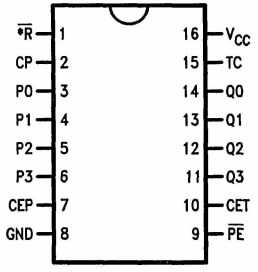
The 'LS160 and 'LS162 are high speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'LS160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'LS162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

Features

- Synchronous counting and loading
- High speed synchronous expansion
- Typical count rate of 35 MHz
- Fully edge triggered

Connection Diagram

Dual-In-Line Package



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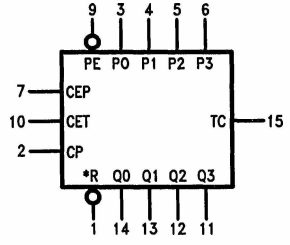
*$\overline{MR}$ for 'LS160
*$\overline{SR}$ for 'LS162

Order Number 54LS160ADMQB, 54LS160AFMQB, 54LS160ALMQB, 54LS162ADMQB, 54LS162AFMQB, 54LS162ALMQB, DM74LS160AM, DM74LS160AN, DM74LS162AM or DM74LS162AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('160)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('162)	Synchronous Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q0–Q3	Flip-Flop Outputs
TC	Terminal Count Output

Logic Symbol



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V_{CC} = Pin 16 *$\overline{MR}$ for 'LS160
GND = Pin 8 *$\overline{SR}$ for 'LS162

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS160A/162A			DM74LS160A/162A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	20 20			20 20			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	0.0 0.0			0.0 0.0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	20 20			20 20			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0			0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW CEP, CET or $\overline{SR}$ to CP	20 20			20 20			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CEP, CET or $\overline{SR}$ to CP	0 0			0 0			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width, HIGH or LOW	15 25			15 25			ns
$t_w(L)$	$\overline{MR}$ Pulse Width LOW ('160)	15			15			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP ('160)	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V Inputs $\overline{PE}$, CET Inputs				0.1 0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V Inputs $\overline{PE}$, CET Inputs				20 40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V Inputs	54LS			−0.4	mA
			DM74			−1.6	
		$\overline{PE}$, CET Inputs				−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max, $\overline{PE}$ = GND CP = ⎍, Other Inputs = 4.5V				31	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max, V_{IN} = GND CP = ⎍				31	mA

Switching Characteristics V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	R_L = 2 kΩ C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	25		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to TC		25 21	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		20 27	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		24 27	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC		14 14	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('160)		28	ns

Functional Description

The 'LS160 and 'LS162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The '161 and '163 count modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'LS160) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('LS160), synchronous reset ('LS162), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, 'LS160), Synchronous Reset ($\overline{SR}$, 'LS162), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('LS160) or $\overline{SR}$ ('LS162) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'LS160A and 'LS162A use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Functional Description (Continued)

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in the 9310 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the decade counters of the 'LS160, 'LS162, the TC output is fully decoded and can only be HIGH in state 9.

LOGIC EQUATIONS:

Count Enable = CEP • CET • PE

TC = Q0 • $\overline{Q1}$ • $\overline{Q2}$ • Q3 • CET

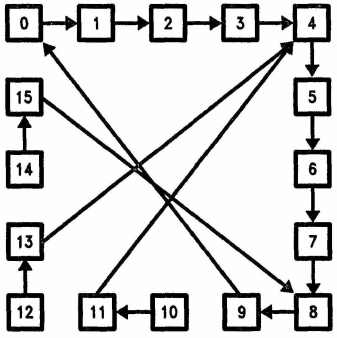
Mode Select Table

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the 'LS162
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagrams

'LS160, 'LS162



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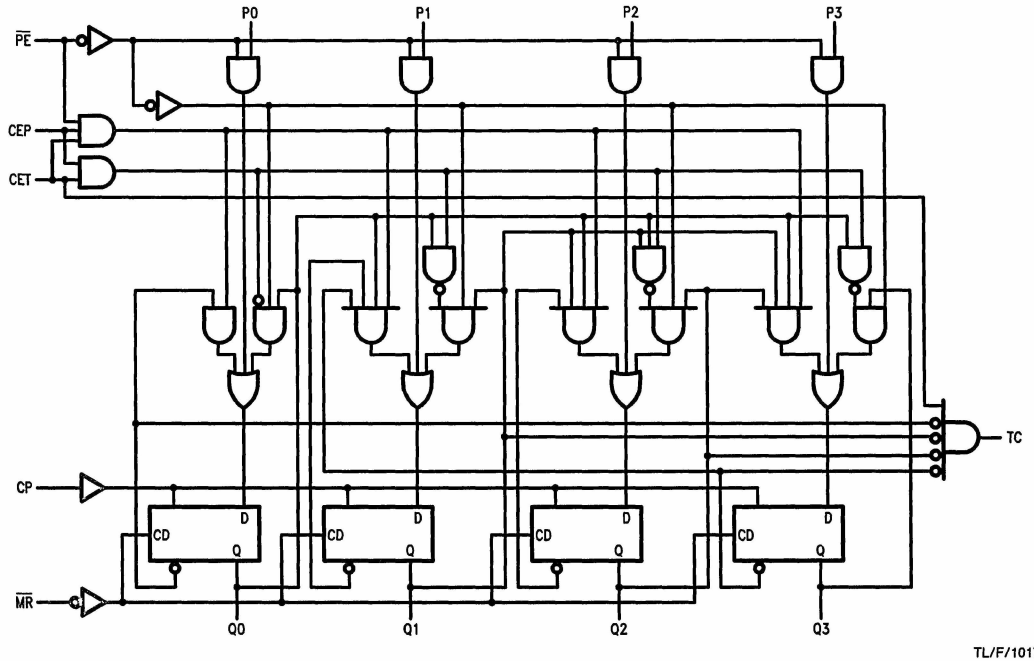
Logic Diagrams

'LS160



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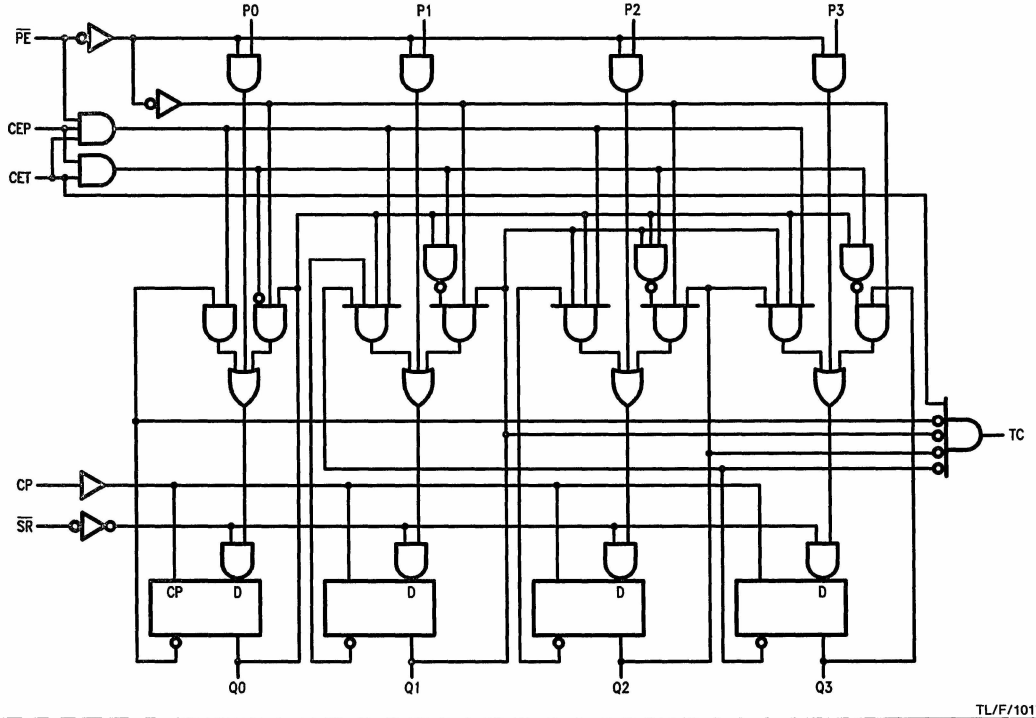
'LS162



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