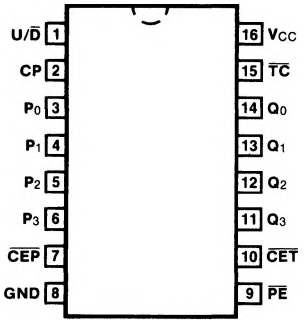
54LS/74LS168

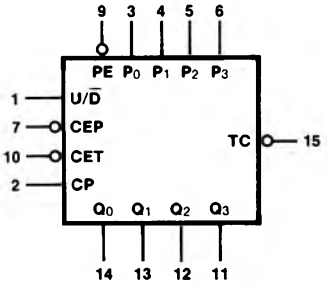
SYNCHRONOUS BI-DIRECTIONAL BCD DECADE COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '168 is a fully synchronous 4-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. It counts in the BCD (8421) sequence and all state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS168PC		9B
Ceramic DIP (D)	A	74LS168DC	54LS168DM	6B
Flatpak (F)	A	74LS168FC	54LS168FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.25
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/0.5
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	0.5/0.25
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.25
U/$\overline{D}$	Up-Down Count Control Input	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	10/5.0 (2.5)
$\overline{TC}$	Terminal Count Output (Active LOW)	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '168 and '169 use edge-triggered D-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the $P_0 - P_3$ inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH. The U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 9 (15 for the '169) in the COUNT UP mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the '168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the '168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

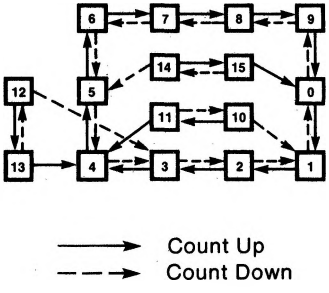
1) Count Enable = $\overline{CEP} \bullet \overline{CET} \bullet \overline{PE}$
2) Up: $\overline{TC} = Q_0 \bullet Q_3 \bullet (U/\overline{D}) \bullet \overline{CET}$
3) Down: $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (U/\overline{D}) \bullet \overline{CET}$

'168 and '169 MODE SELECT TABLE

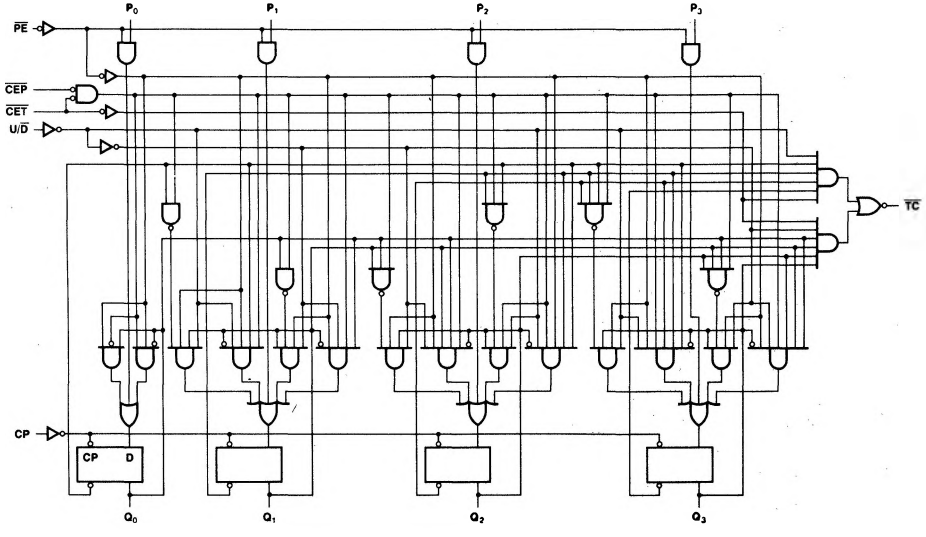
$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (increment)
H	L	L	L	Count Down (decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM
54LS/74LS168



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		34	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		20 20	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$		30 30	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$		15 20	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$		25 25	ns	Figs. 3-1, 3-20

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n, $\overline{CEP}$ or $\overline{CET}$ to CP	15 15		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n, $\overline{CEP}$ or $\overline{CET}$ to CP	5.0 5.0		ns	Fig. 3-6
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP	20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{PE}$ to CP	0 0		ns	Fig. 3-6
t_s (H) t_s (L)	Setup Time HIGH or LOW U/$\overline{D}$ to CP	25 25		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW U/$\overline{D}$ to CP	0 0		ns	Fig. 3-6
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	10 20		ns	Fig. 3-8