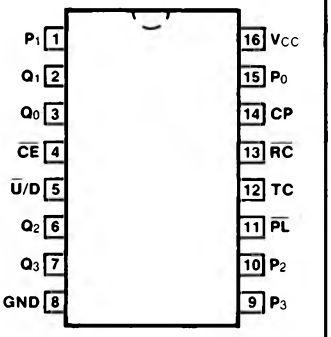
54/74190
54LS/74LS190

UP/DOWN DECADE COUNTER
(With Preset and Ripple Clock)

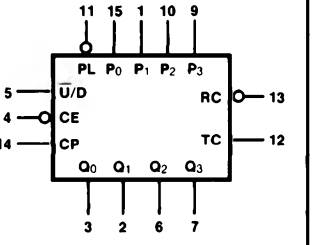
DESCRIPTION — The '190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the '190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multi-stage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- **HIGH SPEED — 30 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **CASCADABLE**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

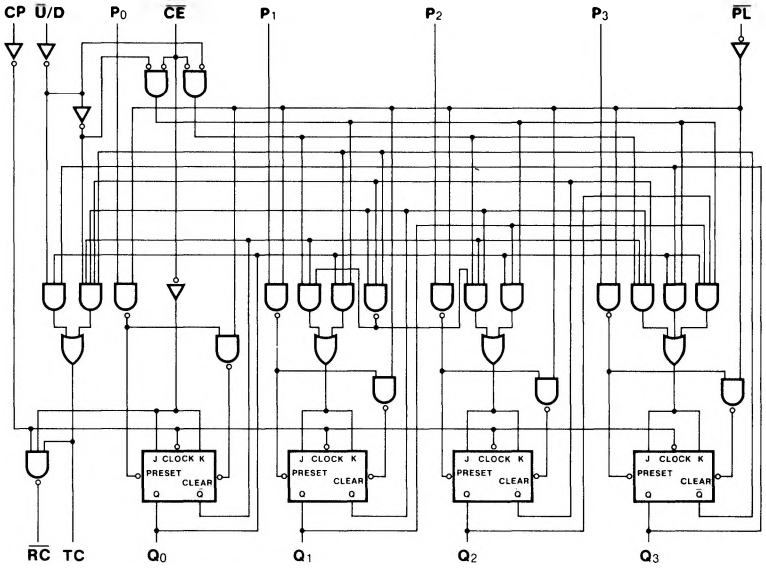
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74190PC, 74LS190PC		9B
Ceramic DIP (D)	A	74190DC, 74LS190DC	54190DM, 54LS190DM	7B
Flatpak (F)	A	74190FC, 74LS190FC	54190FM, 54LS190FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CE}$	Count Enable Input (Active LOW)	3.0/3.0	1.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{U}/D$	Up/Down Count Control Input	1.0/1.0	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	20/10	10/5.0 (2.5)
$\overline{RC}$	Ripple Clock Output (Active LOW)	20/10	10/5.0 (2.5)
TC	Terminal Count Output (Active HIGH)	20/10	10/5.0 (2.5)

LOGIC DIAGRAM



MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

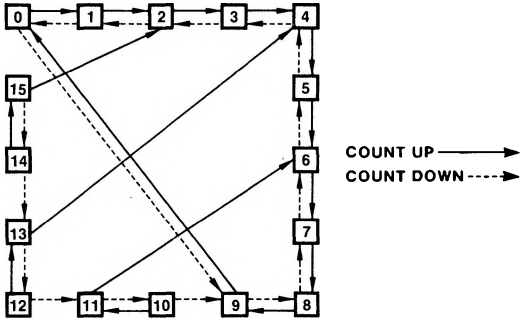
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

RC TRUTH TABLE

INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⎍	⎍
H	X	X	H
X	L	X	H

*TC is generated internally

STATE DIAGRAM



FUNCTIONAL DESCRIPTION — The '190 is a synchronous up/down BCD decade counter and the '191 is a synchronous up/down 4-bit binary counter. The operating modes of the '190 decade counter and the '191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs ($P_0 - P_3$) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. When counting is to be enabled, the $\overline{CE}$ signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH $\overline{CE}$ transition must occur only while the clock is HIGH. Similarly, the $\overline{U}$/D signal should only be changed when either $\overline{CE}$ or the clock is HIGH. These restrictions do not apply to the 'LS190 and 'LS191; $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the '190, 15 for the '191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in *Figures a and b*. In *Figure a*, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages in shown in *Figure b*. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in *Figure c* avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of *Figures a and b* doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

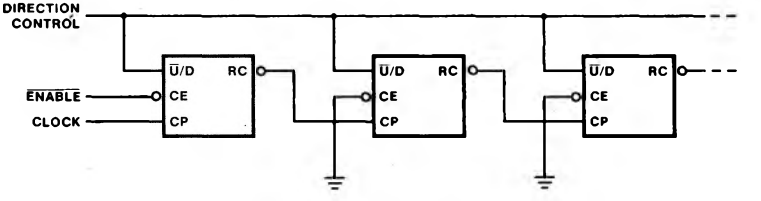


Fig. a N-Stage Counter Using Ripple Clock

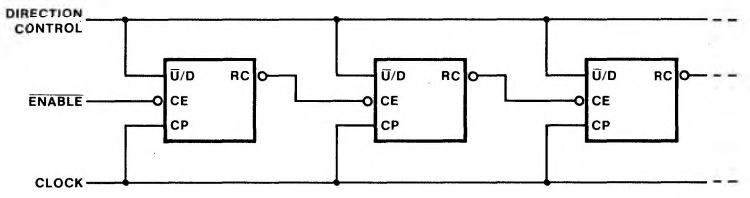


Fig. b Synchronous N-Stage Counter Using Ripple Carry/Borrow

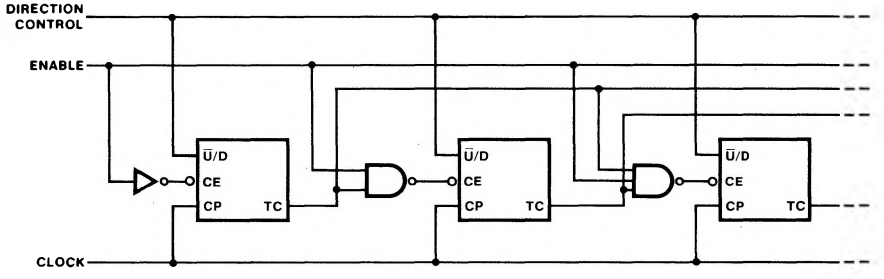


Fig. c Synchronous N-Stage Counter with Parallel Gated Carry/Borrow

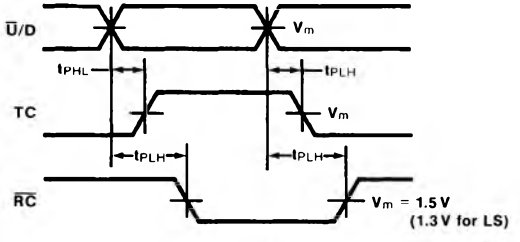


Fig. d

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		99		35	mA	V_{CC} = Max All Inputs = Gnd
		XC		105		35		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency	20		20		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		24 36		24 36	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to TC		42 52		42 52	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		20 24		20 24	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		22 50		22 50	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		33 33		33 33	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		33 50		33 50	ns	Figs. 3-1, 3-16
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$		45 45		45 45	ns	Fig. 3-1, Fig. d
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{TC}$		33 33		33 33	ns	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n to $\overline{PL}$	20 20		20 20		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n to $\overline{PL}$	0 0		5.0 5.0		ns	
t_s (L)	Setup Time LOW $\overline{CE}$ to CP	20		20		ns	Fig. 3-6
t_h (L)	Hold Time LOW $\overline{CE}$ to CP	0		0		ns	
t_w (L)	CP Pulse Width LOW	25		20		ns	Fig. 3-8
t_w (L)	$\overline{PL}$ Pulse Width LOW	35		35		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{PL}$ to CP	20		20		ns	Fig. 3-16