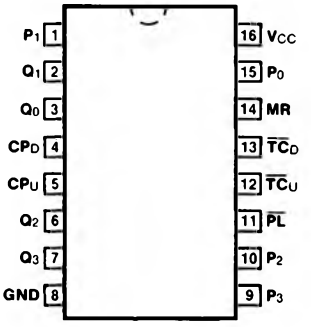
54/74192
54LS/74LS192

UP/DOWN DECADE COUNTER
(With Separate Up/Down Clocks)

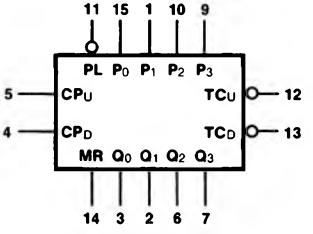
DESCRIPTION — The '192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74192PC, 74LS192PC		9B
Ceramic DIP (D)	A	74192DC, 74LS192DC	54192DM, 54LS192DM	6B
Flatpak (F)	A	74192FC, 74LS192FC	54192FM, 54LS192FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CP_U	Count Up Clock Input (Active Rising Edge)	1.0/1.0	0.5/0.25
CP_D	Count Down Clock Input (Active Rising Edge)	1.0/1.0	0.5/0.25
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	20/10	10/5.0 (2.5)
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)	20/10	10/5.0 (2.5)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)	20/10	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '192 and '193 are asynchronously presettable decade and 4-bit binary synchronous up/down (reversible) counters. The operating modes of the '192 decade counter and the '193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagram. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

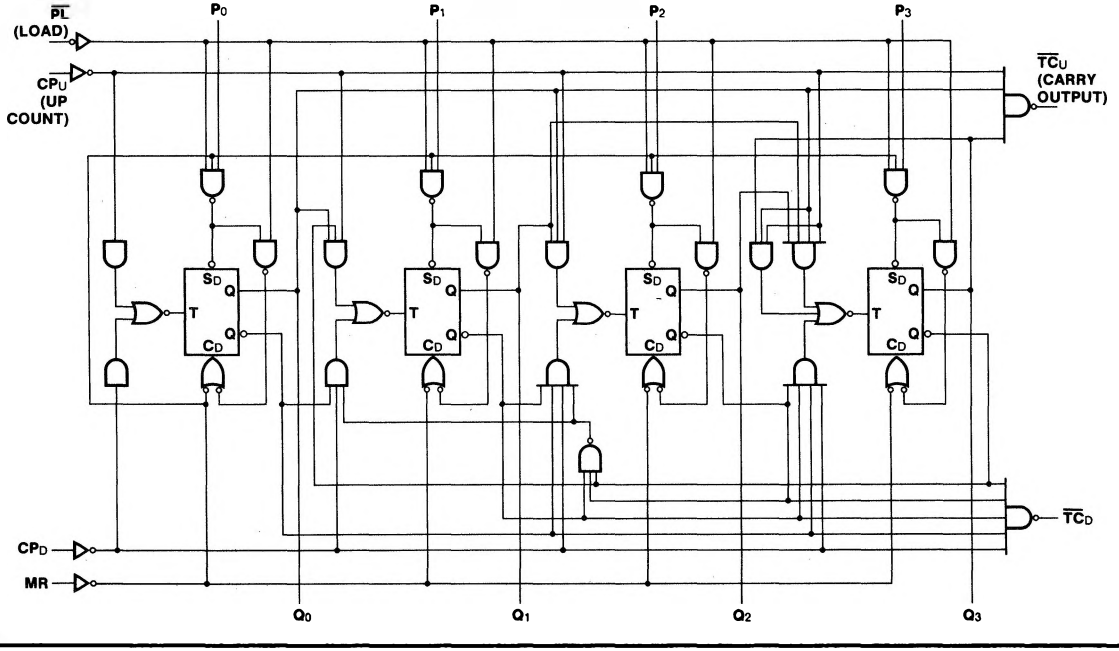
Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the '192, 15 for the '193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q_0 \bullet Q_3 \bullet \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$$

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0 — P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM

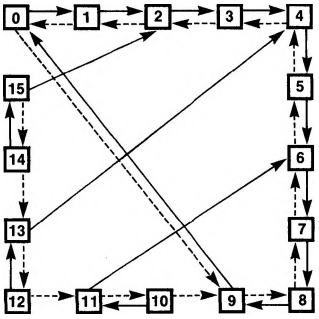


MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-65	-20	-100	mA	V_{CC} = Max
		XC	-18	-65	-20	-100		
I_{CC}	Power Supply Current	XM		89		34	mA	V_{CC} = Max; MR, $\overline{PL}$ = Gnd Other Inputs = 4.5 V
		XC		102		34		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency	25		30		MHz	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay CP_U or CP_D to Q_n		38		31	ns	
t_{PHL}			47		28		
t_{PLH}	Propagation Delay CP_U to $\overline{TC_U}$		26		16	ns	Figs. 3-1, 3-5
t_{PHL}			24		21		
t_{PLH}	Propagation Delay CP_D to $\overline{TC_D}$		24		16	ns	
t_{PHL}			24		24		
t_{PLH}	Propagation Delay P_n to Q_n				20	ns	Figs. 3-1, 3-5
t_{PHL}					30		
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n		40		32	ns	Figs. 3-1, 3-16
t_{PHL}			40		30		
t_{PHL}	Propagation Delay, MR to Q_n		35		25		

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n to $\overline{PL}$	20 20		20 10		ns	Fig. 3-13 CP_U = CP_D = LOW
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n to $\overline{PL}$	0 3.0		3.0 3.0			
t_w (L)	CP Pulse Width LOW	20		17		ns	Fig. 3-8
t_w (L)	$\overline{PL}$ Pulse Width LOW	20		20		ns	Fig. 3-16
t_w (H)	MR Pulse Width HIGH	20		15			
t_{rec}	Recovery Time, MR to CP	6.0		3.0			
t_{rec}	Recovery Time, $\overline{PL}$ to CP	6.0		10			