54LS/74LS299

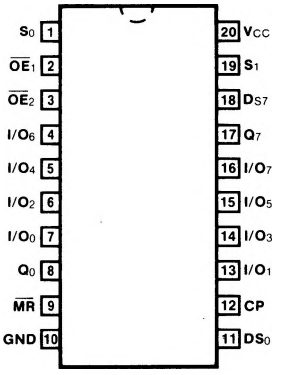
8-INPUT UNIVERSAL SHIFT/STORAGE REGISTER

(With Common Parallel I/O Pins)

DESCRIPTION — The '299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- **COMMON I/O FOR REDUCED PIN COUNT**
- **FOUR OPERATION MODES: SHIFT LEFT, SHIFT RIGHT, LOAD AND STORE**
- **SEPARATE SHIFT RIGHT SERIAL INPUT AND SHIFT LEFT SERIAL INPUT FOR EASY CASCADING**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**

CONNECTION DIAGRAM
PINOUT A



PRELIMINARY

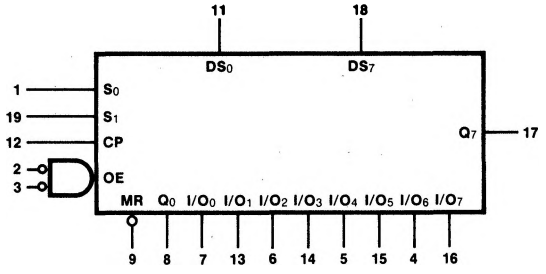
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS299PC		9Z
Ceramic DIP (D)	A	74LS299DC	54LS299DM	4E
Flatpak (F)	A	74LS299FC	54LS299FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
D_{S0}	Serial Data Input for Right Shift	0.5/0.25
D_{S7}	Serial Data Input for Left Shift	0.5/0.25
S_0, S_1	Mode Select Inputs	1.0/0.50
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.25
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)	0.5/0.25
I/O_0 — I/O_7	Parallel Data Inputs or	0.5/0.25
	3-State Parallel Outputs	65/15 (25)/(7.5)
Q_0, Q_7	Serial Outputs	10/5.0 (2.5)

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

FUNCTIONAL DESCRIPTION — The '299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by the S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

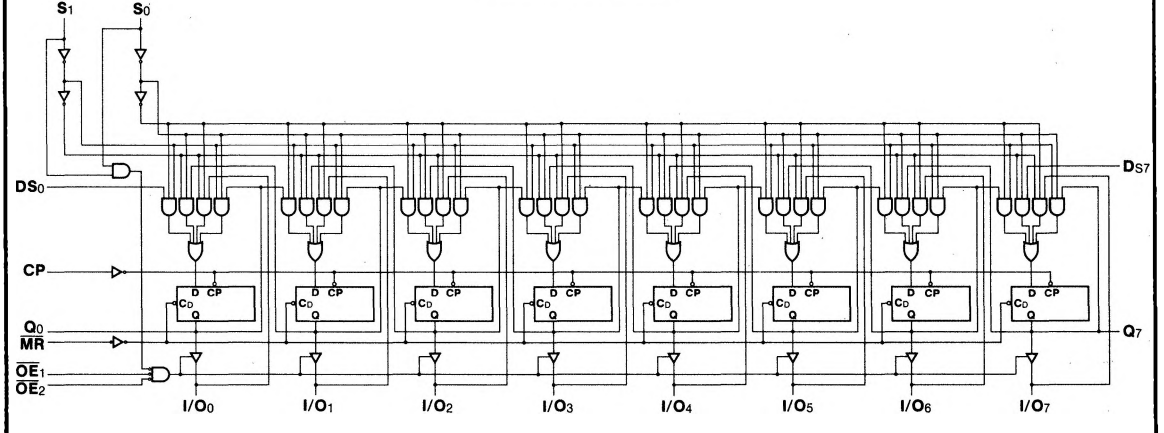
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; $Q_0 - Q_7$ = LOW
H	H	H	⎍	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⎍	Shift Right; $D_{S0} \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⎍	Shift Left; $D_{S7} \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		65	mA	V_{CC} = Max, $\overline{OE}$ = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		MIN	Max		
f_{max}	Maximum Input Frequency	35		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7		23 25	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		25 29	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		30	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		33	ns	
t_{PZH} t_{PZL}	Output Enable Time		18 23	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ
t_{PHZ} t_{PLZ}	Output Disable Time		15 15	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW S_0 or S_1 to CP	24 24		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW S_0 or S_1 to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW I/O_n, D_{S0}, D_{S7} to CP	10 10		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW I/O_n, D_{S0}, D_{S7} to CP	0 0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	15		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	10		ns	Fig. 3-16