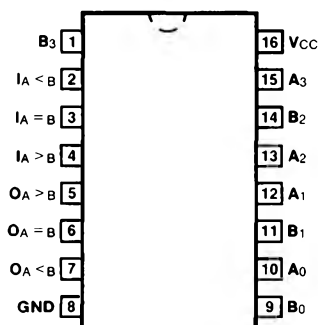


54/7485

54LS/74LS85

4-BIT MAGNITUDE COMPARATOR

CONNECTION DIAGRAM PINOUT A



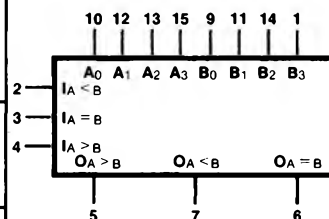
DESCRIPTION — The '85 is a high speed, expandable 4-bit magnitude comparator which compares two 4-bit words in any monotonic code (binary, BCD or other) and generates three outputs: A less than B, A greater than B, and A equal to B. Three expansion inputs allow serial (ripple) expansion over any word length without external gates.

- **EASILY EXPANDABLE**
- **BINARY OR BCD COMPARISON**
- **A > B, A < B, A = B OUTPUTS AVAILABLE**

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	7485PC, 74LS85PC		9B
Ceramic DIP (D)	A	7485DC, 74LS85DC	5485DM, 54LS85DM	6B
Flatpak (F)	A	7485FC, 74LS85FC	5485FM, 54LS85FM	4L

LOGIC SYMBOL



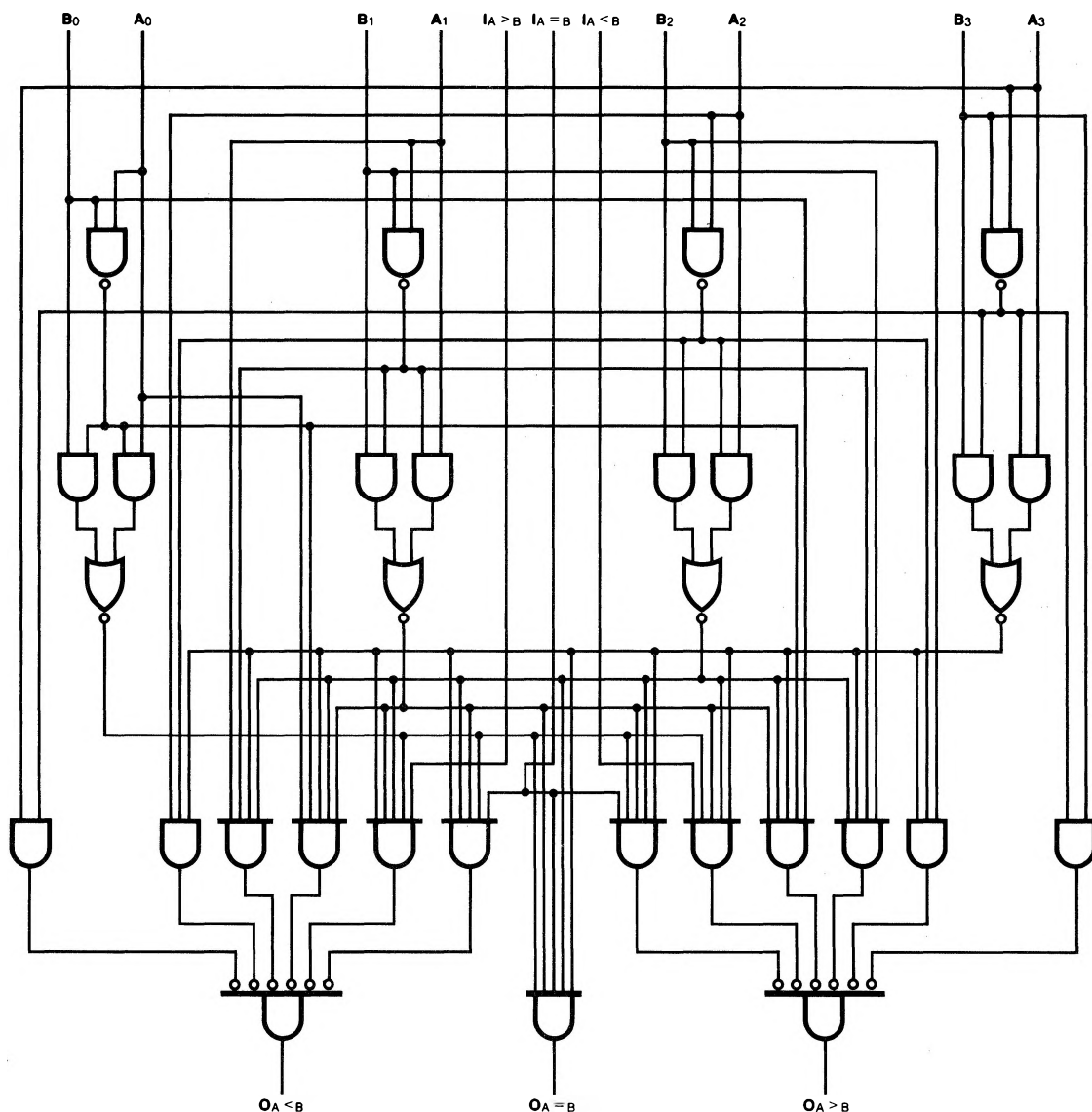
V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A ₀ — A ₃	Word A Inputs	3.0/3.0	1.5/0.75
B ₀ — B ₃	Word B Inputs	3.0/3.0	1.5/0.75
IA = B	A = B Expansion Input	3.0/3.0	1.5/0.75
IA < B, IA > B	A < B, A > B Expansion Inputs	1.0/1.0	0.5/0.25
OA > B	A Greater Than B Output	10/10	10/5.0 (2.5)
OA < B	A Less Than B Output	10/10	10/5.0 (2.5)
OA = B	A Equal B Output	10/10	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION—The '85 compares two 4-bit words (A, B). Each word has four parallel inputs (A_0 — A_3 , B_0 — B_3) of which A_3 and B_3 are the most significant. Three expander inputs ($I_A > B$, $I_A < B$, $I_A = B$) allow cascading without external gates. The three outputs ($O_A > B$, $O_A < B$, $O_A = B$) have only two gate delays from the expander inputs, thus reducing the delay time when units are cascaded for long words. The $I_A = B$ input to the least significant position must be held HIGH for proper compare operation. For serial (ripple) expansion, the $A > B$, $A < B$ and $A = B$ outputs are connected respectively to the $I_A > B$, $I_A < B$, and $I_A = B$ inputs of the next most significant comparator.

LOGIC DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	I _A > B	I _A < B	I _A = B	O _A > B	O _A < B	O _A = B
A ₃ > B ₃	X	X	X	X	X	X	H	L	L
A ₃ < B ₃	X	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ > B ₂	X	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ < B ₂	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ > B ₁	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ < B ₁	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ > B ₀	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ < B ₀	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	L	L	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	H	L	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	X	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	L	H	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	H	L	L	L	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

APPLICATIONS — Figure a shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure b six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table I.

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2-6
25-120 Bits	8-31

NOTE:

The 54LS/74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A₀ — A₃ and B₀ — B₃ inputs of another 54LS/74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.

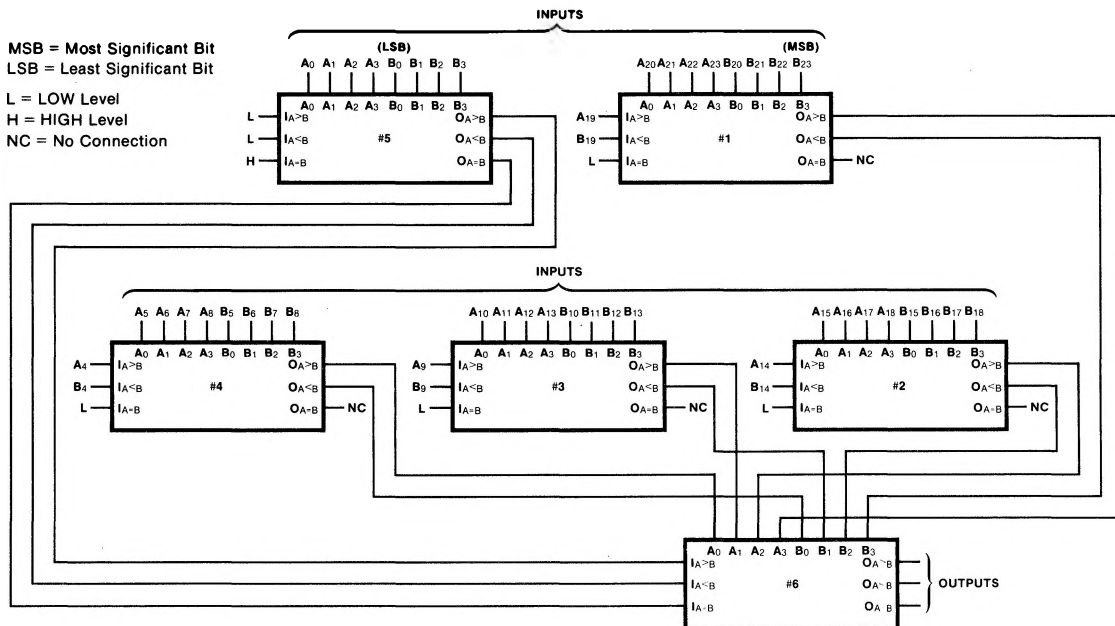


Fig. a Comparison of Two 24-Bit Words

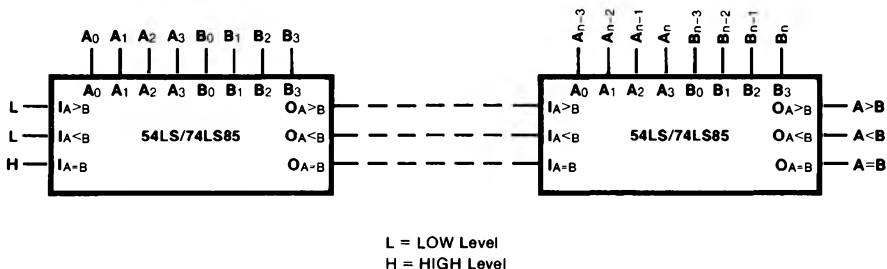


Fig. b Comparison of Two n-Bit Words

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max		
Ios	Output Short Circuit Current	XM	-20	-55	-20	-100	mA	Vcc = Max
		XC	-18	-55				
Icc	Power Supply Current		88		20		mA	Vcc = Max IA = B = Gnd Other Inputs Open

AC CHARACTERISTICS: Vcc = +5.0 V, TA = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		CL = 15 pF RL = 400 Ω		CL = 15 pF			
		Min	Max	Min	Max		
tPLH tPHL	Propagation Delay An or Bn to OA > B or OA < B	26 30		36 30		ns	Figs. 3-1, 3-20
tPLH tPHL	Propagation Delay An or Bn to OA = B	35 30		45 45			
tPLH tPHL	Propagation Delay An lxx to OA > B or OA < B	11 17		22 17		ns	Figs. 3-1, 3-4
tPLH tPHL	Propagation Delay IA = B to OA = B	20 17		22 17			