



54LS85/DM54LS85/DM74LS85

4-Bit Magnitude Comparators

General Description

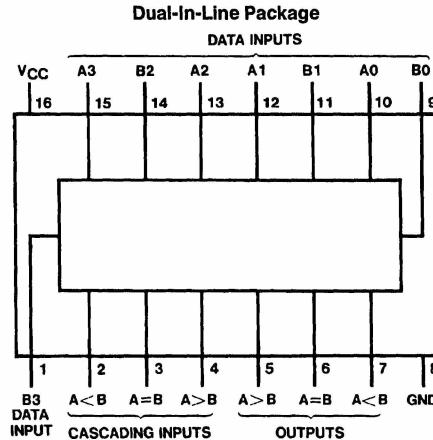
These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must

have a high-level voltage applied to the A = B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Features

- Typical power dissipation 52 mW
- Typical delay (4-bit words) 24 ns
- Alternate Military/Aerospace device (54LS85) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



Order Number 54LS85DMQB,
54LS85FMQB, 54LS85LMQB,
DM54LS85J, DM54LS85W,
DM74LS85M or DM74LS85N
See NS Package Number E20A,
J16A, M16A, N16E or W16A

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Function Table

| Comparing Inputs | | | | Cascading Inputs | | | Outputs | | |
|------------------|---------|---------|---------|------------------|-------|-------|---------|-------|-------|
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A > B | A < B | A = B | A > B | A < B | A = B |
| A3 > B3 | X | X | X | X | X | X | H | L | L |
| A3 < B3 | X | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 > B2 | X | X | X | X | X | H | L | L |
| A3 = B3 | A2 < B2 | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 > B1 | X | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 < B1 | X | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 > B0 | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 < B0 | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | L | L | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | H | L | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | H | L | L | H |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | X | X | H | L | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | H | L | L | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | H | H | H | L |

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | |
| DM54LS and 54LS | -55°C to +125°C |
| DM74LS | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | DM54LS85 | | | DM74LS85 | | | Units |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|-------|
| | | Min | Nom | Max | Min | Nom | Max | |
| V _{CC} | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High Level Input Voltage | 2 | | | 2 | | | V |
| V _{IL} | Low Level Input Voltage | | | 0.7 | | | 0.8 | V |
| I _{OH} | High Level Output Current | | | -0.4 | | | -0.4 | mA |
| I _{OL} | Low Level Output Current | | | 4 | | | 8 | mA |
| T _A | Free Air Operating Temperature | -55 | | 125 | 0 | | 70 | °C |

Electrical Characteristics

 over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 1) | Max | Units |
|-----------------|-----------------------------------|--|-------|-----------------|------|-------|
| V _I | Input Clamp Voltage | V _{CC} = Min, I _I = -18 mA | | | -1.5 | V |
| V _{OH} | High Level Output Voltage | V _{CC} = Min, I _{OH} = Max | DM54 | 2.5 | 3.4 | V |
| | | V _{IL} = Max, V _{IH} = Min | DM74 | 2.7 | 3.4 | |
| V _{OL} | Low Level Output Voltage | V _{CC} = Min, I _{OL} = Max | DM54 | 0.25 | 0.4 | V |
| | | V _{IL} = Max, V _{IH} = Min | DM74 | 0.35 | 0.5 | |
| | | I _{OL} = 4 mA, V _{CC} = Min | DM74 | 0.25 | 0.4 | |
| I _I | Input Current @ Max Input Voltage | V _{CC} = Max | A < B | | 0.1 | mA |
| | | V _I = 7V | A > B | | 0.1 | |
| | | Others | | | 0.3 | |
| I _{IH} | High Level Input Current | V _{CC} = Max | A < B | | 20 | μA |
| | | V _I = 2.7V | A > B | | 20 | |
| | | Others | | | 60 | |
| I _{IL} | Low Level Input Current | V _{CC} = Max | A < B | | -0.4 | mA |
| | | V _I = 0.4V | A > B | | -0.4 | |
| | | Others | | | -1.2 | |
| I _{os} | Short Circuit Output Current | V _{CC} = Max (Note 2) | DM54 | -20 | | mA |
| | | | DM74 | -20 | | |
| I _{CC} | Supply Current | V _{CC} = Max (Note 3) | | 10 | 20 | mA |

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

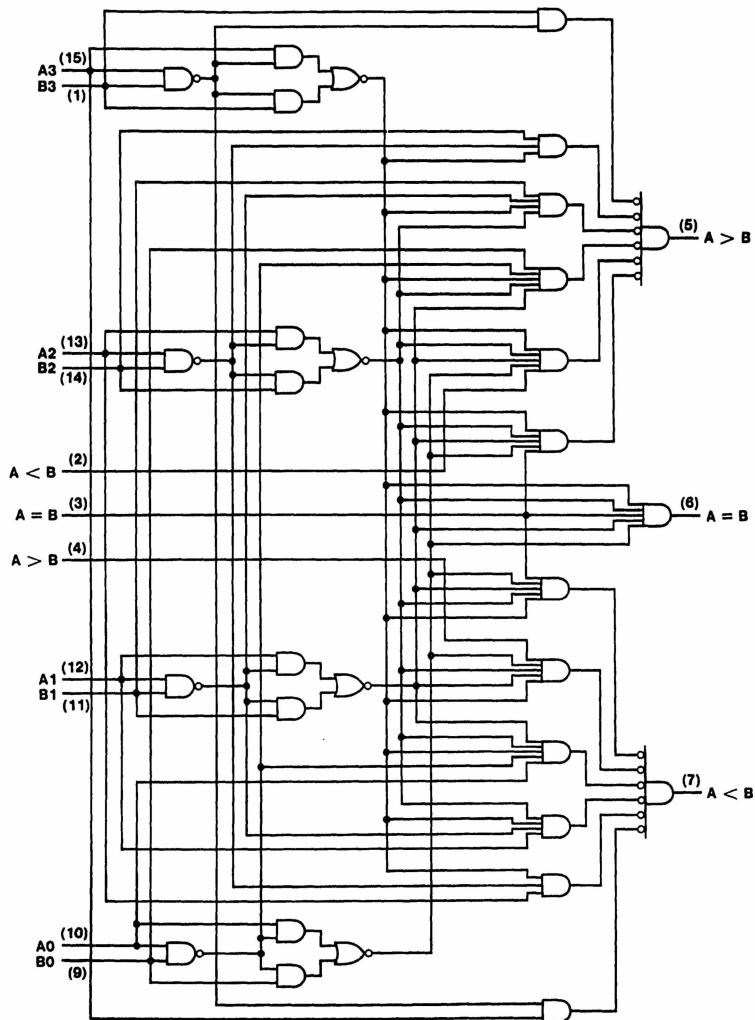
Note 3: I_{CC} is measured with all outputs open, A = B grounded and all other inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From Input | To Output | Number of Gate Levels | $R_L = 2 \text{ k}\Omega$ | | | | Units | |
|-----------|--|--------------------------|-----------------|-----------------------|---------------------------|-----|-----------------------|-----|-------|--|
| | | | | | $C_L = 15 \text{ pF}$ | | $C_L = 50 \text{ pF}$ | | | |
| | | | | | Min | Max | Min | Max | | |
| t_{PLH} | Propagation Delay Time Low-to-High Level Output | Any A or B Data Input | A < B, A > B | 3 | | 36 | | 42 | ns | |
| | | | A = B | 4 | | 40 | | 40 | | |
| t_{PHL} | Propagation Delay Time High-to-Low Level Output | Any A or B Data Input | A < B, A > B | 3 | | 30 | | 40 | ns | |
| | | | A = B | 4 | | 30 | | 40 | | |
| t_{PLH} | Propagation Delay Time Low-to-High Level Output | A < B or A = B | A > B | 1 | | 22 | | 26 | ns | |
| t_{PHL} | Propagation Delay Time High-to-Low Level Output | A < B or A = B | A > B | 1 | | 17 | | 26 | ns | |
| t_{PLH} | Propagation Delay Time Low-to-High Level Output | A = B | A = B | 2 | | 20 | | 25 | ns | |
| t_{PHL} | Propagation Delay Time High-to-Low Level Output | A = B | A = B | 2 | | 17 | | 26 | ns | |
| t_{PLH} | Propagation Delay Time Low-to-High Level Output | A > B or A = B | A < B | 1 | | 22 | | 26 | ns | |
| t_{PHL} | Propagation Delay Time High-to-Low Level Output | A > B or A = B | A < B | 1 | | 17 | | 26 | ns | |

Logic Diagram

LS85



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