

54/7490A

54LS/74LS90

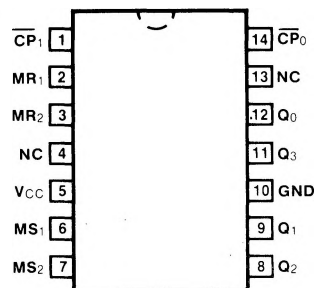
DECADE COUNTER

DESCRIPTION — The '90 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops connected as a divide-by-five counter. It can be connected to operate with a conventional BCD output pattern or it can be connected to provide a 50% duty cycle output. In the BCD mode, HIGH signals on the Master Set (MS) inputs set the outputs to BCD nine. HIGH signals on the Master Reset (MR) inputs force all outputs LOW. For a similar counter with corner power pins, see the 'LS290; for dual versions, see the 'LS390 and 'LS490.

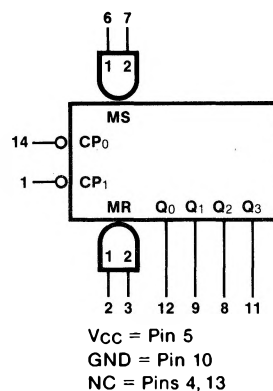
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	7490APC, 74LS90PC		9A
Ceramic DIP (D)	A	7490ADC, 74LS90DC	5490ADM, 54LS90DM	6A
Flatpak (F)	A	7490AFC, 74LS90FC	5490AFM, 54LS90FM	3I

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP}_0$	$\div 2$ Section Clock Input (Active Falling Edge)	2.0/2.0	0.125/1.5
$\overline{CP}_1$	$\div 5$ Section Clock Input (Active Falling Edge)	3.0/3.0	0.250/2.0
MR ₁ , MR ₂	Asynchronous Master Reset Inputs (Active HIGH)	1.0/1.0	0.5/0.25
MS ₁ , MS ₂	Asynchronous Master Set (Preset 9) Inputs (Active HIGH)	1.0/1.0	0.5/0.25
Q ₀	$\div 2$ Section Output*	20/10	10/5.0 (2.5)
Q ₁ — Q ₃	$\div 5$ Section Outputs	20/10	10/5.0 (2.5)

*The Q₀ output is guaranteed to drive the full rated fan-out plus the $\overline{CP}_1$ input.

FUNCTIONAL DESCRIPTION — The '90 is a 4-bit ripple type decade counter. It consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input. A gated AND asynchronous Master Reset (MR_1, MR_2) is provided which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set (MS_1, MS_2) is provided which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH). Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:.

- A. BCD Decade (8421) Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.
- B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0 .
- C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

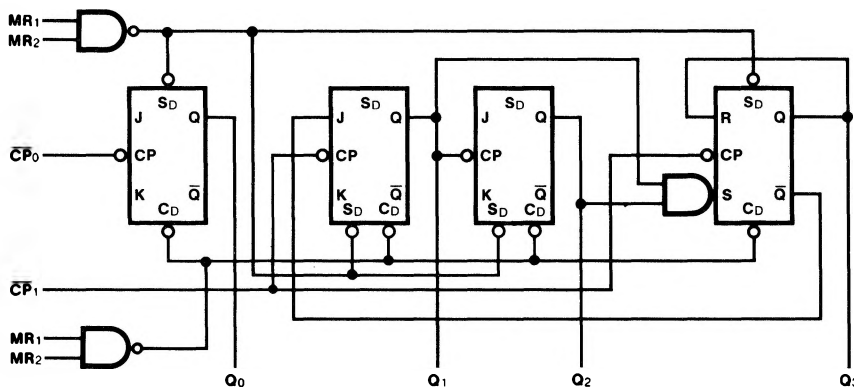
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

BCD COUNT SEQUENCE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input $\overline{CP}_1$ for BCD count.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max				
I_{IH}	Input HIGH Current, $\overline{CP}_0$	1.0		0.2		mA	$V_{CC} = \text{Max}$, $V_{IN} = 5.5 \text{ V}$
I_{IH}	Input HIGH Current $\overline{CP}_1$	1.0		0.4		mA	$V_{CC} = \text{Max}$, $V_{IN} = 5.5 \text{ V}$
I_{CC}	Power Supply Current	42		15		mA	$V_{CC} = \text{Max}$

AC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^\circ \text{ C}$ (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		CL = 15 pF RL = 400 Ω		CL = 15 pF			
		Min	Max	Min	Max		
fmax	Maximum Count Frequency, CP0	32		32		MHz	Figs. 3-1, 3-9
fmax	Maximum Count Frequency, CP1	16		16		MHz	Figs. 3-1, 3-9
tPLH tPHL	Propagation Delay CP0 to Q0	16 18		16 18		ns	Figs. 3-1, 3-9
tPLH tPHL	Propagation Delay CP0 to Q3	48 50		48 50		ns	Figs. 3-1, 3-9
tPLH tPHL	Propagation Delay CP1 to Q1	16 21		16 21		ns	Figs. 3-1, 3-9
tPLH tPHL	Propagation Delay CP1 to Q2	32 35		32 35		ns	Figs. 3-1, 3-9
tPLH tPHL	Propagation Delay CP1 to Q3	32 35		32 35		ns	Figs. 3-1, 3-9
tPLH	Propagation Delay MS to Q0 and Q3	30		30		ns	Figs. 3-1, 3-17
tPHL	Propagation Delay MS to Q1 and Q3	40		40		ns	Figs. 3-1, 3-17
tPHL	Propagation Delay MR to Qn	40		40		ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^\circ \text{ C}$

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
$t_w (H)$	$\overline{CP}_0$ Pulse Width HIGH	15		15		ns	Fig. 3-9
$t_w (H)$	$\overline{CP}_1$ Pulse Width HIGH	30		30		ns	Fig. 3-9
$t_w (H)$	MS Pulse Width HIGH	15		15		ns	Fig. 3-17
$t_w (H)$	MR Pulse Width HIGH	15		15		ns	Fig. 3-17
t_{rec}	Recovery Time, MS to $\overline{CP}$	25		25		ns	Fig. 3-17
t_{rec}	Recovery Time, MR to $\overline{CP}$	25		25		ns	Fig. 3-17