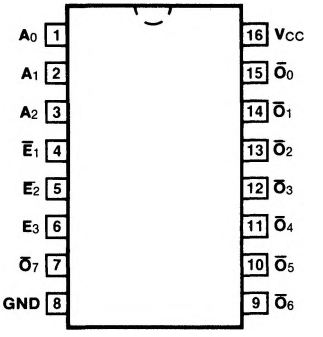
54S/74S138
54LS/74LS138
1-OF-8 DECODER/DEMULTIPLEXER

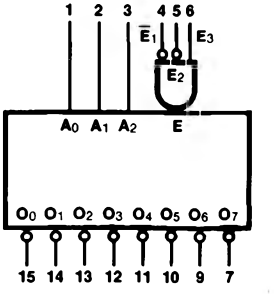
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '138 is a high speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three '138 devices or to a 1-of-32 decoder using four '138 devices and one inverter. The '138 is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **DEMULTIPLEXING CAPABILITY**
- **MULTIPLE INPUT ENABLE FOR EASY EXPANSION**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S138PC, 74LS138PC		9B
Ceramic DIP (D)	A	74S138DC, 74LS138DC	54S138DM, 54LS138DM	6B
Flatpak (F)	A	74S138FC, 74LS138FC	54S138FM, 54LS138FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_2$	Address Inputs	1.25/1.25	0.5/0.25
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)	1.25/1.25	0.5/0.25
E_3	Enable Input (Active HIGH)	1.25/1.25	0.5/0.25
$\overline{O}_0 - \overline{O}_7$	Outputs (Active LOW)	25/12.5	10/5.0 (2.5)

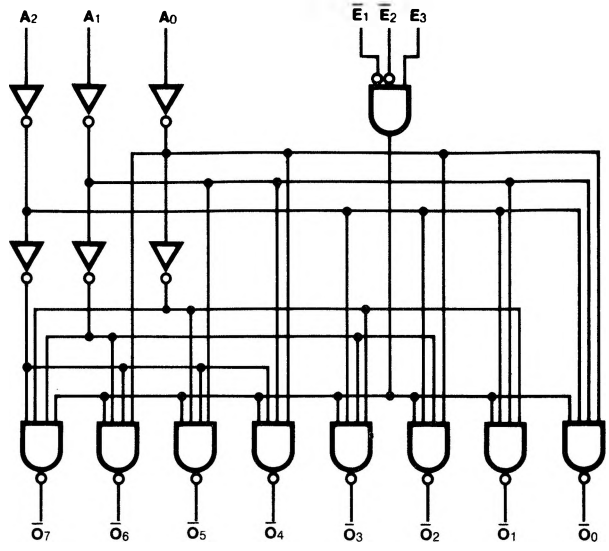
FUNCTIONAL DESCRIPTION — The '138 is a high speed 1-of-8 decoder/demultiplexer fabricated with the low power Schottky barrrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$ — $\overline{O}_7$). The '138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138 devices and one inverter. (See *Figure a.*) The '138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



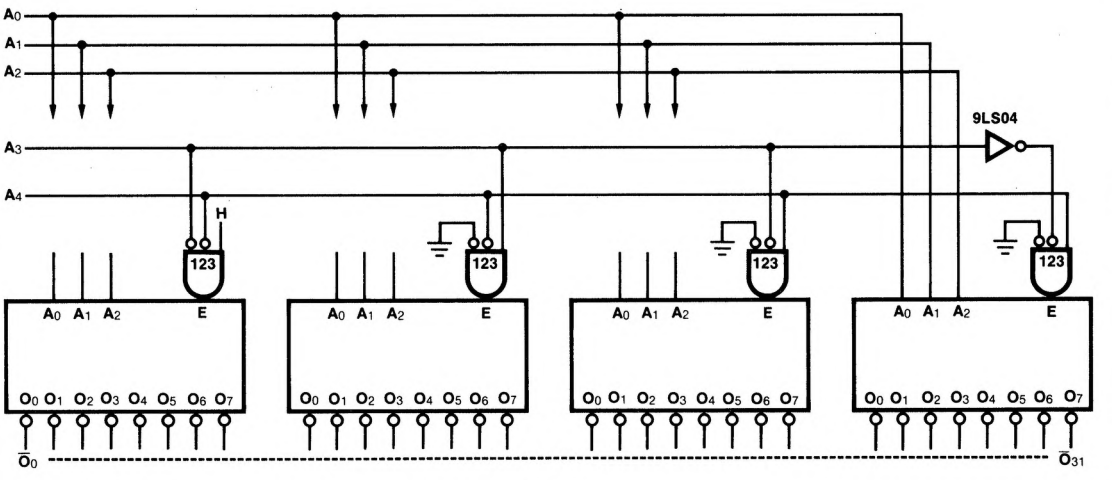


Fig. a

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		74		10	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S C_L = 15 pF, R_L = 280 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		12 12		18 27	ns	Figs. 3-1, 3-4, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		8.0 11		15 24	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$		11 11		18 28	ns	Figs. 3-1, 3-4