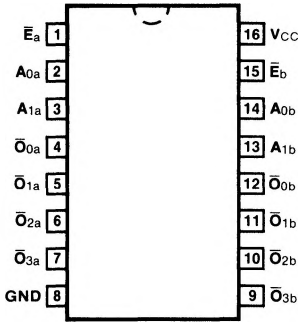
139

54S/74S139
54LS/74LS139
DUAL 1-OF-4 DECODER

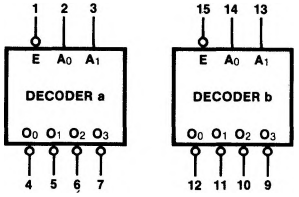
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '139 is a high speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the '139 can be used as a function generator providing all four minterms of two variables. The '139 is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **TWO COMPLETELY INDEPENDENT 1-OF-4 DECODERS**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S139PC, 74LS139PC		9B
Ceramic DIP (D)	A	74S139DC, 74LS139DC	54S139DM, 54LS139DM	6B
Flatpak (F)	A	74S139FC, 74LS139FC	54S139FM, 54LS139FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A_0, A_1	Address Inputs	1.25/1.25	0.5/0.25
$\overline{E}$	Enable Input (Active LOW)	1.25/1.25	0.5/0.25
$\overline{O}_0 - \overline{O}_3$	Outputs (Active LOW)	25/12.5	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0 - \overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the '139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in *Figure* a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

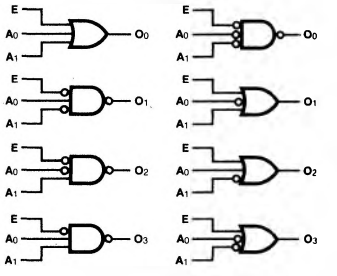
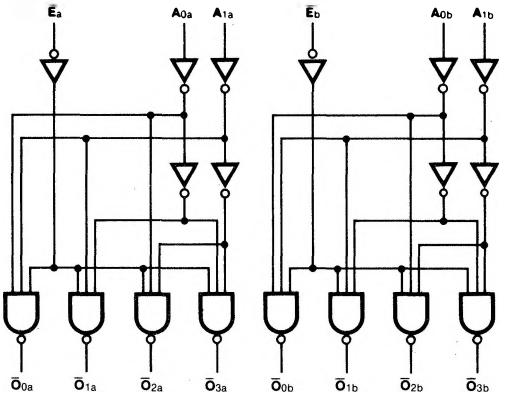


Fig. a

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwisespecified)

SYMBOL	PARAMETER	54/74LS		54/74S		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		11		90	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		54/74S		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF R_L = 280 Ω			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_n$		18 27		12 12	ns	Figs. 3-1, 3-4, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{O}_n$		15 24		8.0 10	ns	Figs. 3-1, 3-5