DESCRIPTION

The SE/NE 567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

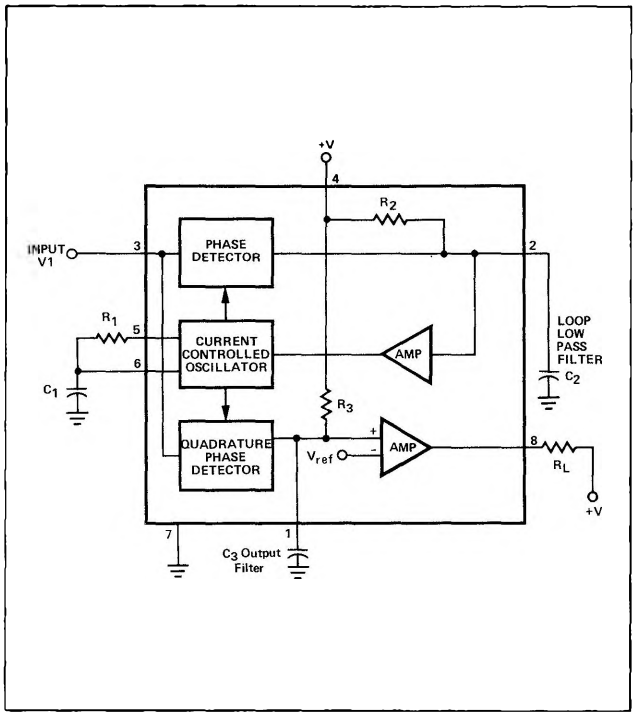
FEATURES

- WIDE FREQUENCY RANGE (.01Hz TO 500kHz)
- HIGH STABILITY OF CENTER FREQUENCY
- INDEPENDENTLY CONTROLLABLE BANDWIDTH (0 TO 14 PERCENT)
- HIGH OUT-BAND SIGNAL AND NOISE REJECTION
- LOGIC-COMPATIBLE OUTPUT WITH 100mA CURRENT SINKING CAPABILITY
- INHERENT IMMUNITY TO FALSE SIGNALS
- FREQUENCY ADJUSTMENT OVER A 20 TO 1 RANGE WITH AN EXTERNAL RESISTOR

APPLICATIONS

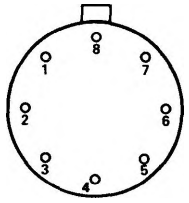
TOUCH TONE® DECODING
CARRIER CURRENT REMOTE CONTROLS
ULTRASONIC CONTROLS (REMOTE TV, ETC.)
COMMUNICATIONS PAGING
FREQUENCY MONITORING AND CONTROL
WIRELESS INTERCOM
PRECISION OSCILLATOR

BLOCK DIAGRAM



PIN CONFIGURATION

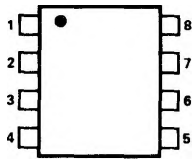
T PACKAGE
(Top View)



1. Output Filter Capacitor C_3
2. Low Pass Filter Capacitor C_2
3. Input
4. Supply Voltage +V
5. Timing Element R_1
6. Timing Elements R_1 and C_1
7. Ground
8. Output

ORDER PART NOS. SE567T/NE567T

V PACKAGE



1. Output Filter Capacitor C_3
2. Low Pass Filter Capacitor C_2
3. Input
4. Supply Voltage +V
5. Timing Element R_1
6. Timing Elements R_1 and C_1
7. Ground
8. Output

ORDER PART NO. NE567V

ABSOLUTE MAXIMUM RATINGS:

Operating Temperature	0°C to 70°C NE567 -55°C to 125°C SE567
Operating Voltage	10V
Positive Voltage at Input	0.5V above Supply Voltage (Pin 4)
Negative Voltage at Input	-10 VDC
Output Voltage (collector of output transistor)	15 VDC
Storage Temperature	-65°C to 150°C
Power Dissipation	300mW

ELECTRICAL CHARACTERISTICS (V+ = 5.0 Volts, T_A = 25°C unless noted)

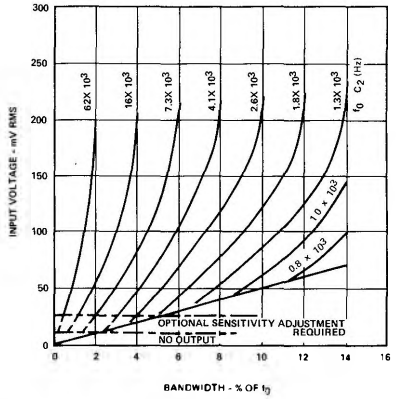
CHARACTERISTICS	SE567			NE567			UNITS	TEST CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
CENTER FREQUENCY(NOTE 1)								
Highest Center Frequency (f_o)	100	500		100	500		kHz	
Center Frequency Stability (Note 2)		35±140 35±60			35±140 35±60		ppm/°C ppm/°C	-55 to 125°C 0 to 70°C
Center Frequency Shift with Supply Voltage		0.5	1		0.7	2	%/Volt	f_o = 100KHz
DETECTION BANDWIDTH								
Largest Detection Bandwidth	12	14	16	10	14	18	% of f_o	f_o = 100KHz
Largest Detection Bandwidth Skew		1	2		2	3	% of f_o	
Largest Detection Bandwidth - Variation with Temperature		±0.1			±0.1		%/°C	V_i = 300mVrms
Largest Detection Bandwidth - Variation with Supply Voltage		±2			±2		%/Volt	V_i = 300mVrms
INPUT								
Input Resistance		20			20		KΩ	
Smallest Detectable Input Voltage(V_i)		20	25		20	25	mV rms	I_L = 100mA, $f_i = f_o$
Largest No-Output Input Voltage	10	15		10	15		mV rms	I_L = 100mA, $f_i = f_o$
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6			+6		dB	
Minimum Input Signal to Wideband Noise Ratio		-6			-6		dB	Bn = 140KHz
OUTPUT								
Fastest On-Off Cycling Rate		f_o/20			f_o/20			
"1" Output Leakage Current		0.01	25		0.01	25	μA	
"0" Output Voltage		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	Volt Volt	I_L = 30mA I_L = 100mA
Output Fall Time (Note 3)		30			30		n sec	R_L = 50Ω
Output Rise Time (Note 3)		150			150		n sec	R_L = 50Ω
GENERAL								
Operating Voltage Range	4.75		9.0	4.75		9.0	Volts	
Supply Current - Quiescent		6	8		7	10	mA	
Supply Current - Activated		11	13		12	15	mA	R_L = 20KΩ
Quiescent Power Dissipation		30			35		mW	

NOTES:

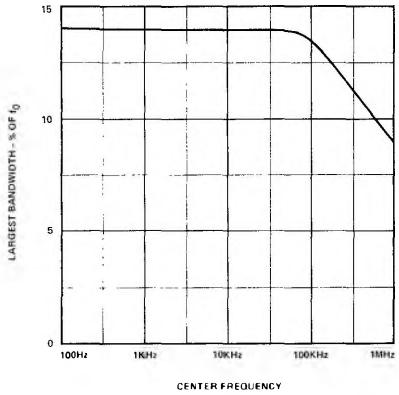
1. Frequency determining resistor R_1 should be between 1 and 20KΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.

TYPICAL CHARACTERISTIC CURVES

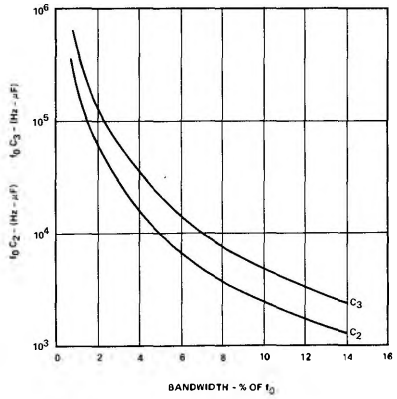
BANDWIDTH VERSUS INPUT SIGNAL AMPLITUDE



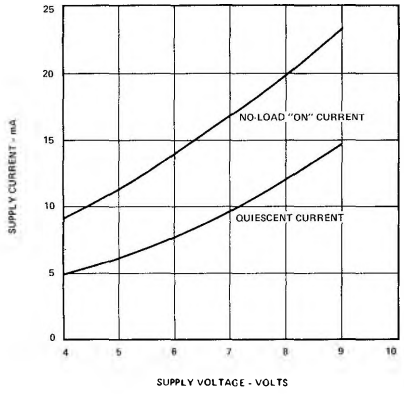
LARGEST DETECTION BANDWIDTH VERSUS OPERATING FREQUENCY



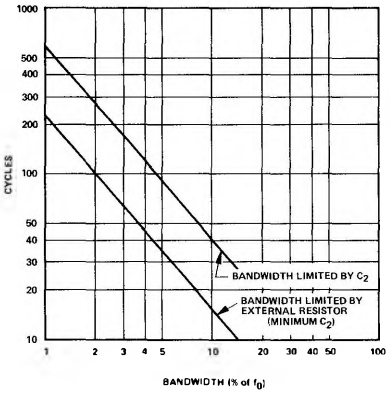
DETECTION BANDWIDTH AS A FUNCTION OF C_2 AND C_3



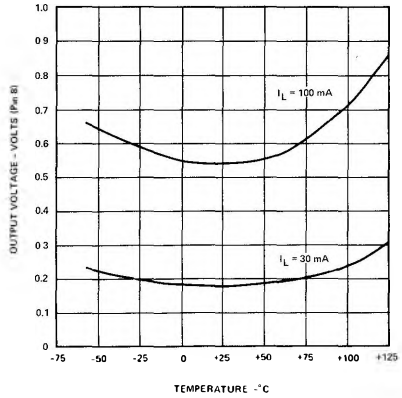
TYPICAL SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



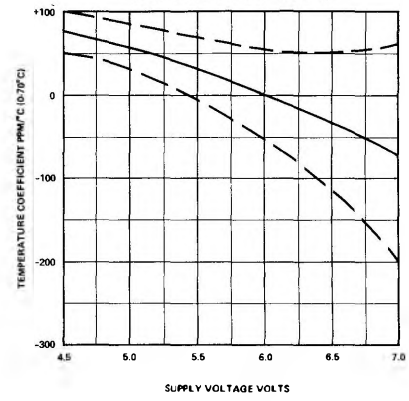
GREATEST NUMBER OF CYCLES BEFORE OUTPUT



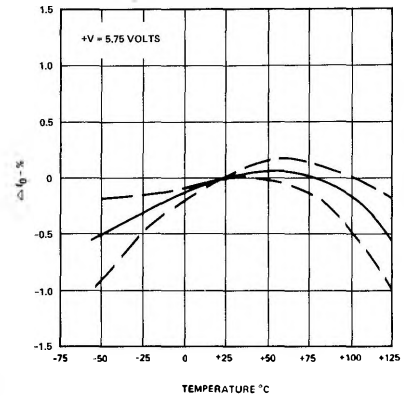
TYPICAL OUTPUT VOLTAGE VERSUS TEMPERATURE



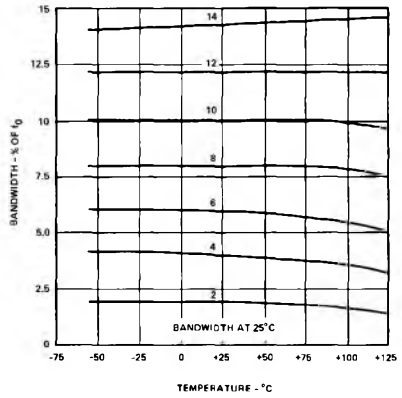
CENTER FREQUENCY COEFFICIENT TEMPERATURE (MEAN AND S.D.)



TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)

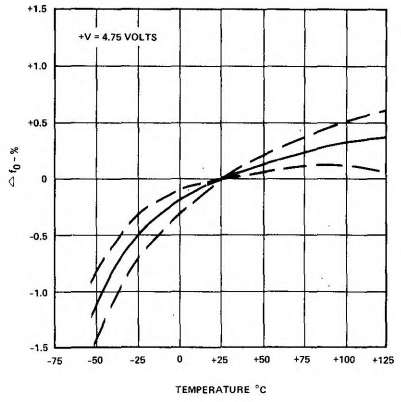


TYPICAL BANDWIDTH VARIATION WITH TEMPERATURE

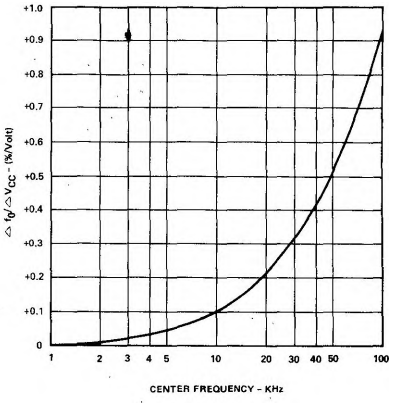


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

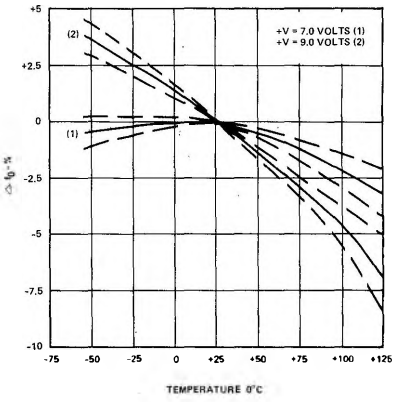
TYPICAL FREQUENCY DRIFT WITH (MEAN AND S.D.) TEMPERATURE



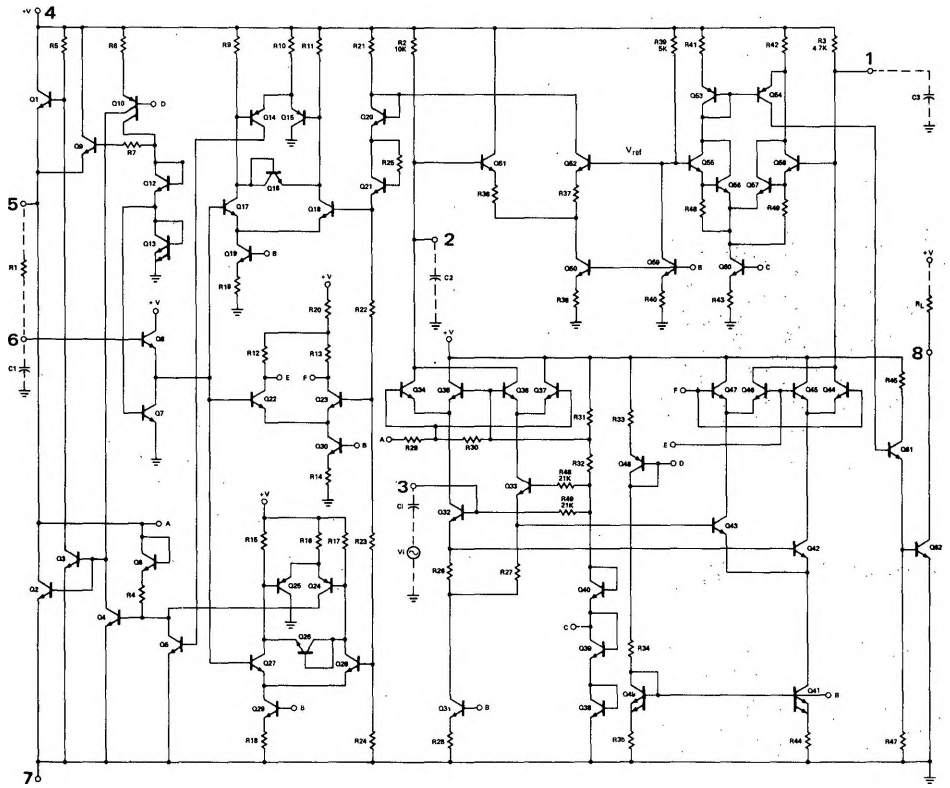
CENTER FREQUENCY SHIFT WITH SUPPLY VOLTAGE CHANGE VERSUS OPERATING FREQUENCY



TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



SCHEMATIC DIAGRAM



DESIGN FORMULAS

$$f_0 \simeq \frac{1}{R_1 C_1}$$

$$BW \simeq 1070 \sqrt{\frac{V_i}{f_0 C_2}} \quad \text{in \% of } f_0$$

Where

V_i = Input Voltage (Volts)
C_2 = Low-Pass Filter Capacitor (μF)

PHASE LOCKED LOOP TERMINOLOGY

CENTER FREQUENCY (f_0)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

DETECTION BANDWIDTH (BW)

The frequency range, centered about f_0, within which an input signal above the threshold voltage (typically 20mV rms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

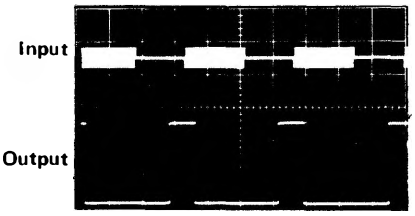
LARGEST DETECTION BANDWIDTH

The largest frequency range within which an input signal above the threshold voltage will cause a logical zero state on the output. The maximum detection bandwidth corresponds to the loop lock range.

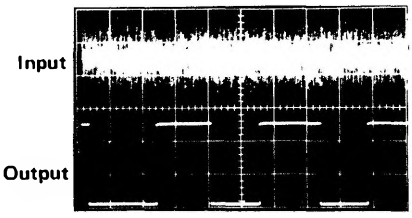
DETECTION BAND SKEW

A measure of how well the largest detection band is centered about the center frequency, f_0. The skew is defined as $(f_{max} + f_{min} - 2f_0)/f_0$ where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

TYPICAL RESPONSE



Response to 100mV RMS tone burst.
R_L = 100 ohms.



Response to same input tone burst with wideband noise.
$\frac{S}{N}$ = -6db R_L = 100 ohms
Noise Bandwidth = 140 Hz

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R_1 and C_1 for the desired center frequency ($f_0 \simeq 1/R_1 C_1$). For best temperature stability, R_1 should be between 2 and 20 ohm, and the R_1C_1 product should have sufficient stability, over the projected temperature range to meet the necessary requirements.
2. Select the low-pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_0C_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_0C_2 product.
3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such a delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

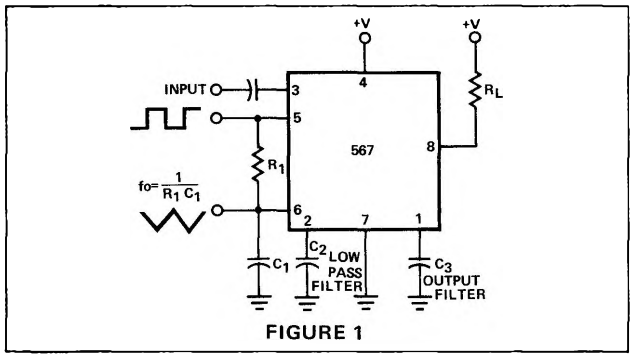


FIGURE 1

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output, a linear function of frequency, over the range of 0.95 to 1.05 f_0, with a slope of about 20mV/% frequency deviation. The average voltage at pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(V^+ - 2Vbe) \approx (V^+ - 1.4V)$ having a dc average of $V^+/2$. A 1KΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak

AVAILABLE OUTPUTS (Cont'd.)

with an average dc level of V^+ /2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

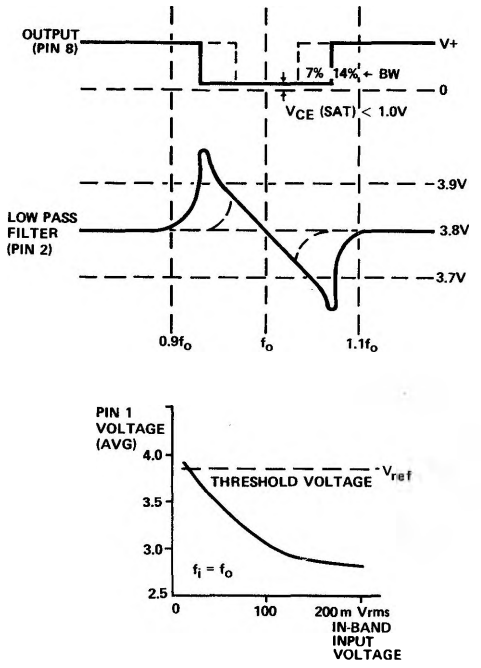


FIGURE 2

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user attain the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_o/3$, $f_o/5$, etc.

2. The 567 will lock onto signals near $(2n+1)\ f_o$, and will give an output for signals near $(4n+1)\ f_o$ where n = 0, 1, 2, etc. Thus, signals at 5 f_o and 9 f_o can cause an unwanted output. If such signals are anticipated, they should be attentuated before reaching the 567 input.

3. Maximum immunity from noise and out-band signals is afforded in the low input level (Below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs. Bandwidth graph.

4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with an 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply, or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_0/10$ baud.

$$C_2 = \frac{130}{f_o}\mu F$$

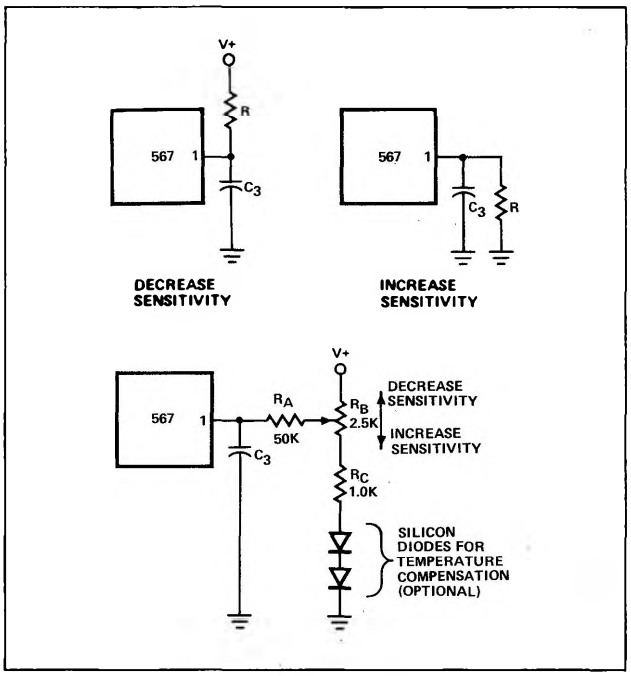
$$C_3 = \frac{260}{f_o}\mu F$$

in cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased low-voltage zeners or forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

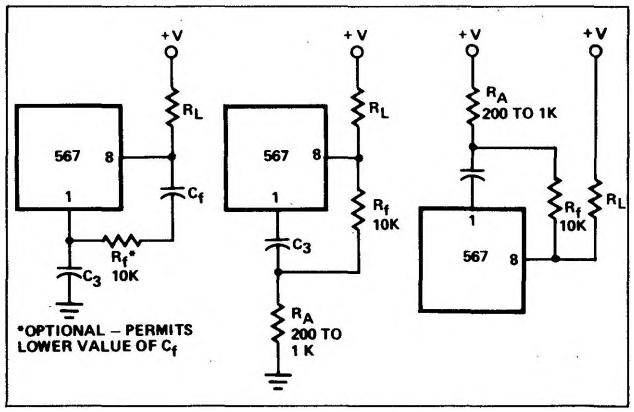
SENSITIVITY ADJUSTMENT



When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10m or lower).

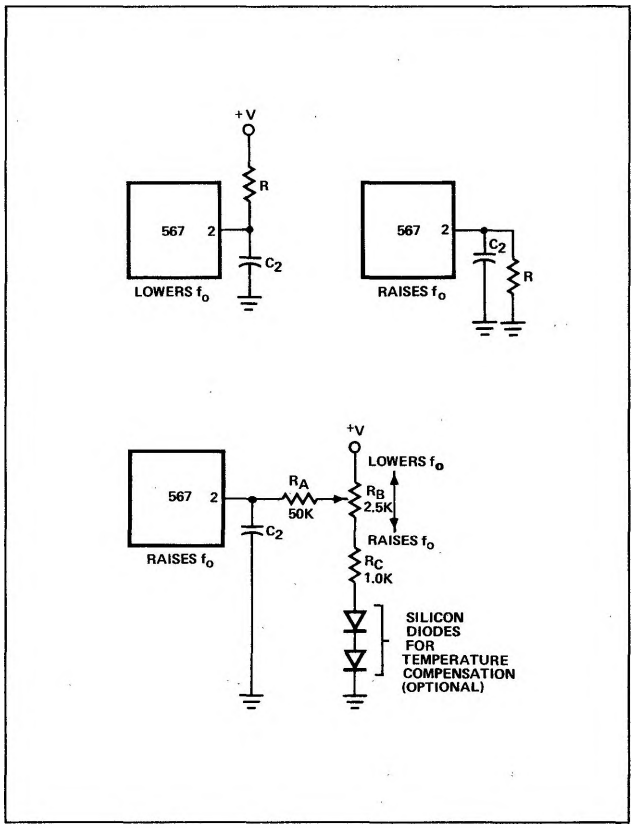
By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION



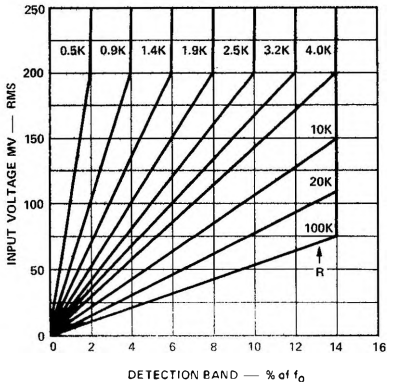
Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input, (pin 1) the chatter can be eliminated. Three schemes for doing this are given above. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

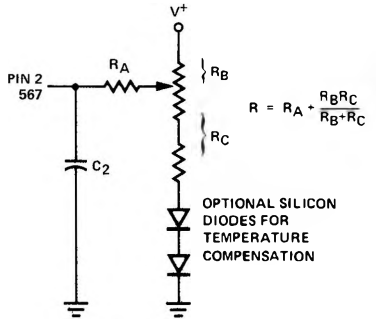
DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT



When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the largest detection band (lock range), the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

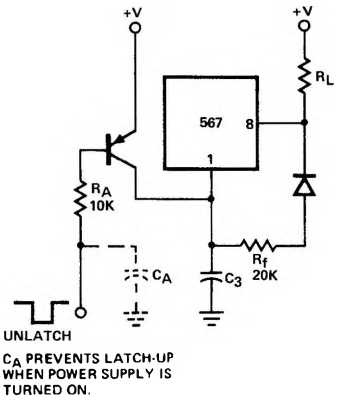


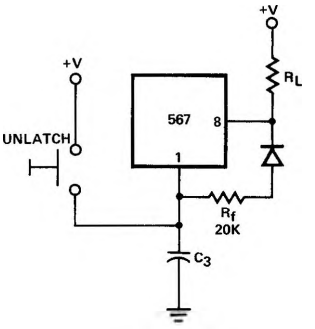


NOTE: Adjust control for symmetry of detection band edges about f_o.

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band operation. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the R_B, R_C network can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

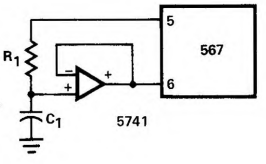
OUTPUT LATCHING





To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

REDUCTION OF C_1 VALUE



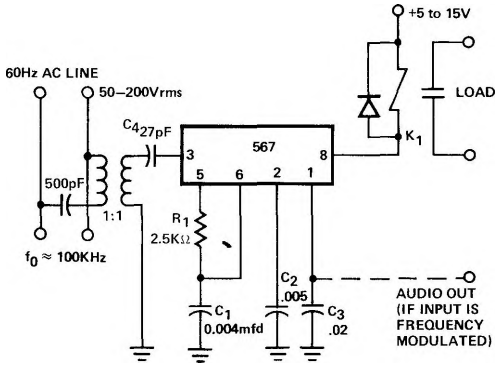
For precision, very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

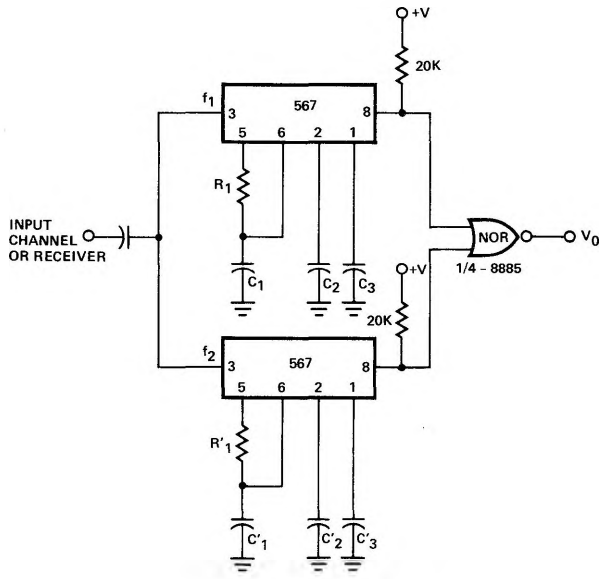
To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.

TYPICAL APPLICATIONS

CARRIER-CURRENT REMOTE CONTROL OR INTERCOM

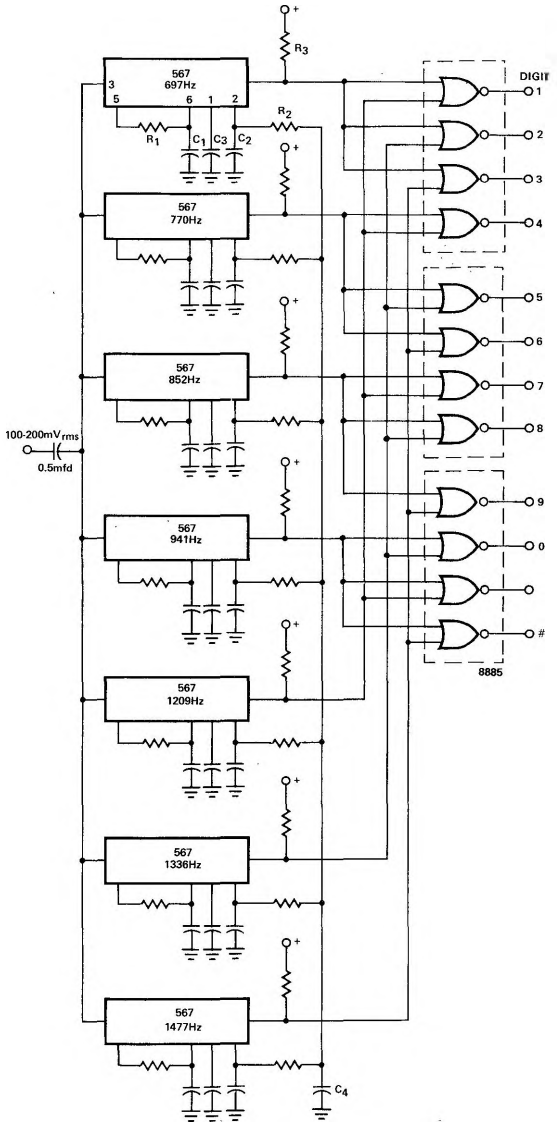


DUAL-TONE DECODER



1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1, f_2) tones is possible.

TOUCH-TONE® DECODER

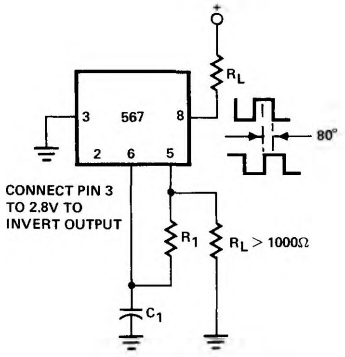


Component Values (Typical)

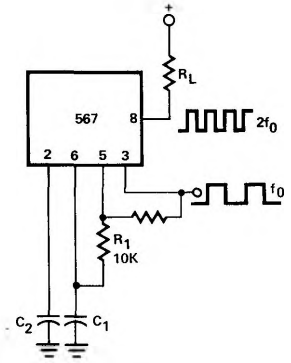
R_1	6.8 to 15K ohm
R_2	4.7K ohm
R_3	20K ohm
C_1	0.10 mfd
C_2	1.0 mfd 6V
C_3	2.2mfd 6V
C_4	250 6V

TYPICAL APPLICATIONS (Cont'd.)

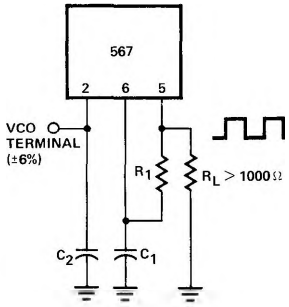
OSCILLATOR WITH QUADRATURE OUTPUT



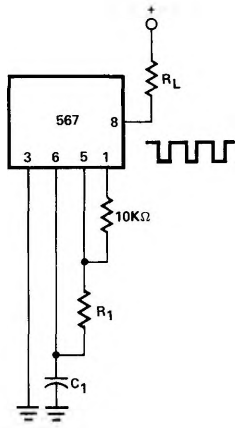
OSCILLATOR WITH DOUBLE FREQUENCY OUTPUT



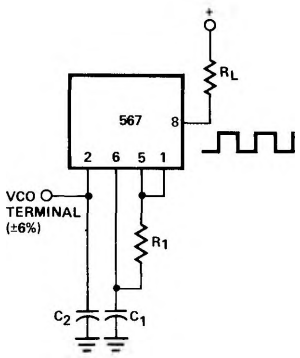
PRECISION OSCILLATOR WITH 20nsec SWITCHING



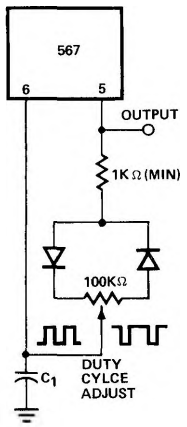
PULSE GENERATOR WITH 25% DUTY CYCLE



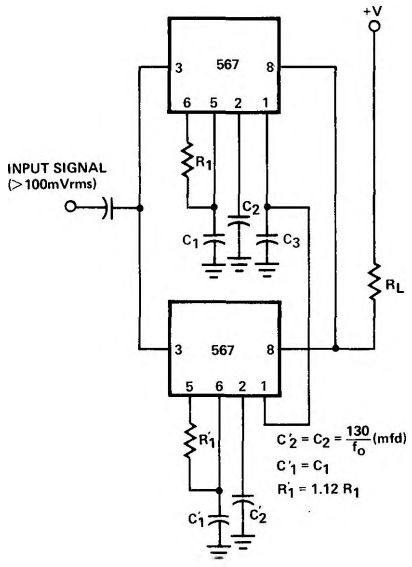
PRECISION OSCILLATOR TO SWITCH 100ma LOADS



PULSE GENERATOR



24% BANDWIDTH TONE DECODER



0° TO 180° PHASE SHIFTER