Freescale Semiconductor
56F8013 Product Brief

The 56F8013 is a member of the 56800E core-based family of Digital Signal Controllers (DSCs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create a cost-effective solution for motor control applications requiring a greater number of PWM modules.

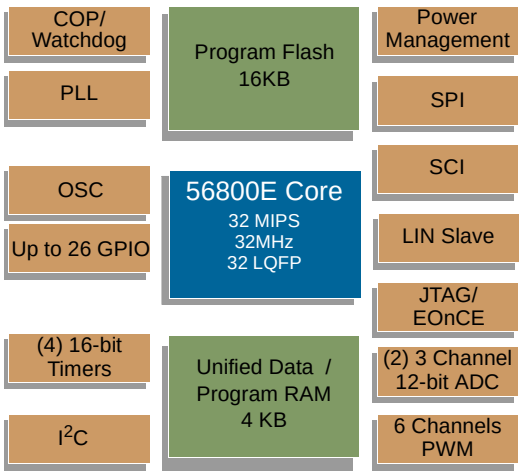
Because of its low cost, configuration flexibility, and compact program code, the 56F8013 is well suited for many applications. The 56800E core is based on a Harvard architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications.

BENEFITS

- Hybrid architecture facilitates implementation of both control and signal processing functions in a single device
- Extended temperature range allows for operation of non-volatile memory in harsh environments
- Flash memory emulation of EEPROM eliminates the need for external non-volatile memory
- High performance with 16-bit code density
- On-chip voltage regulator and power management reduces overall system cost
- Flexible power saving modes
- System-on-a-chip integration of flexible peripherals eliminates external components, improves system reliability and minimizes system cost
- High-performance PWM with programmable fault capability simplifies design and promotes compliance with safety regulations
- PWM, ADC, and Quad Timers modules coupled to reduce processing overhead
- Low-voltage interrupts protect the system from brownout or power failure
- Simple in-application Flash memory programming via Enhanced OnCE™ or serial communication
- PWM and Timers can be clocked at up to 96MHz
- High-performance 12-bit ADC

56800E CORE FEATURES

- Up to 32 MIPS at 32MHz execution frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- JTAG/Enhanced On-Chip Emulation (EOnCE) for unobtrusive, real-time debugging
- Four 36-bit accumulators
- 16- and 32-bit bidirectional barrel shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops available
- Three internal address buses
- Four internal data buses
- MCU-style software stack support
- Controller-style addressing modes and instructions
- Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Proven to deliver more control functionality with a smaller memory footprint than competing architectures



EXAMPLE APPLICATIONS

- Industrial motor control
- Dimming lamp ballast
- Switched-mode power supply
- Soft-switching PFC
- Appliance motor control
- DC-DC power supplies

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MEMORY FEATURES

- Architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory includes high-speed volatile and non-volatile components
  - 16KB of Program Flash
  - 4KB of Unified Data/Program RAM
- All memories operate at 32MHz (zero wait states) over temperature range (-40° to +105°C), with no software tricks or hardware accelerators required
- Flash security feature prevents unauthorized accesses to its content
- Flash protection prevents accidental modifications

AWARD-WINNING DEVELOPMENT ENVIRONMENT

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

56F8013 PERIPHERAL CIRCUIT FEATURES

- High-speed Pulse Width Modulator (PWM) that can be clocked at up to 96MHz
- Serial Peripheral Interface (SPI)
- Serial Communication Interface (SCI) with LIN Slave
- Four 16-bit Timers that can be clocked at up to 96MHz
- Software-programmable Phase Lock Loop (PLL)
- Two 12-bit Analog-to-Digital Converters (ADC) with six inputs at rates up to 1.1µs per sequential or simultaneous conversion
- Up to 26 General Purpose I/O (GPIO) pins
- Computer Operating Properly (COP)
- Integrated Power-On Reset and Low-Voltage Interrupt module
- I^2C Communication Module supporting Slave, Master and MultiMaster Mode
- On-Chip Relaxation Oscillator

ORDERING INFORMATION

PART	***MC56F8013***
PACKAGE	***32 LQFP***
ORDER NUMBER	***MC56F8013VFAE***
TEMPERATURE RANGE	***-40° to 105°C***

PRODUCT DOCUMENTATION

56F8000 Peripherals Reference Manual	Detailed peripheral description of the 56F8000 family of devices Order Number: MC56F8000RM
56F8013 Technical Data Sheet	Electrical and timing specifications, device-specific peripheral information and package and pin descriptions Order Number: MC56F8013
56F8013 Product Brief	Summary description and block diagram of the core, memory, peripherals and interfaces Order number: MC56F8013PB
DSP56800E Reference Manual	Detailed description of the DSP56800E architecture, 16-bit core processor and the instruction set Order Number: DSP56800ERM

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