High-Performance 512 x 8 Registered PROM

53/63RA481
53/63RA481A

Features/Benefits

- **Versatile synchronous and asynchronous enables**
- **Asynchronous preset and clear**
- **Edge-triggered "D" registers**
- **8-bit-wide in 24-pin SKINNYDIP® for high board density**
- **On-chip register simplifies system timing**
- **Faster cycle times**
- **16 mA I_{OL} output drive capability**
- **Reliable titanium-tungsten fuses (Ti-W), with programming yields typically greater than 98%.**

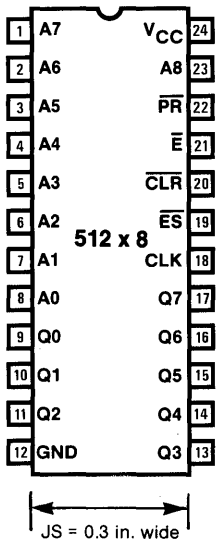
Applications

- **Microprogram control store**
- **State sequencers/state machines**
- **Next address generation**
- **Mapping PROM**

Description

The 53/63RA481 and 53/63RA481A are 512 x 8 Registered PROMs with on-chip "D" type registers, versatile output enable control through synchronous and asynchronous three-state enable inputs, and asynchronous preset and clear.

Pin Configuration



Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	PERF.	PINS	TYPE	MIL	COM
4 K	Standard	24 (28)	NS, JS (L)	53RA481	63RA481
	Enhanced			53RA481A	63RA481A

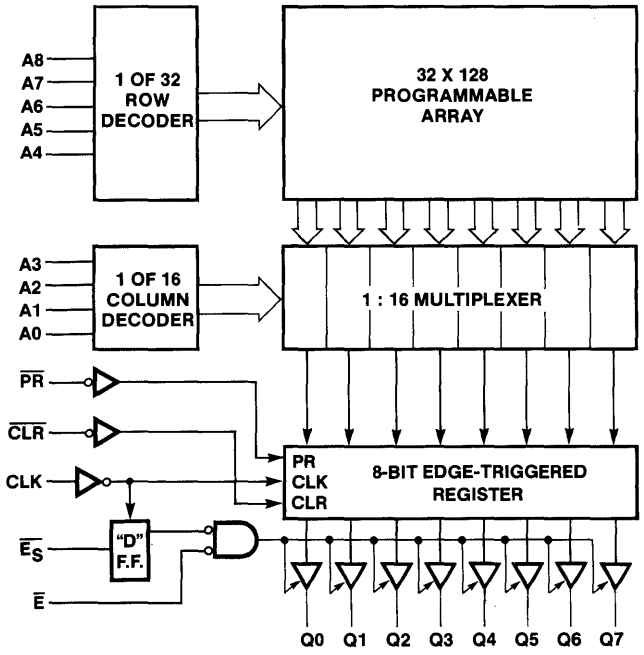
Flatpak — Contact the factory.

Data is transferred into the output registers on the rising edge of the clock. The data will appear at the outputs provided that both the asynchronous $\overline{E}$ and synchronous $\overline{ES}$ enables are Low. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made more flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting $\overline{E}$ to a High or if $\overline{ES}$ is High when the rising clock edge occurs. When V_{CC} power is first applied, the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high-impedance state.

The output registers will be set to all Highs when preset is Low independent of the state of clock. The output registers will be reset to all Lows when clear is Low independent of the state of clock. Note that preset and clear are exclusive operations and cannot occur simultaneously.

Block Diagram



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Monolithic Memories MMI

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150° C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	COMMERCIAL				MILITARY				UNIT
			63RA481A		63RA481		53RA481A		53RA481		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	5.0	4.75	5.25	4.75	5.25	4.5	5.5	4.5	5.5	V
T_A	Operating free-air temperature	25	0	75	0	75	-55	125	-55	125	°C
t_w	Width of clock (High or Low)	10	20		20		20		20		ns
t_{prw} / t_{clrw}	Width of preset or clear (Low) to Output (High or Low)	10	20		20		20		20		ns
t_{prr} / t_{clrr}	Recovery from preset or clear (Low) to clock High	11	20		20		25		25		ns
t_s (A)	Setup time from address to clock	22	30		35		35		45		ns
t_s ($\overline{ES}$)	Setup time from $\overline{ES}$ to clock	7	10		10		15		15		ns
t_h (A)	Hold time from address to clock	-5	0		0		0		0		ns
t_h ($\overline{ES}$)	Hold time from $\overline{ES}$ to clock	-3	5		5		5		5		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = -2 mA COM I_{OH} = -3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-40	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V	-20		-90	mA
I_{CC}	Supply Current	V_{CC} = MAX	All outputs open.		130	180	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC} and 25° C T_A.

Switching Characteristics Over Operating Conditions and using Standard Test Load

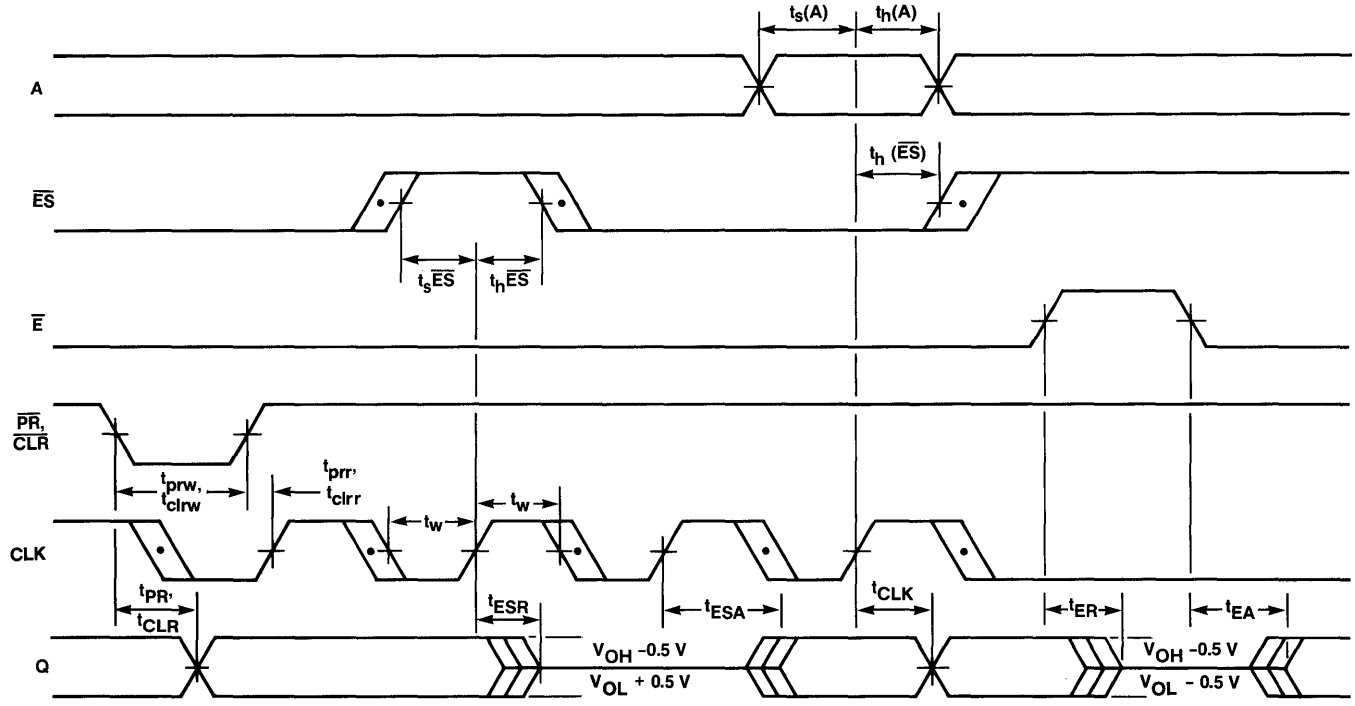
SYMBOL	PARAMETER	TYP†	COMMERCIAL		MILITARY		UNIT
			63RA481A	63RA481	53RA481A	53RA481	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t_{CLK}	Clock to output Delay	11	15	20	20	25	ns
t_{ESA}	Clock to output access time ($\overline{ES}$)	14	25	30	30	35	ns
t_{ESR}	Clock to output recovery time ($\overline{ES}$)	14	25	30	30	35	ns
t_{EA}	Enable to output access time ($\overline{E}$)	10	20	30	25	35	ns
t_{ER}	Disable to output recovery time ($\overline{E}$)	10	20	30	25	35	ns
t_{PR}	Preset to output delay ($\overline{PR}$)	15	20	25	25	30	ns
t_{CLR}	Clear to output delay ($\overline{CLR}$)	18	25	30	35	40	ns

† Typical at 5.0 V V_{CC} and 25 °C T_A

Function Table

$\overline{E}$	$\overline{ES}$	CLK	$\overline{PR}$	$\overline{CLR}$	A8-A0	Q7-Q0	Operation
H	X	X	X	X	X	Z	High-Impedance
X	H	↑	X	X	X	Z	High-Impedance
L	L	X	L	H	X	H	Preset
L	L	X	H	L	X	L	Clear
L	L	X	L	L	X	Illegal Operation	
L	L	↑	H	H	A	Data	Memory Access

Definition of Waveforms

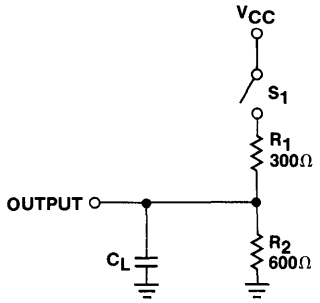


NOTES: 1. Input pulse amplitude 0 V to 3.0 V.

2. Input rise and fall times 2-5 ns from 1.0 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V level for all tests except t_{ESA} and t_{ESR}.
5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high impedance to "0" test.

   t_{ER} and t_{ESR} are tested with C_L = 5 pF. S_1 is open for "1" to high-impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} +0.5 V output level.

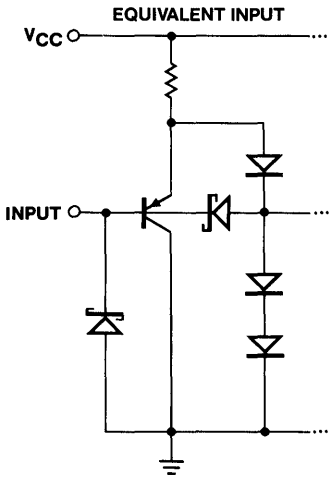
Switching Test Load

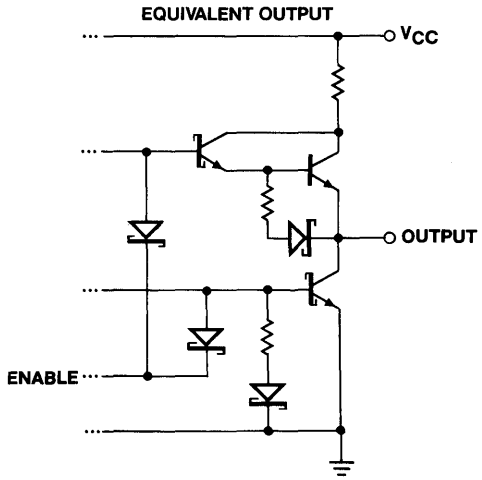


Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE	NOT APPLICABLE

Schematic of Inputs and Outputs





Programming

The 53/63RA481 and 53/63RA481A are programmed with the same programming algorithm as all other Monolithic Memories' registered PROMs. For details refer to Monolithic Memories' LSI Data Book.

Monolithic Memories' PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

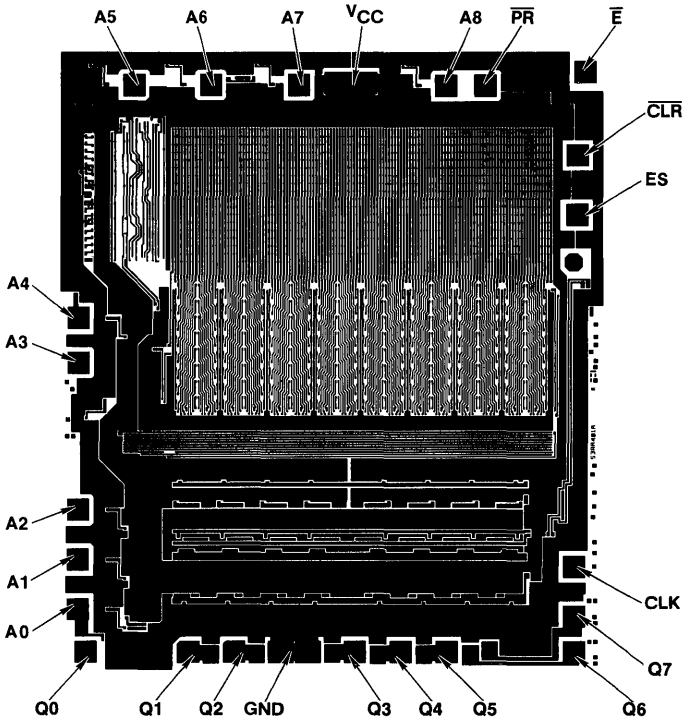
Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltage must meet published specifications for the device.

Remember — The best PROMs availale can be made unreliable by improper programming techniques.

Commercial Programmers

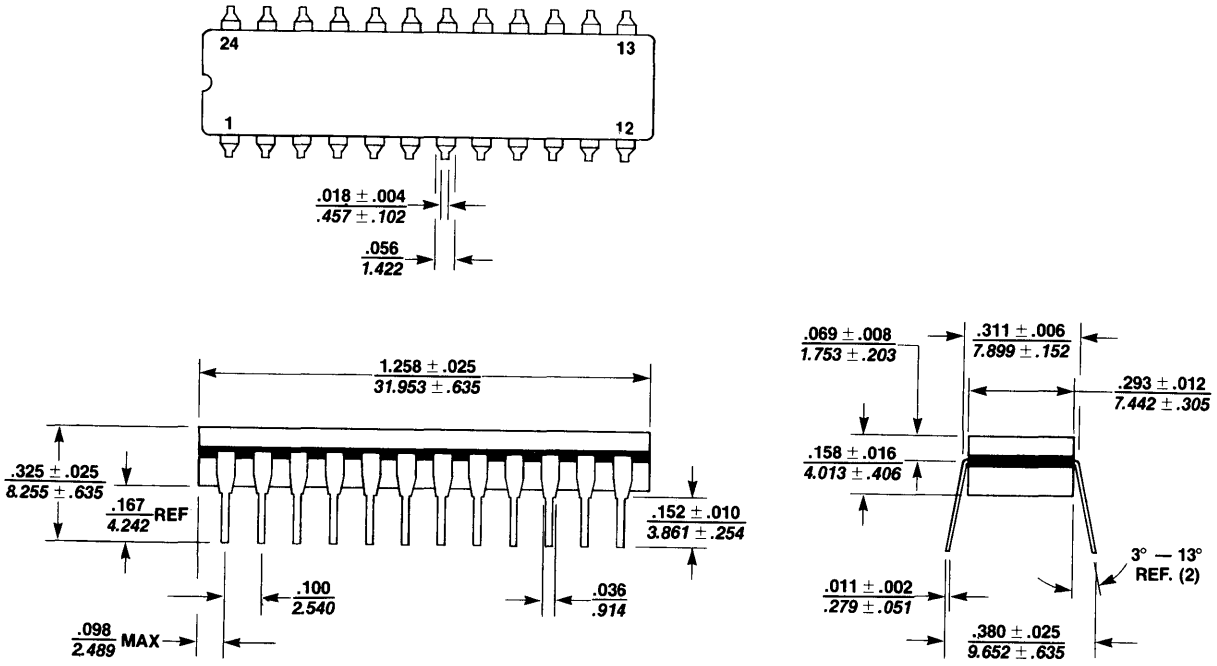
MANUFACTURER	PROGRAMMER TYPE	PROGRAMMING MODULE	SOCKET CONFIGURATION
Data I/O	Unipak Rev-V05 Unipak 2 Rev-V04	Family Code 18	Pinout Code 65

Metal Mask Layout



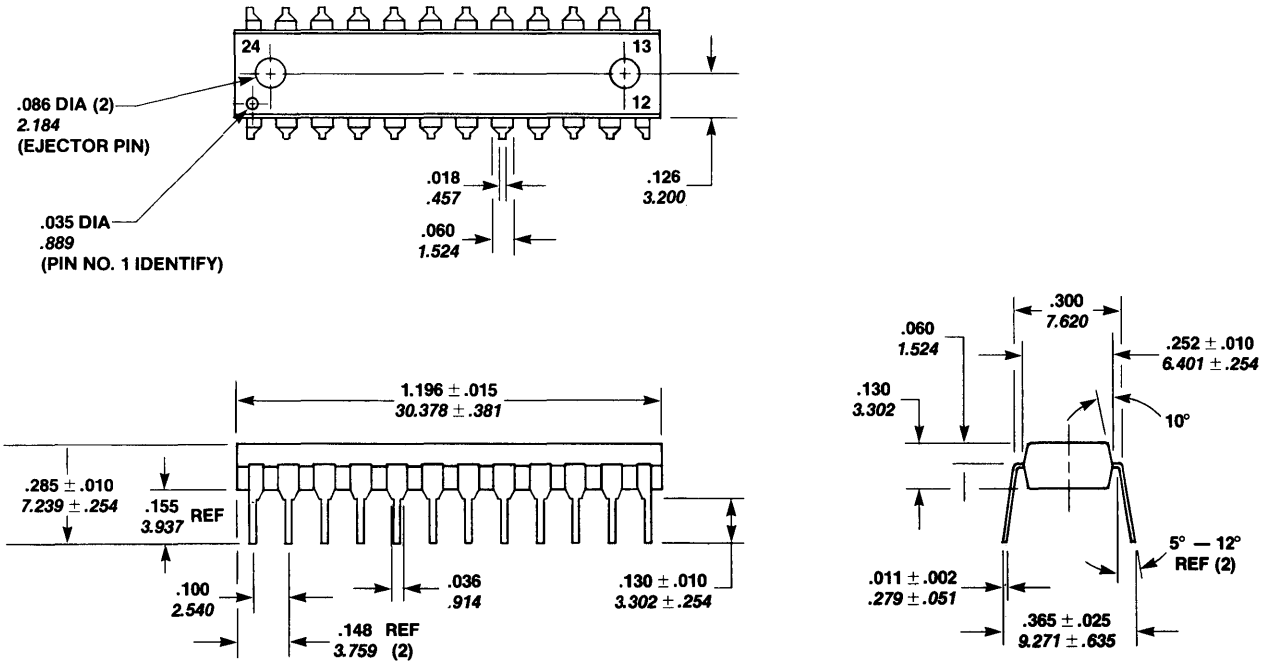
Package Drawings

J24S Ceramic SKINNYDIP



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

N24S Molded SKINNYDIP



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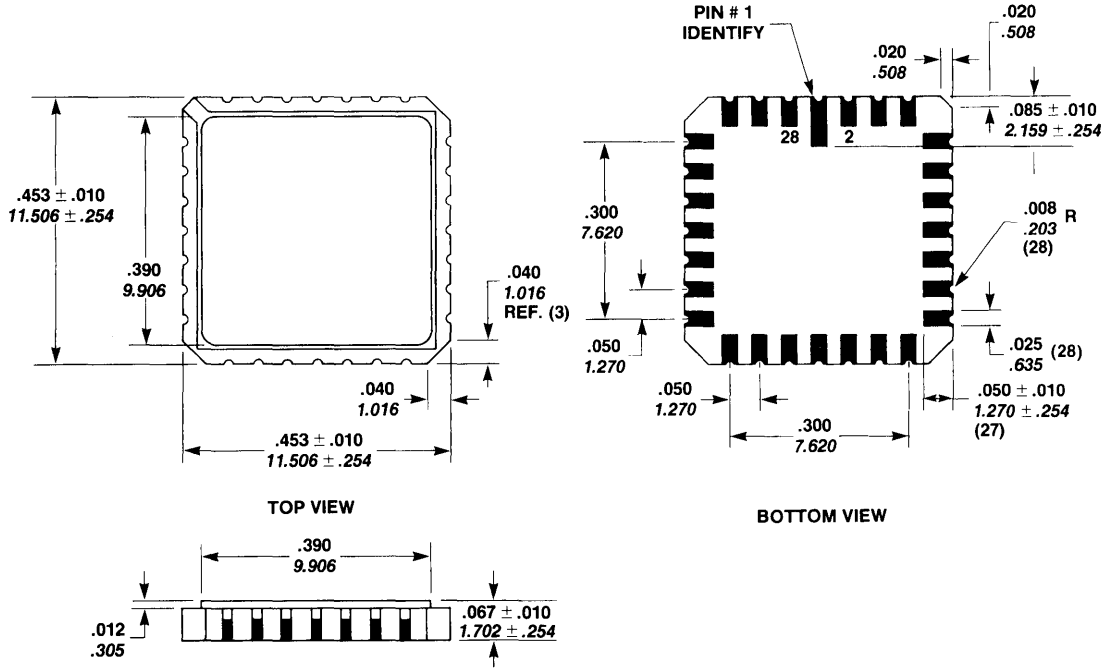
L28 Leadless Chip Carrier



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
3. Solder Fillets on Lid Edges Not Shown.

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