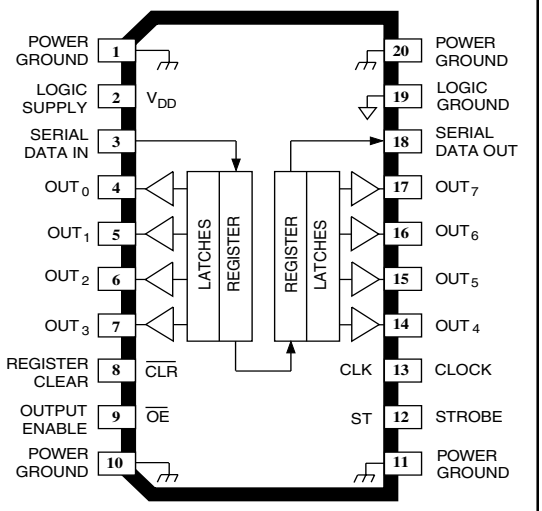
6595

Data Sheet
26185.120

ADVANCE INFORMATION
(Subject to change without notice)
January 24, 2000

8-BIT SERIAL-INPUT, DMOS POWER DRIVER



Dwg. PP-029-13

Note that the A6595KA (DIP) and the A6595KLW (SOIC) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS
at T_A = 25°C

Output Voltage, V_O ..... **50 V**
Output Drain Current,
Continuous, I_O ..... **250 mA***
Peak, I_{OM} ..... **750 mA*†**
Peak, I_{OM} ..... **2.0 A†**
Single-Pulse Avalanche Energy,
E_{AS} ..... **75 mJ**
Logic Supply Voltage, V_{DD} ..... **7.0 V**
Input Voltage Range,
V_I ..... **-0.3 V to +7.0 V**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range,
T_A ..... **-40°C to +125°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

* Each output, all outputs on.

† Pulse duration ≤ 100 µs, duty cycle ≤ 2%.

Caution: These CMOS devices have input static protection (Class 3) but are still susceptible to damage if exposed to extremely high static electrical charges.

The A6595KA and A6595KLW combine an 8-bit CMOS shift register and accompanying data latches, control circuitry, and DMOS power driver outputs. Power driver applications include relays, solenoids, and other medium-current or high-voltage peripheral power loads.

The serial-data input, CMOS shift register and latches allow direct interfacing with microprocessor-based systems. Serial-data input rates are over 5 MHz. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

A CMOS serial-data output enables cascade connections in applications requiring additional drive lines. Similar devices with reduced $r_{DS(on)}$ are available as the A6A595.

The A6595 DMOS open-drain outputs are capable of sinking up to 750 mA. All of the output drivers are disabled (the DMOS sink drivers turned off) by the OUTPUT ENABLE input high.

The A6595KA is furnished in a 20-pin dual in-line plastic package. The A6595KLW is furnished in a wide-body, small-outline plastic package (SOIC) with gull-wing leads. Copper lead frames, reduced supply current requirements, and low on-state resistance allow both devices to sink 150 mA from all outputs continuously, to ambient temperatures over 85°C.

FEATURES

- 50 V Minimum Output Clamp Voltage
- 250 mA Output Current (all outputs simultaneously)
- 1.3 Ω Typical $r_{DS(on)}$
- Low Power Consumption
- Replacements for TPIC6595N and TPIC6595DW

Always order by complete part number:

Part Number	Package	$R_{\theta JA}$	$R_{\theta JC}$
A6595KA	20-pin DIP	55°C/W	25°C/W
A6595KLW	20-lead SOIC	70°C/W	17°C/W

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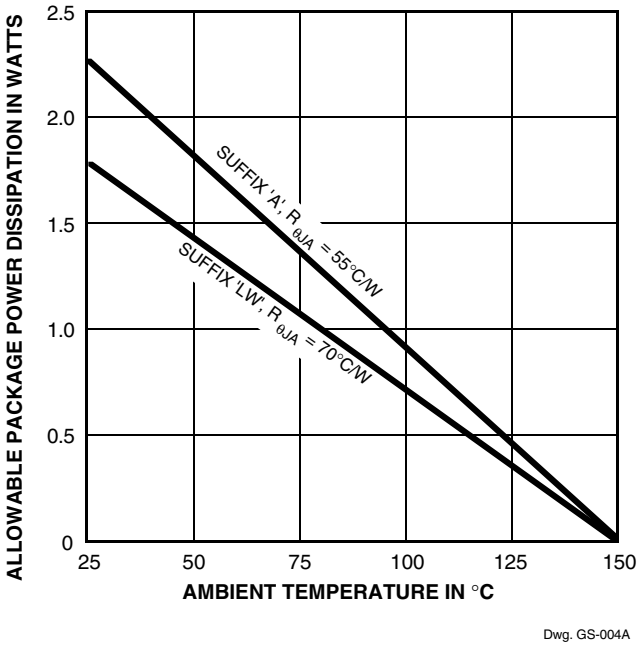
8-BIT SERIAL-INPUT, DMOS POWER DRIVER



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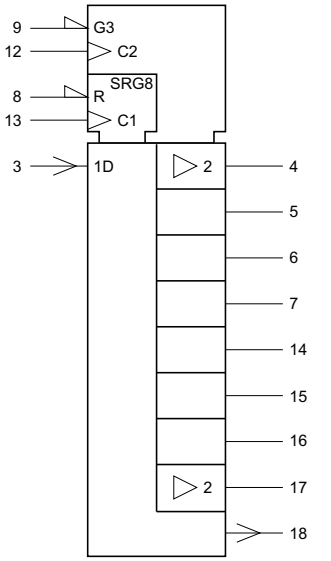
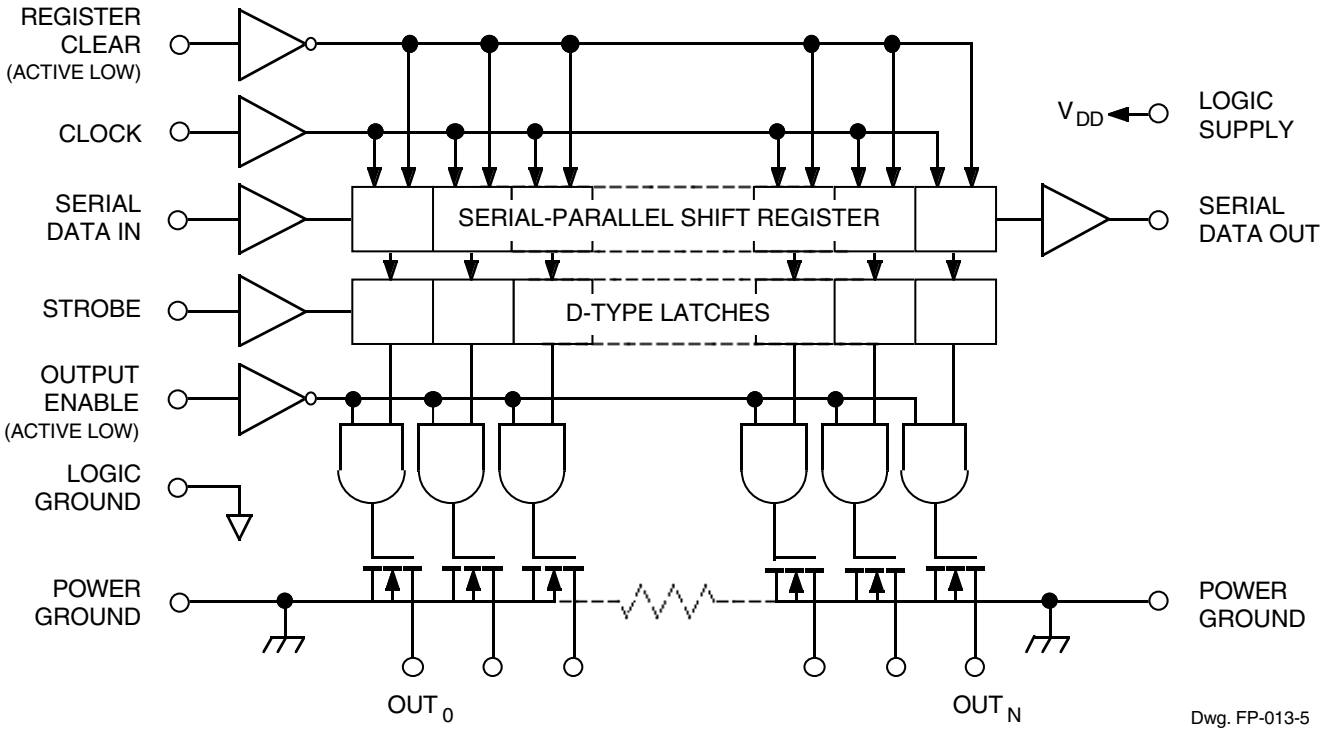
LOGIC SYMBOL



Dwg. FP-043

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-013-5

Grounds (terminals 1, 10, 11, 19, and 20) must be connected together externally.

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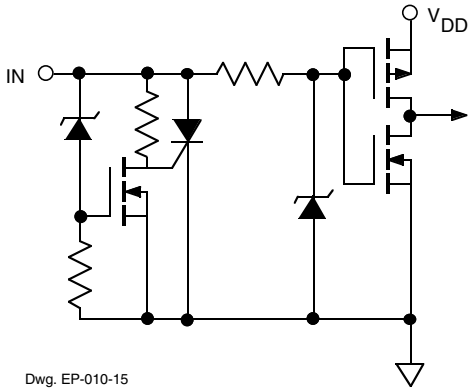
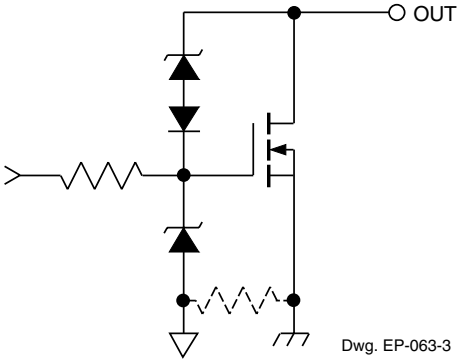


LOGIC INPUTS

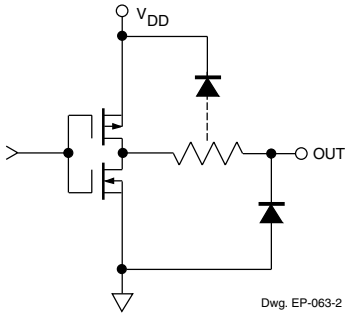


DMOS POWER DRIVER OUTPUT

RECOMMENDED OPERATING CONDITIONS

over operating temperature range

Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 5.5 V
High-Level Input Voltage, V_{IH} ..... $\geq 0.85V_{DD}$
Low-level input voltage, V_{IL} ..... $\leq 0.15V_{DD}$



SERIAL DATA OUT

TRUTH TABLE

Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe	Latch Contents						Output Enable	Output Contents					
		I_0	I_1	I_2	...	I_6	I_7			I_0	I_1	I_2	...	I_6	I_7		I_0	I_1	I_2	...	I_6	I_7
H	⌐	H	R_0	R_1	...	R_5	R_6	R_6														
L	⌐	L	R_0	R_1	...	R_5	R_6	R_6														
X	⌐	R_0	R_1	R_2	...	R_6	R_7	R_7														
		X	X	X	...	X	X	X	—	R_0	R_1	R_2	...	R_6	R_7							
		P_0	P_1	P_2	...	P_6	P_7	P_7	⌐	P_0	P_1	P_2	...	P_6	P_7	L	P_0	P_1	P_2	...	P_6	P_7
										X	X	X	...	X	X	H	H	H	H	...	H	H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, t_{ir} = t_{if} ≤ 10 ns (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Breakdown Voltage	$V_{(BR)DSX}$	I_O = 1 mA	50	—	—	V
Off-State Output Current	I_{DSX}	V_O = 40 V	—	0.05	1.0	µA
		V_O = 40 V, T_A = 125°C	—	0.15	5.0	µA
Static Drain-Source On-State Resistance	$r_{DS(on)}$	I_O = 250 mA, V_{DD} = 4.5 V	—	1.3	2.0	Ω
		I_O = 250 mA, V_{DD} = 4.5 V, T_A = 125°C	—	2.0	3.2	Ω
		I_O = 500 mA, V_{DD} = 4.5 V (see note)	—	1.3	2.0	Ω
Nominal Output Current	I_{ON}	$V_{DS(on)}$ = 0.5 V, T_A = 85°C	—	250	—	mA
Logic Input Current	I_{IH}	V_I = V_{DD} = 5.5 V	—	—	1.0	µA
	I_{IL}	V_I = 0, V_{DD} = 5.5 V	—	—	-1.0	µA
Logic Input Hysteresis	$V_{I(hys)}$		—	1.3	—	V
SERIAL-DATA Output Voltage	V_{OH}	I_{OH} = -20 µA, V_{DD} = 4.5 V	4.4	4.49	—	V
		I_{OH} = -4 mA, V_{DD} = 4.5 V	4.1	4.3	—	V
	V_{OL}	I_{OL} = 20 µA, V_{DD} = 4.5 V	—	0.002	0.1	V
		I_{OL} = 4 mA, V_{DD} = 4.5 V	—	0.2	0.4	V
Prop. Delay Time	t_{PLH}	I_O = 250 mA, C_L = 30 pF	—	650	—	ns
	t_{PHL}	I_O = 250 mA, C_L = 30 pF	—	150	—	ns
Output Rise Time	t_r	I_O = 250 mA, C_L = 30 pF	—	7500	—	ns
Output Fall Time	t_f	I_O = 250 mA, C_L = 30 pF	—	425	—	ns
Supply Current	$I_{DD(OFF)}$	All inputs low	—	15	100	µA
	$I_{DD(ON)}$	V_{DD} = 5.5 V, Outputs on	—	150	300	µA
	$I_{DD(fclk)}$	f_{clk} = 5 MHz, C_L = 30 pF, Outputs off	—	0.6	5.0	mA

Typical Data is at V_{DD} = 5 V and is for design information only.

NOTE — Pulse test, duration ≤100 µs, duty cycle ≤2%.

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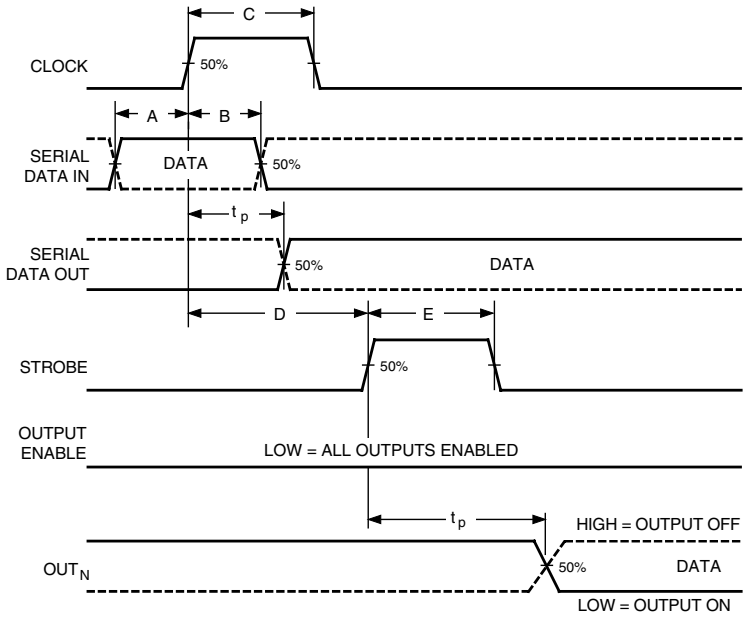
TIMING REQUIREMENTS and SPECIFICATIONS

(Logic Levels are V_{DD} and Ground)



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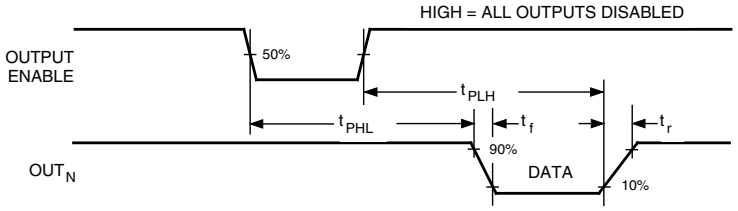


Dwg. WP-030-2

A. Data Active Time Before Clock Pulse (Data Set-Up Time), $t_{su(D)}$ ..... **10 ns**
B. Data Active Time After Clock Pulse (Data Hold Time), $t_{h(D)}$ ..... **10 ns**
C. Clock Pulse Width, $t_{w(CLK)}$ ..... **20 ns**
D. Time Between Clock Activation and Strobe, $t_{su(ST)}$ ..... **50 ns**
E. Strobe Pulse Width, $t_{w(ST)}$ ..... **50 ns**
F. Output Enable Pulse Width, $t_{w(OE)}$ ..... **4.5 µs**

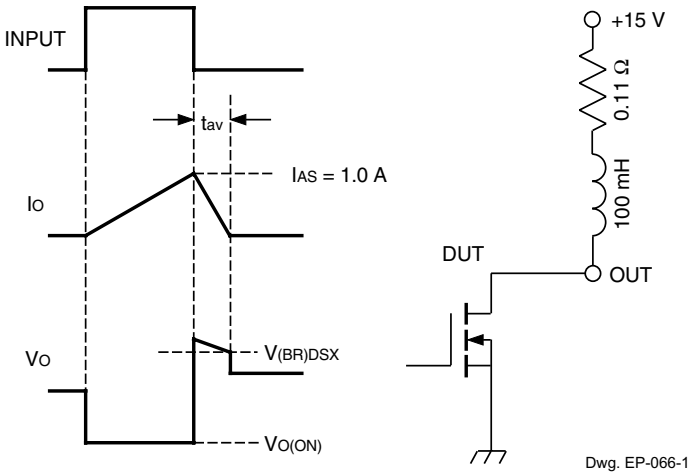
NOTE – Timing is representative of a 12.5 MHz clock. Higher speeds are attainable.

Serial data present at the input is transferred to the shift register on the rising edge of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT.

Information present at any register is transferred to the respective latch on the rising edge of the STROBE input pulse (serial-to-parallel conversion).

When the OUTPUT ENABLE input is high, the output source drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

TEST CIRCUITS



$$E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{AV}/2$$

Single-Pulse Avalanche Energy Test Circuit and Waveforms

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TERMINAL DESCRIPTIONS

Terminal No.	Terminal Name	Function
1	POWER GROUND	Reference terminal for output voltage measurements (OUT_{0-3}).
2	LOGIC SUPPLY	(V_{DD}) The logic supply voltage (typically 5 V).
3	SERIAL DATA IN	Serial-data input to the shift-register.
4-7	OUT_{0-3}	Current-sinking, open-drain DMOS output terminals.
8	CLEAR	When (active) low, the registers are cleared (set low).
9	OUTPUT ENABLE	When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
10	POWER GROUND	Reference terminal for output voltage measurements (OUT_{0-3}).
11	POWER GROUND	Reference terminal for output voltage measurements (OUT_{0-7}).
12	STROBE	Data strobe input terminal; shift register data is latched on rising edge.
13	CLOCK	Clock input terminal for data shift on rising edge.
14-17	OUT_{4-7}	Current-sinking, open-drain DMOS output terminals.
18	SERIAL DATA OUT	CMOS serial-data output to the following shift register.
19	LOGIC GROUND	Reference terminal for input voltage measurements.
20	POWER GROUND	Reference terminal for output voltage measurements (OUT_{4-7}).

NOTE — Grounds (terminals 1, 10, 11, 19, and 20) must be connected together externally.

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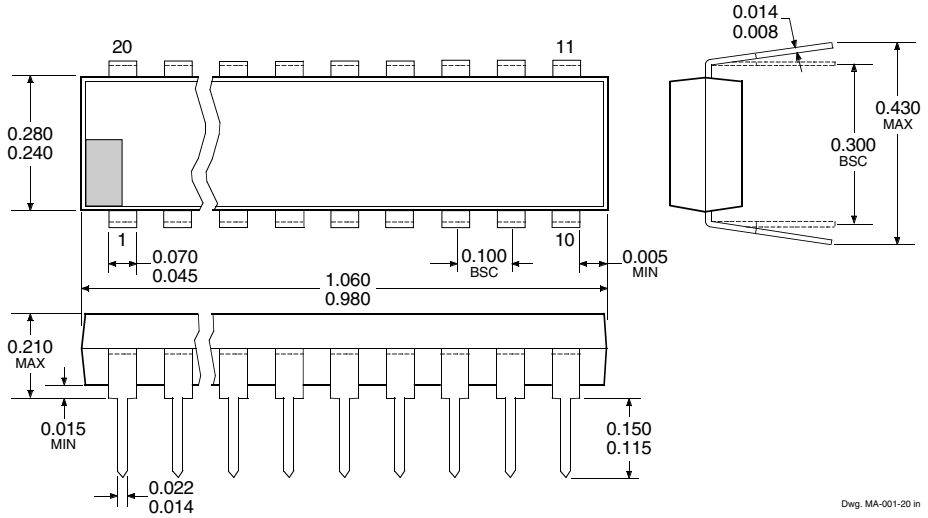
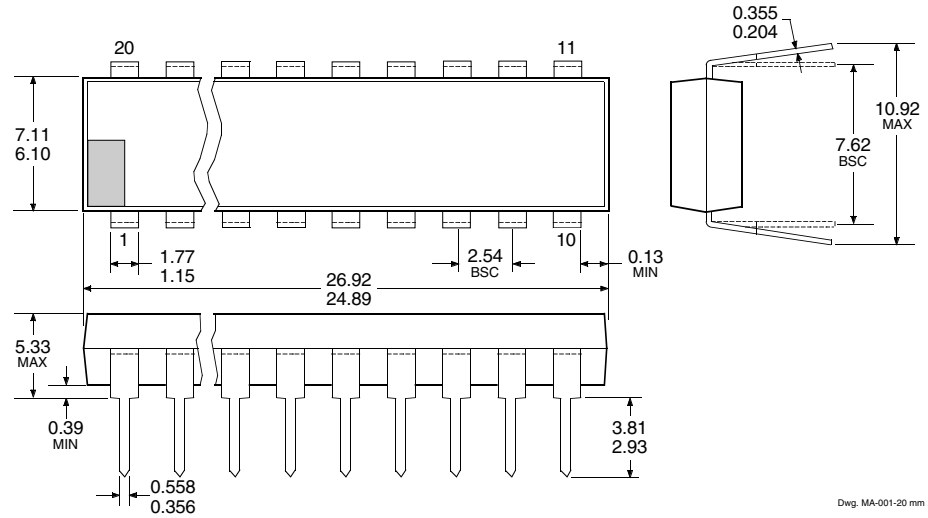
8-BIT SERIAL-INPUT, DMOS POWER DRIVER

A6595KA

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative
3. Lead thickness is measured at seating plane or below.

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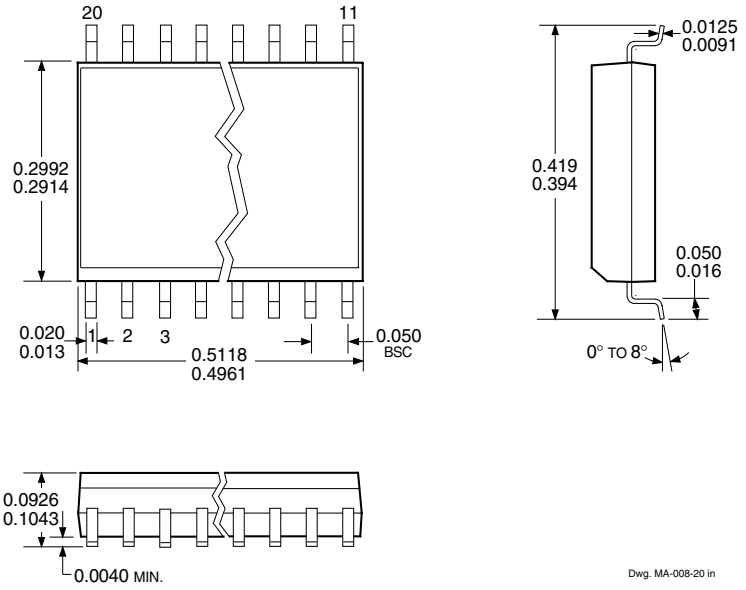
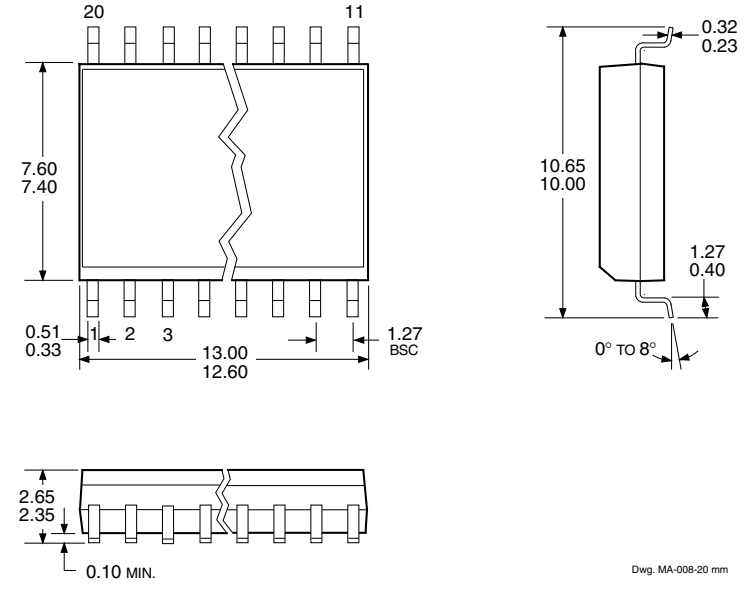
A6595KLW

Dimensions in Inches
(for reference only)



Dimensions in Millimeters
(controlling dimensions)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

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8-BIT SERIAL-INPUT, DMOS POWER DRIVER

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