9000 • 9001
9020 • 9022

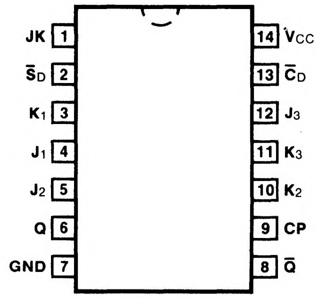
JK FLIP-FLOPS ('00, '01)
DUAL JK FLIP-FLOPS ('20, '22)

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Ceramic DIP (D)	A	9000DC	9000DM	6A
	B	9001DC	9001DM	
	C	9020DC	9020DM	6B
	D	9022DC	9022DM	
Flatpak (F)	A	9000FC	9000FM	3I
	B	9001FC	9001FM	
	C	9020FC	9020FM	4L
	D	9022FC	9022FM	

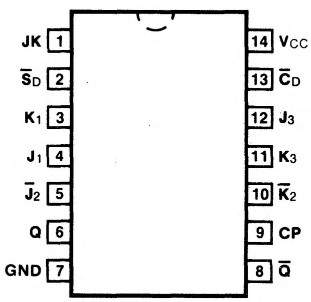
CONNECTION DIAGRAMS

PINOUT A



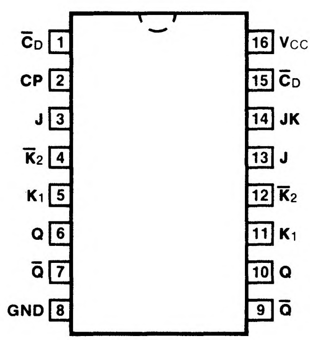
$J = A \bullet B \bullet C \bullet D$
$K = A \bullet B \bullet C \bullet D$

PINOUT B

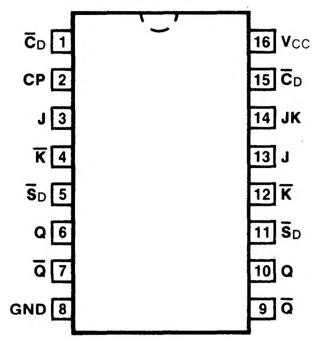


$J = A \bullet \overline{B} \bullet C \bullet D$
$K = A \bullet B \bullet \overline{C} \bullet D$

PINOUT C



PINOUT D

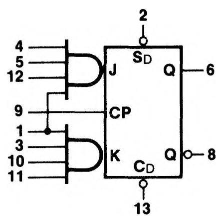


INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	9000 (U.L.) HIGH/LOW	9001 (U.L.) HIGH/LOW	9020 (U.L.) HIGH/LOW	9022 (U.L.) HIGH/LOW
JK	JK Input	3.0/2.0	3.0/2.0	6.0/4.0	6.0/4.0
J_n, K_n, $\overline{J}_n$, $\overline{K}_n$	Data Inputs	1.5/1.0	1.5/1.0	1.5/1.0	1.5/1.0
$\overline{CP}$	Clock Pulse Input	1.5/1.0	1.5/1.0	3.0/2.0	3.0/2.0
$\overline{C}_D$	Direct Clear Input	4.0/2.7	4.0/2.7	4.0/2.7	4.0/2.7
$\overline{S}_D$	Direct Set Input	4.0/2.7	4.0/2.7		4.0/2.7
Q, $\overline{Q}$	Outputs	30/8.8 (7.8)	30/8.8 (7.8)	30/8.8 (7.8)	30/8.8 (7.8)

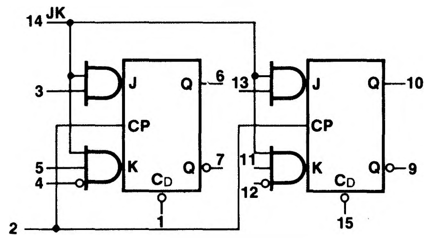
LOGIC SYMBOLS

9000



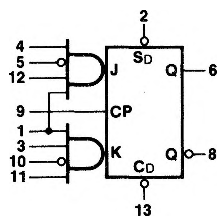
V_{CC} = Pin 14
GND = Pin 7

9020



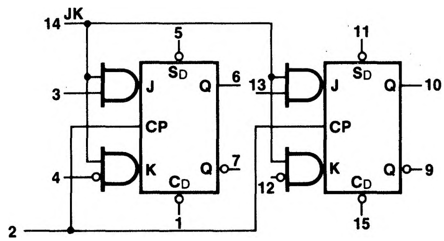
V_{CC} = Pin 16
GND = Pin 8

9001



V_{CC} = Pin 14
GND = Pin 7

9022



V_{CC} = Pin 16
GND = Pin 8

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS	
$\overline{S}_D$	$\overline{C}_D$	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	SYNCHRONOUS INPUTS CONTROL	

H = HIGH Voltage Level
L = LOW Voltage Level

SYNCHRONOUS OPERATION

BEFORE CLOCK				AFTER CLOCK	
OUTPUTS		INPUTS		OUTPUTS	
Q	$\overline{Q}$	J	K	Q	$\overline{Q}$
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

L* = Input does not go HIGH at any time while the clock is LOW.
H* = Input is HIGH at some time while the clock is LOW.
X = Immaterial

FUNCTIONAL DESCRIPTION — The TTL 9000 series has four flip-flops to satisfy the storage requirements of a logic system. All are master/slave JK designs and have the same high speed and high noise immunity as the rest of the 9000 series. As with the gates, all inputs have diode clamps to reduce ringing caused by long lines and impedance mismatches.

The JK type flip-flop was chosen for all flip-flop elements in this family because of its inherent logic power. The input function required to produce a given sequence of states for a JK flip-flop will, in general, contain more "don't care" conditions than the corresponding function for an RS flip-flop. These additional "don't care" conditions will, in most cases, reduce the amount of gating elements required to implement the input function.

The master/slave design offers the advantage of a dc threshold on the clock input initiating the transition of the outputs, so that careful control of clock pulse rise and fall times is not required.

Data is accepted by the master while the clock is in the LOW state. Refer to the truth tables for definition of HIGH and LOW data. Transfer from the master to the slave occurs on the LOW-to-HIGH transition of the clock. When the clock is HIGH, the J and K inputs are inhibited.

A joint (JK) input is provided for all flip-flops in this family. The common input removes the necessity of gating the clock signal with an external gate in many applications. This not only reduces package count, but also reduces the possibility of clock skew problems, since with internal gating provided, all flip-flops may be driven from a common clock line. Several TTL drivers may be used in parallel to drive this common clock line if the load exceeds the fan-out capability of the 9009 buffer.

The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided on all flip-flops except the 9020, which because of a logic trade-off has only clear inputs. The set or clear pin being LOW absolutely guarantees that one output will be HIGH, but if opposing data is present at the synchronous inputs and the flip-flop is clocked, the LOW output may momentarily spike HIGH synchronous with a positive transition of the clock. If the LOW output of the flip-flop is connected to other flip-flop inputs clocked from the same line, the spike will be masked by the clock. If the clock is suspended during the time when the asynchronous inputs are activated, no spike will occur. When the spikes can cause problems, a simple solution is to common the joint JK inputs with the synchronous set or reset signal.

Synchronous Operation — The truth table defines the next state of the flip-flop after a LOW-to-HIGH transition of the clock pulse. The next state is a function of the present state and the J and K inputs as shown in the table. The J and K inputs in the table refer to the basic flip-flop J and K inputs as indicated on the logic symbols. These internal inputs are for every flip-flop the result of a logic operation on the external J and K inputs. This operation is represented symbolically by AND gates in the logic symbol for each flip-flop. Logic symbols are in accordance with MIL Standard 806B.

The L* symbol in the J and K input column is defined as meaning that **input does not go HIGH at any time while the clock is LOW.**

The H* symbol in the J or K input column is defined as meaning that the **input is HIGH at some time while the clock is LOW.**

The X symbol indicates that the condition of that input has no effect on the next state of the flip-flop.

The H and L symbols refer to steady state HIGH and LOW voltage levels, respectively.

Unused Inputs — The 9001, 9020 and 9022 all have active level LOW synchronous inputs. When not in use they must be grounded. All other unused inputs, including asynchronous, should be tied HIGH for maximum operating speed.

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

SYMBOL	PARAMETER	0°C		25°C		75°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16 mA
I_{IL}	Input LOW Current							mA	V_{CC} = 5.25 V V_{IN} = 0.45 V 5.25 V on Other Inputs
	All J, K Inputs		-1.60		-1.60		-1.60		
	CP Inputs 9000, 9001								
	JK Inputs 9000, 9001		-3.20		-3.20		-3.20		
	CP Inputs 9020, 9022								
	JK inputs 9020, 9022		-6.40		-6.40		-6.40		
	$\overline{S}_D$, $\overline{C}_D$ (all Flip-flops)		-4.32		-4.32		-4.32		
	Input LOW Current							mA	V_{CC} = 4.75 V V_{IN} = 0.45 V 5.25 V on Other Inputs
	All J, K Inputs		-1.41		-1.41		-1.41		
	CP Inputs 9000, 9001								
	JK Inputs 9000, 9001		-2.82		-2.82		-2.82		
	CP Inputs 9020, 9022								
	JK Inputs 9020, 9022		-5.64		-5.64		-5.64		
	$\overline{S}_D$, $\overline{C}_D$ (all Flip-flops)		-3.78		-3.78		-3.78		
I_{CC}	Power Supply Current							mA	
	9000		28		28		28		$\overline{S}_D$ at Gnd
	9001		33		33		33		$\overline{S}_D$ at Gnd
	9020, 9022 each Flip-flop		30		30		30		$\overline{C}_{D1}$, $\overline{C}_{D2}$ at Gnd

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V ±10%

SYMBOL	PARAMETER	-55°C		25°C		125°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.8		0.9		0.8	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12.4 mA V_{CC} = 5.5 V, I_{OL} = 16 mA

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: (Cont'd)

SYMBOL	PARAMETER	-55°C Min	-55°C Max	25°C Min	25°C Max	125°C Min	125°C Max	UNITS	CONDITIONS
I_{IL}	Input LOW Current								
	All J, K Inputs		-1.60		-1.60		-1.60		
	CP Inputs 9000, 9001								V_{CC} = 5.5 V
	JK Inputs 9000, 9001		-3.20		-3.20		-3.20	mA	V_{IN} = 4.5 V
	CP Inputs 9020, 9022								5.5 V on
	JK Inputs 9020, 9022		-6.40		-6.40		-6.40		Other Inputs
	$\overline{S}_D$, $\overline{C}_D$ (all Flip-flops)		-4.32		-4.32		-4.32		
	Input LOW Current								
	All J, K Inputs		-1.24		-1.24		-1.24		
	CP Inputs 9000, 9001								V_{CC} = 4.5 V
	JK Inputs 9000, 9001		-2.48		-2.48		-2.48	mA	V_{IN} = 0.4 V
	CP Inputs 9020, 9022								5.5 V on
	JK Inputs 9020, 9022		-4.96		-4.96		-4.96		Other Inputs
	$\overline{S}_D$, $\overline{C}_D$ (all Flip-flops)		-3.35		-3.75		-3.35		
I_{CC}	Power Supply Current								
	9000		24		24		24		$\overline{S}_D$ at Gnd
	9001		28		28		28	mA	$\overline{S}_D$ at Gnd
	9020, 9022 each Flip-flop		27		27		27		$\overline{C}_{D1}$, $\overline{C}_{D2}$, at Gnd

SWITCHING CHARACTERISTICS (T_A = 25° C, V_{CC} = 5.0 V, C_L = C_1 = 15 pF of all flip-flops unless otherwise noted)

SYMBOL	PARAMETER			LIMITS Min	LIMITS Max	UNITS	CONDITIONS
t_{PLH}	Clock to Output				20	ns	Figs. a, b, c
	$\overline{S}_D$ or $\overline{C}_D$ to Output				20		
t_{PHL}	Clock to Output				30	ns	
	$\overline{S}_D$ or $\overline{C}_D$ to Output				35		
t_{setup}	J, K or JK	9000XM		30		ns	Figs. a, c
		9000XC		35			
		9001XM, 9020XM, 9022XM		10		ns	Figs. a, b, c
		9001XC, 9020XC, 9022XC		15			
	$\overline{J}$ or $\overline{K}$ Data Entry			17			
$t_{release}$	J, K or JK	9000 only			10	ns	Figs. a, c
		9001, 9020, 9022			1.0	ns	Figs. a, b, c
	$\overline{J}$ or $\overline{K}$ Data Entry				4.0		
Pulse Widths	Clock	9000 only	Positive	20*		ns	Figs. a, c
			Negative	25*			
		9001, 9020, 9022	Positive	8.0*		ns	Figs. a, b, c
			Negative	10*			
	$\overline{S}_D$ or $\overline{C}_D$		Negative	25*			
	Toggle Frequency		9000 only	20*		MHz	Figs. a, c
			9001, 9020, 9022	50*		MHz	Figs. a, b, c

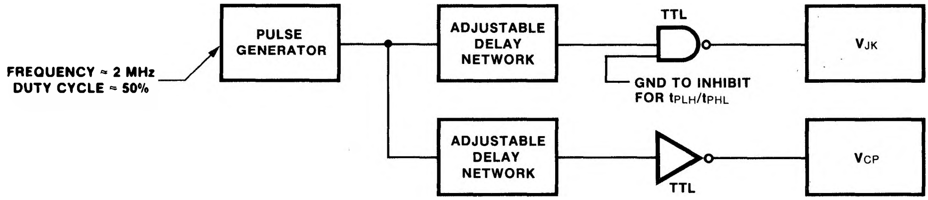
*Typical Value

SWITCHING TEST NOTES

t_{PLH} and t_{PHL}

1. V_{JK} should be kept at the HIGH level when performing t_{PLH}/t_{PHL} test.
2. Drive the clock pulse input with a suitable pulse source. t_{PLH} and t_{PHL} delays are as defined in the waveforms.

RECOMMENDED INPUT PULSE SOURCES



DTL9932 gates with adjustable capacitors connected from extender inputs to ground make suitable delay elements.

t_{setup}

1. t_{setup} is defined as the minimum time required for a HIGH to be present at a synchronous logic input at any time during the LOW state of the clock in order for the flip-flop to respond to the data.
2. The test for t_{setup} is performed by adjusting the timing relationship between the V_{CP} and V_{JK} inputs to the t_{setup} minimum value. A device that passes the test will have the output waveform shown. The output of a device that does not pass the t_{setup} test will remain at a static logic level (no switching will occur).

$t_{release}$

1. $t_{release}$ is defined as the maximum time allowed for a HIGH to be present at a synchronous logic input at any time during the LOW state of the clock and not be recognized.
2. The test for $t_{release}$ is performed by adjusting the timing relationship between V_{CP} and V_{JK} to the $t_{release}$ maximum value. The outputs of devices that pass will remain at static logic levels. In order to check both J and K sides of the flip-flop it is necessary to perform the test with the flip-flop in each of its two possible states, i.e., set and clear. This can be accomplished by making use of the appropriate direct inputs to establish the state before a test. The outputs of devices that do not pass the $t_{release}$ test will exhibit pulses instead of static levels.

SWITCHING TEST CIRCUITS

9000/9001

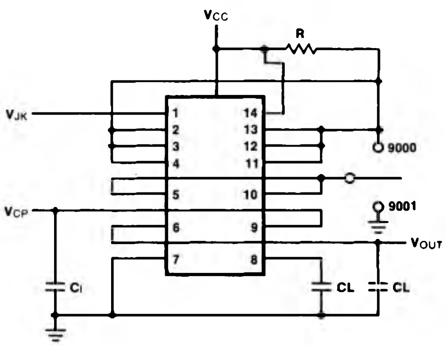


Fig. a

9020/9022

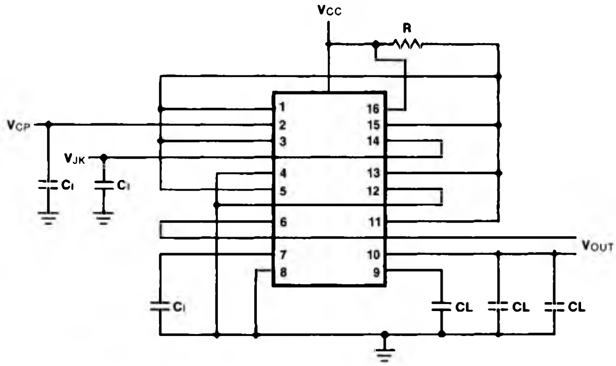


Fig. b

V_{CC} = Pin 5.0 V
R = 2.0 kΩ
C_I = C_L = 15 pF including probe and jig capacitance

WAVEFORM

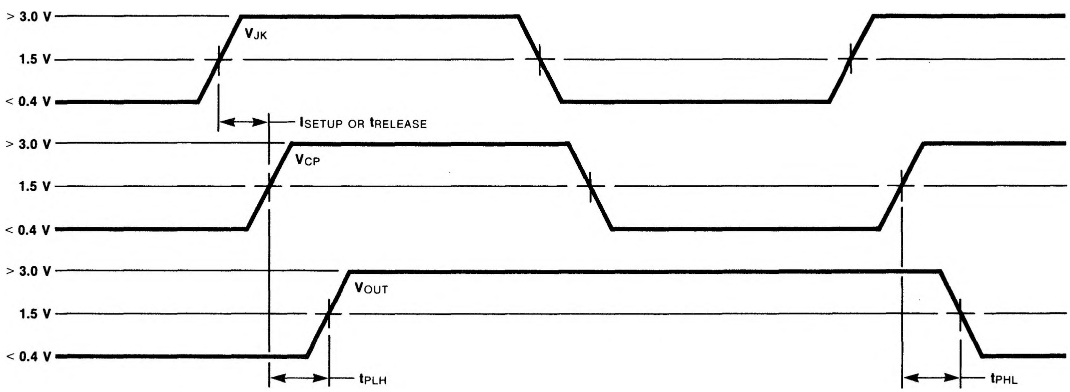


Fig. c