

Integrated Triple High-Side Switch with Embedded MCU and LIN Serial Communication for Relay Drivers

THERMAL ADDENDUM

Introduction

This thermal addendum is provided as a supplement to the MM908E624 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

Packaging and Thermal Considerations

The MM908E624 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2 . This results in two junction temperatures, T_{J1} and T_{J2} , and a thermal resistance matrix with $R_{\theta JA mn}$.

For $m, n = 1$, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1 .

For $m = 1, n = 2$, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2 . This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 1. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [$^{\circ}\text{C}/\text{W}$]		
	$m = 1, n = 1$	$m = 1, n = 2$ $m = 2, n = 1$	$m = 2, n = 2$
$R_{\theta JA mn}$ ⁽¹⁾⁽²⁾	40	31	36
$R_{\theta JB mn}$ ⁽²⁾⁽³⁾	25	16	21
$R_{\theta JA mn}$ ⁽¹⁾⁽⁴⁾	57	47	52
$R_{\theta JC mn}$ ⁽⁵⁾	21	12	16

Notes:

- Per JEDEC JESD51-2 at natural convection, still air condition.
- 2s2p thermal test board per JEDEC JESD51-7 and JESD51-5.
- Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
- Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
- Thermal resistance between the die junction and the exposed pad, "infinite" heat sink attached to exposed pad.

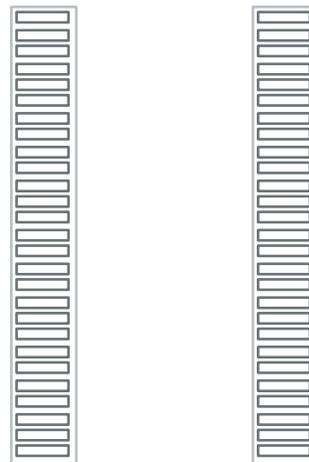
908E624ACDWB

**54-TERMINAL
SOICW**



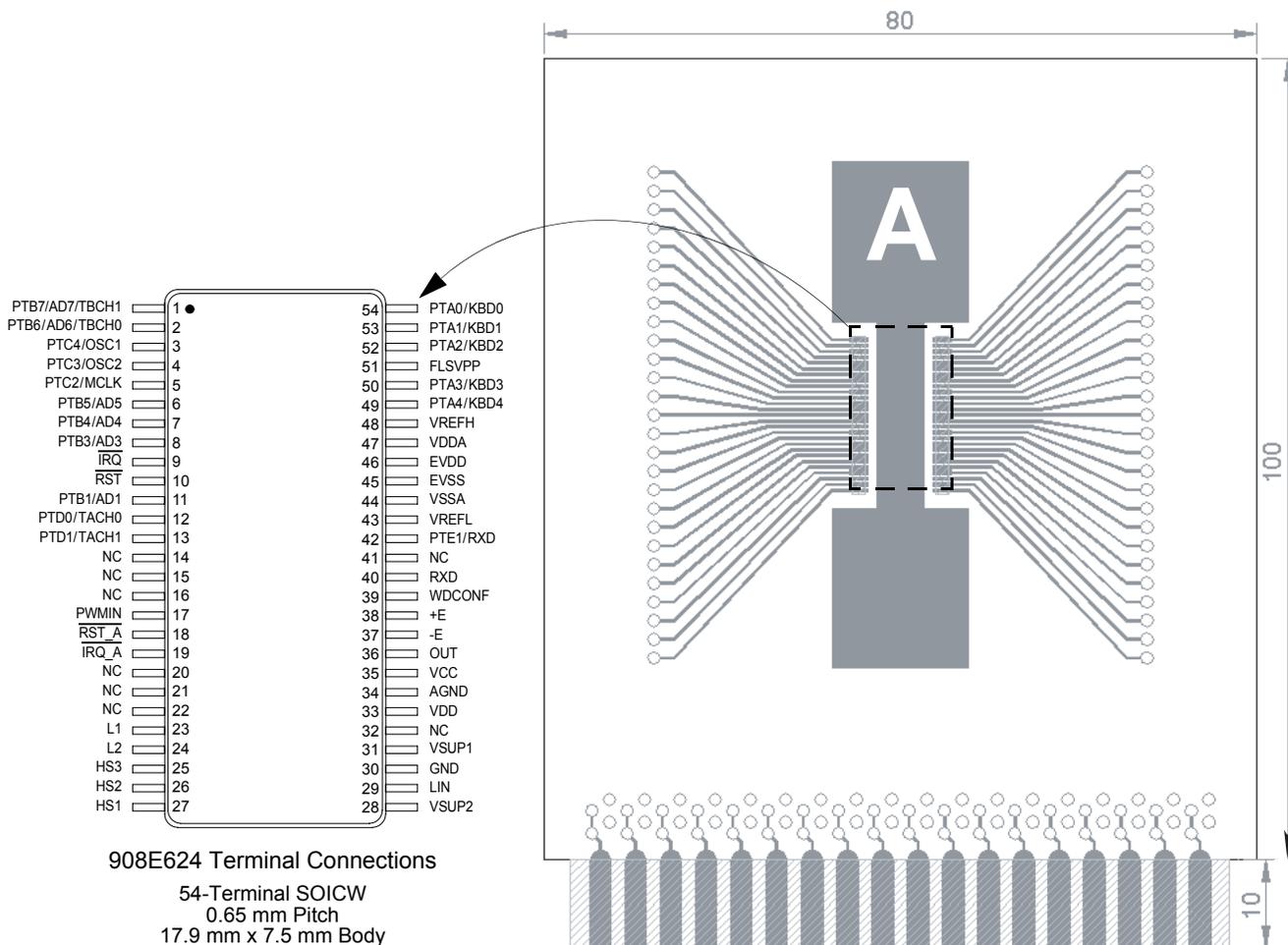
**DWB SUFFIX
EW (Pb-FREE) SUFFIX
98ASA99294D
54-TERMINAL SOICW**

Note For package dimensions, refer to the MM908E624 datasheet.



54 Terminal SOIC
0.65 mm Pitch
17.9 mm x 7.5 mm Body

Figure 1. Surface Mount for SOIC Wide Body non-Exposed Pad



Device on Thermal Test Board

- Material:** Single layer printed circuit board
 FR4, 1.6 mm thickness
 Cu traces, 0.07 mm thickness
- Outline:** 80 mm x 100 mm board area,
 including edge connector for thermal testing
- Area A:** Cu heat-spreading areas on board surface
- Ambient Conditions:** Natural convection, still air

Table 2. Thermal Resistance Performance

Terminal Resistance	Area A (mm ²)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		<i>m</i> = 1, <i>n</i> = 1	<i>m</i> = 1, <i>n</i> = 2 <i>m</i> = 2, <i>n</i> = 1	<i>m</i> = 2, <i>n</i> = 2
$R_{\theta JA mn}$	0	58	48	53
	300	56	46	51
	600	54	45	50

$R_{\theta JA mn}$ is the thermal resistance between die junction and ambient air.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

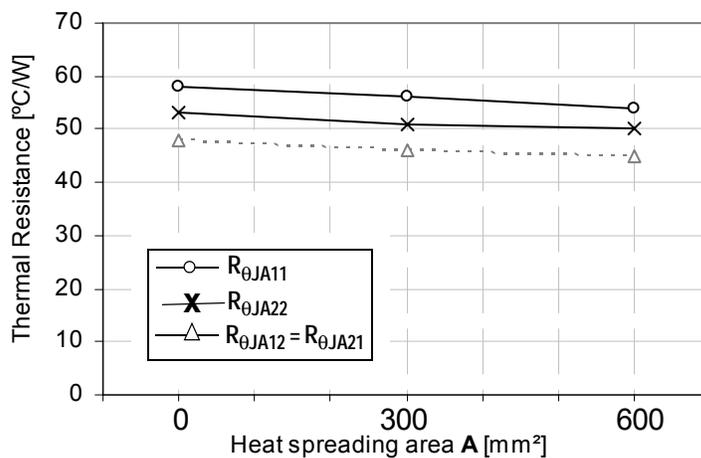


Figure 2. Device on Thermal Test Board $R_{\theta JA}$

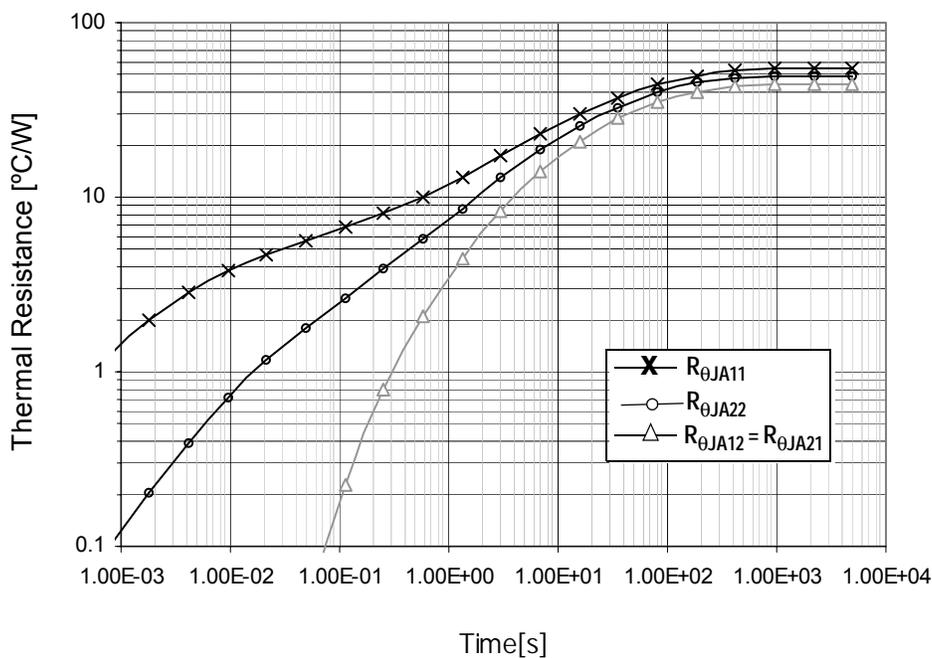


Figure 3. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response) Device on Thermal Test Board Area A = 600 (mm²)

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