9313

8-INPUT MULTIPLEXER

(With Open-Collector Output)

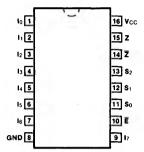
DESCRIPTION — The '13 is an 8-input multiplexer with open-collector output. It has the same pinning and logic configuration as the '12, but with an open-collector \overline{Z} output which allows for easy expansion of input terms. The device can select one bit of data from up to eight sources. The '13 has an active LOW enable and internal select decoding.

- PIN FOR PIN REPLACEMENT FOR THE SIGNETICS 8231
- SAME PINNING AND LOGIC CONFIGURATION AS THE 9312
 BUT WITH OPEN-COLLECTOR OUTPUT
- OPEN-COLLECTOR OUTPUT Z FOR EASY EXPANSION OF INPUT TERMS (WIRED-OR APPLICATIONS)
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED Z OUTPUT

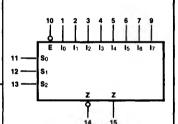
ORDERING CODE: See Section 9

	PIN	COMMERCIAL GRADE	MILITARY GRADE	PKG	
PKGS	ОПТ	$V_{CC} = +5.0 \text{ V } \pm 5\%,$ $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$	$V_{CC} = +5.0 \text{ V} \pm 10\%,$ $T_A = -55^{\circ}\text{ C to} + 125^{\circ}\text{ C}$	TYPE	
Plastic DIP (P)	A	9313PC		9B	
Ceramic DIP (D)	A	9313DC	9313DM	6B	
Flatpak (F)	A	9313FC	9313FM	4L	

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16 GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
<u>S</u> 0 - S2	Select Inputs	1.0/1.0
Ē	Enable Input (Active LOW)	1.0/1.0
lo — I7	Multiplexer Inputs	1.0/1.0
Z	Multiplexer Output	20/10
Ī*	Complementary Multiplexer Output	OC**/10

^{*}An external pull-up resistor is needed to provide HIGH level drive capability. This output will sink a maximum of 16 mA at V_{OUT} = 0.4 V.
**OC — Open Collector

FUNCTIONAL DESCRIPTION — The '13 is a logical implementation of a single pole, eight-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . An open-collector output \overline{Z} is provided for easy expansion of input terms. Also a fully buffered Z output is available. The Enable Input (\overline{E}) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

The '13 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the '13 can provide any logic functions of four variables and its negation.

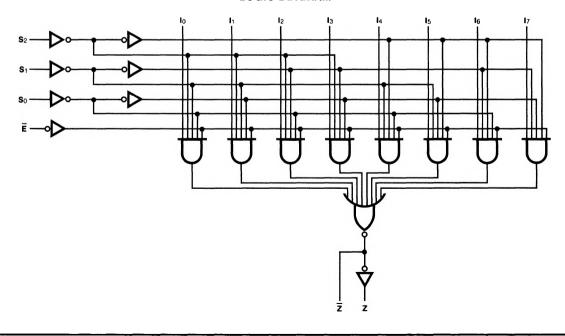
TRUTH TABLE

INPUTS			OUT	PUTS	
E	S ₂	S ₁	S ₀	Z	Z
ILLL	X L L	X L L	XLHL	H 0 1 1 2	L 0 1 2
	_ IIII	HLLHH	ILILI	13 14 15 16 17	3 4 5 6 7

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS	
		Min	Max	OMITS	CONDITIONS	
Іон	Output HIGH Current, Z	=	150	μΑ	$V_{CC}=4.5$ V, $V_{OUT}=4.5$ V, $V_{IN}=0.6$ V on Data Input, V_{IN} (\overline{E} & S_n Inputs) = V_{IL} or V_{IH} per Truth Table	
los	Output Short Circuit Current, Z	-20	-70	mA	V _{CC} = Max, V _{OUT} = 0 V	
Icc	Power Supply Current		47	mA	V _{CC} = Max, I ₀ — I ₇ = Gnd	

AC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^{\circ}\text{C}$ (See Section 3 for waveforms and load configurations)

SYMBOL		93XX C _L = 15 pF		UNITS	CONDITIONS
	PARAMETER				
		Min	Max	1	
tPLH tPHL	Propagation Delay S ₀ to Z		34 34	ns	Figs. 3-1, 3-20
tPLH tPHL	Propagation Delay S_0 to \overline{Z}		29 28	ns	Figs. 3-2, 3-20 $R_L = 400 \Omega$
tPLH tPHL	Propagation Delay I ₀ to Z		30 30	ns	Figs. 3-1, 3-5
tPLH tPHL	Propagation Delay I ₀ to Z		26 24	ns	Figs. 3-2, 3-4 R _L = 400 Ω
tpLH tpHL	Propagation Delay E to Z		34 36	ns	Figs. 3-1, 3-4
tpLH tpHL	Propagation Delay E to Z		27 29	ns	Figs. 3-2, 3-5 R _L = 400 Ω