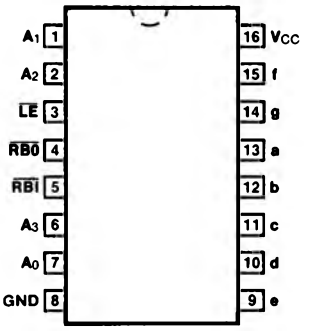
9368

7-SEGMENT DECODER/DRIVER/LATCH

(Constant Current Source Outputs)

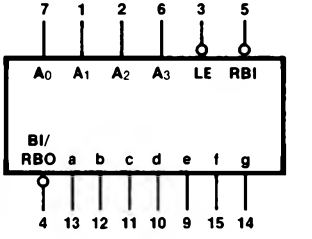
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '68 is a 7-segment decoder driver incorporating input latches and constant current output circuits to drive common cathode type LED displays directly.

- **HIGH SPEED INPUT LATCHES FOR DATA STORAGE**
- **DRIVES COMMON CATHODE LED DISPLAYS SUCH AS FND357 OR FND500 DIRECTLY**
- **ACTIVE LOW LATCH ENABLE FOR EASY INTERFACE WITH MSI CIRCUITS**
- **HEXADECIMAL DECODE FORMAT**
- **LATCH SPEED COMPARABLE TO STANDARD MSI LATCHES**
- **DATA INPUT FAN-IN ZERO WHEN LATCH NOT ENABLED**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZEROS**
- **PINOUTS COMPARABLE WITH OTHER STANDARD MSI DECODERS SUCH AS 9307, 9317, 7446, 7447, 7448**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	PKG TYPE
Plastic DIP (P)	A	9368PC	9B
Ceramic DIP (D)	A	9368DC	6B

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$A_0 - A_3$	Address (Data) Inputs	2.0/1.0*
$\overline{LE}$	Latch Enable Input (Active LOW)	1.0/1.0
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	1.0/1.0
$\overline{RBO}$	Ripple Blanking as Output (Active LOW)	-/2.0
	as Input (Active LOW)	-/2.0
a — g	Segment Outputs (Active HIGH)	20 mA/"OFF"

*Except Loadings is 100 μA at 0.4 V when $\overline{LE}$ is HIGH.

FUNCTIONAL DESCRIPTION — The '68 is a 7-segment decoder driver designed to drive 7-segment common cathode LED displays such as the Fairchild FND357 or FND500 directly. The '68 drives any common cathode LED display rated at a nominal 20 mA at 1.7 V per segment without need for current limiting resistors.

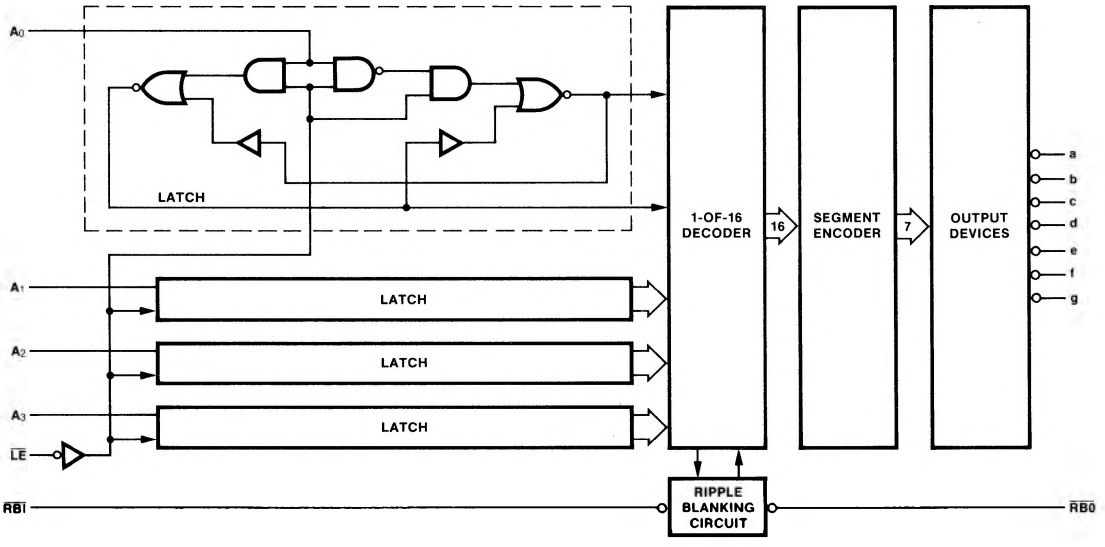
This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a hexadecimal decode format which produces numeric codes "0" thru "9" and alpha codes "A" thru "F" using upper and lower case fonts.

Latches on the four data inputs are controlled by an active LOW latch enable $\overline{LE}$. When the $\overline{LE}$ is LOW, the state of the outputs is determined by the input data. When the $\overline{LE}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{LE}$ pulse width necessary to accept and store data is typically 30 ns which allows data to be strobed into the '68 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

Another feature of the '68 is that the unit loading on the data inputs is very low (-100 μA Max) when the latch enable is HIGH. This allows '68s to be driven from an MOS device in multiplex mode without the need for drivers on the data lines.

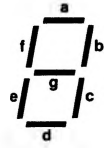
The '68 also has provision for automatic blanking of the leading and/or trailing edge zeros in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeros. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

LOGIC DIAGRAM



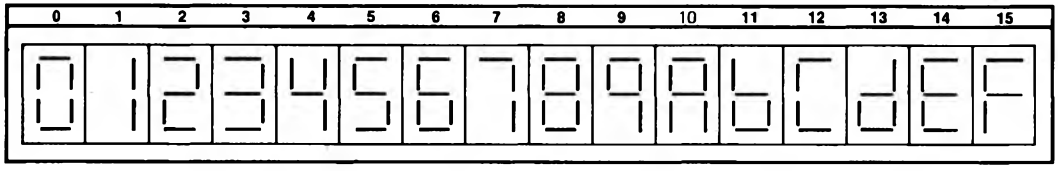
TRUTH TABLE

BINARY STATE	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	a	b	c	d	e	f	g	$\overline{RBO}$	
—	H	*	X	X	X	X	◄ STABLE ►							H	STABLE
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	L	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	H	H	10
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	11
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	12
13	L	X	H	H	L	H	L	H	H	H	H	L	H	H	13
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	14
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	15
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L**	BLANK

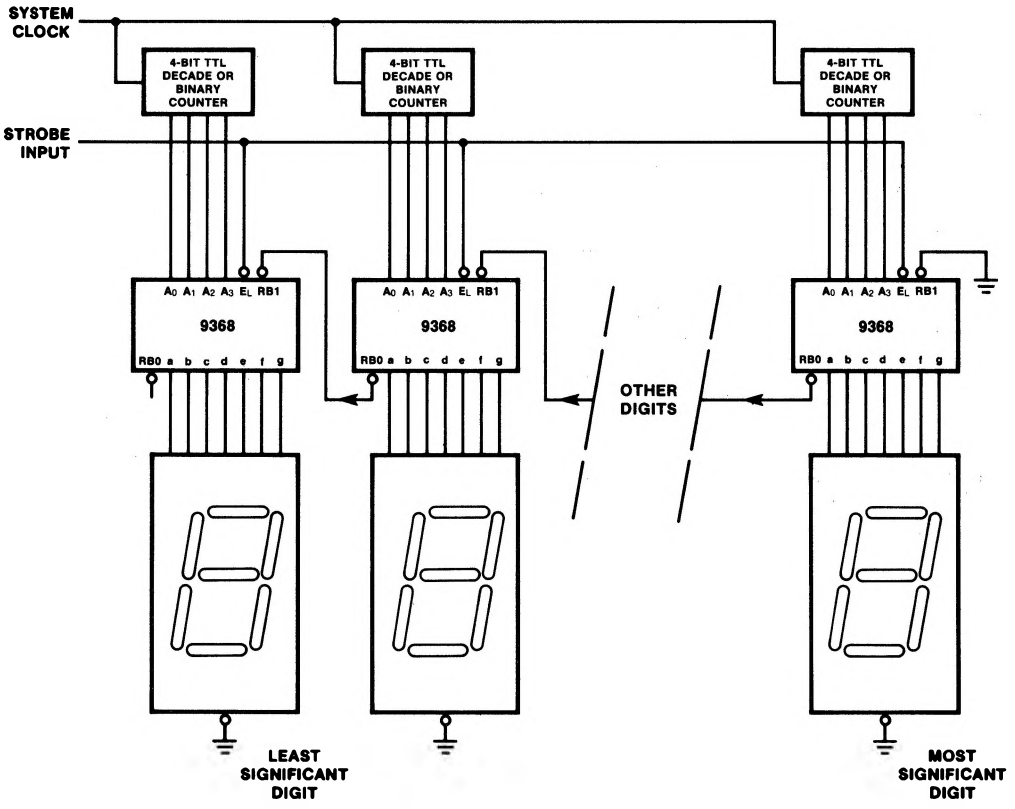


*The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
**The $\overline{RBO}$ used as an input overrides all other input conditions.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NUMERICAL DESIGNATIONS

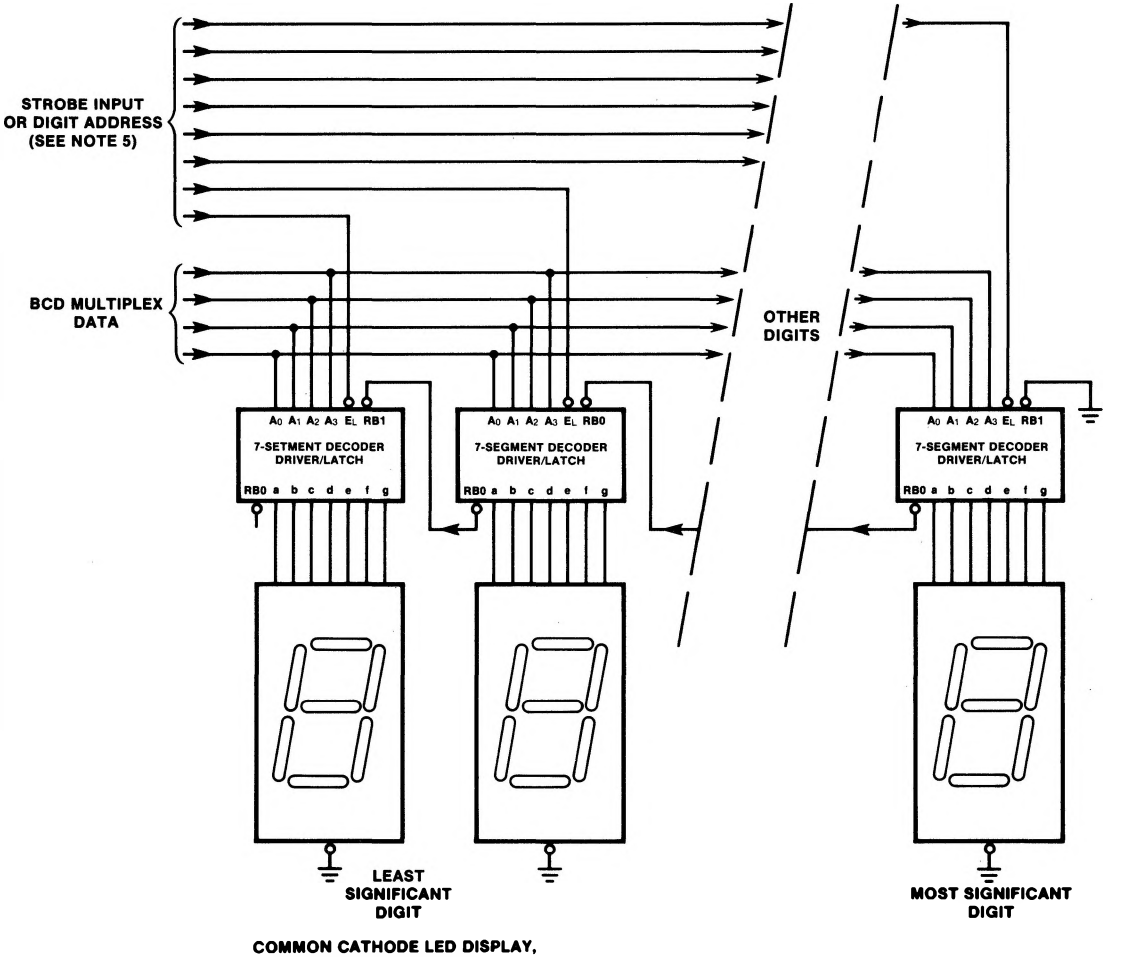


PARALLEL DATA DISPLAY SYSTEM WITH RIPPLE BLANKING



COMMON CATHODE LED DISPLAY,
SUCH AS FAIRCHILD FND357
OR FND500

DISPLAY DEMULTIPLEXING SYSTEM WITH RIPPLE BLANKING



**COMMON CATHODE LED DISPLAY,
SUCH AS FAIRCHILD FND357
OR FND500**

NOTE:
Digit address data must be non-overlapping. Standard TTL decoders like the 9301, 9311, 7442 or 74155 must be strobed, since the address decoding glitches could cause erroneous data to be strobed into the latches.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I_{OH}	Segment Output HIGH Current	-16	-22	mA	V_{CC} = 5.0 V, V_{OUT} = 1.7 V, T_A = +25°C
I_{OL}	Segment Output LOW Current	-250	250	μA	V_{CC} = 5.0 V, V_{OUT} = 1.7 V
I_{CC}	Power Supply Current		67	mA	V_{CC} = Max, Outputs Open, Data & Latch Inputs = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF R_L = 100 Ω		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to a—g		50 75	ns	Fig. 3-21
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to a—g		70 90	ns	Fig. 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH A_n to $\overline{LE}$	30		ns	Fig. 3-13
t_h (H)	Hold Time HIGH A_n to $\overline{LE}$	0		ns	Fig. 3-13
t_s (L)	Setup Time LOW A_n to $\overline{LE}$	20		ns	Fig. 3-13
t_h (L)	Hold Time LOW A_n to $\overline{LE}$	0		ns	Fig. 3-13
t_w (L)	$\overline{LE}$ Pulse Width LOW	45		ns	Fig. 3-8