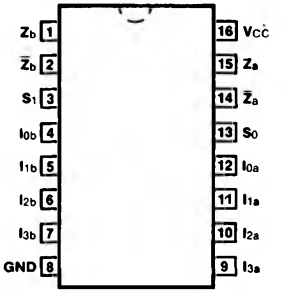
9309
93L09
DUAL 4-INPUT MULTIPLEXER

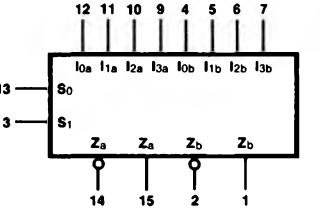
DESCRIPTION — The '09 monolithic dual 4-input digital multiplexers consist of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. In addition to multiplexer operation, the '09 can generate any two function of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because or its high speed performance and on-chip select decoding, the '09 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output bus.

- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9309PC, 93L09PC		9B
Ceramic DIP (D)	A	9309DC, 93L09DC	9309DM, 93L09DM	6B
Flatpak (F)	A	9309FC, 93L09FC	9309FM, 93L09FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L) HIGH/LOW	93L (U.L.) HIGH/LOW
S_0, S_1	Common Select Inputs	1.0/1.0	0.5/0.25
I_{0a} — I_{3a}	Multiplexer A Inputs	1.0/1.0	0.5/0.25
Z_a	Multiplexer A Output	20/10	10/5.0 (3.0)
$\overline{Z}_a$	Complementary Multiplexer A Output	18/9.0	10/5.0 (3.0)
I_{0b} — I_{3b}	Multiplexer B Inputs	1.0/1.0	0.5/0.25
Z_b	Multiplexer B Output	20/10	10/5.0 (3.0)
$\overline{Z}_b$	Complementary Multiplexer B Output	18/9.0	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '09 dual 4-input multiplexers are able to select two bits of either HIGH or LOW data or control from up to four sources, in one package. The '09 is the logical implementation of two-pole, four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$$Z_a = I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0$$
$$Z_b = I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0$$

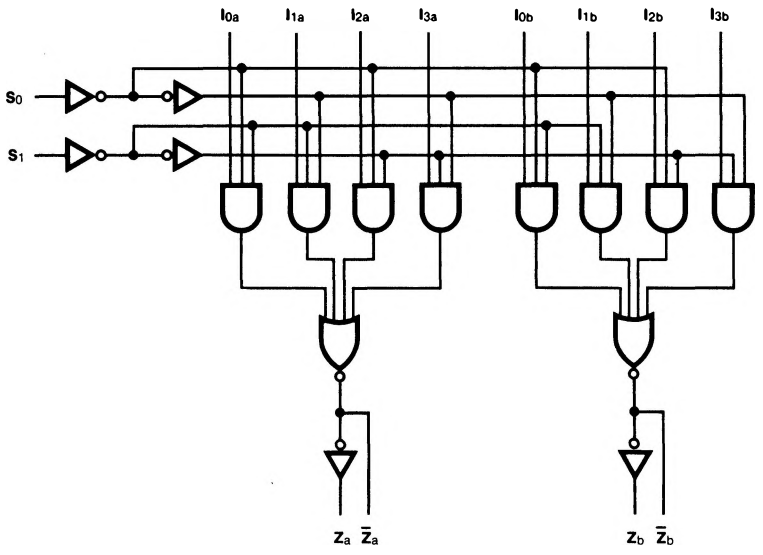
The '09 is frequently used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the select inputs. A less obvious application is as a function generator. The '09 can generate two functions of three variables. This is useful for implementing random gating functions.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)				OUTPUTS (a or b)	
S_0	S_1	I_0	I_1	I_2	I_3	Z	$\overline{Z}$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current			-10	-40	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		44		11.5	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load definitions)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15pF		C_L = 15pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_0 to Z_a		29 27		70 60	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay S_0 to $\overline{Z}_a$		21 21		55 50	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_{0a} to $\overline{Z}_a$		12 13		40 60	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay I_{0a} to Z_a		20 21		70 65	ns	Figs. 3-1, 3-5