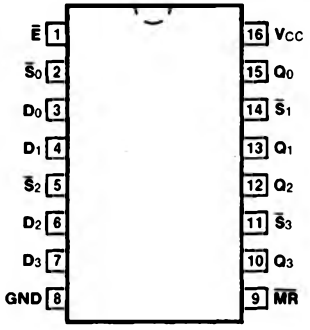
9314
93L14
QUAD LATCH

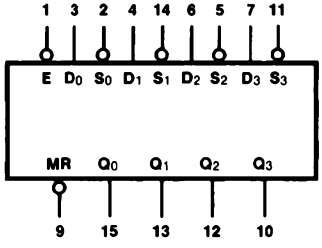
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '14 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.

- **CAN BE USED AS SINGLE INPUT D LATCHES OR SET/RESET LATCHES**
- **ACTIVE LOW ENABLE GATE INPUT**
- **OVERRIDING MASTER RESET**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9314PC, 93L14PC		9B
Ceramic DIP (D)	A	9314DC, 93L14DC	9314DM, 93L14DM	6B
Flatpak (F)	A	9314FC, 93L14FC	9314FM, 93L14FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	0.5/0.25
$D_0 - D_3$	Data Inputs	1.5/1.5	0.75/0.375
$\bar{S}_0 - \bar{S}_3$	Set Inputs (Active LOW)	1.0/1.0	0.5/0.25
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
$Q_0 - Q_3$	Latch Outputs	20/10	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '14 consists of four latches with a common active LOW Enable input and active LOW Master Reset input. When the Enable goes HIGH, data present in the latches is stored and the state of the latch is no longer affected by the $\overline{S}_n$ and D_n inputs. The Master Reset when activated overrides all other input conditions forcing all latch outputs LOW. Each of the four latches can be operated in one of two modes:

D-TYPE LATCH — For D-type operation the $\overline{S}$ input of a latch is held LOW. While the common Enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the Enable goes HIGH.

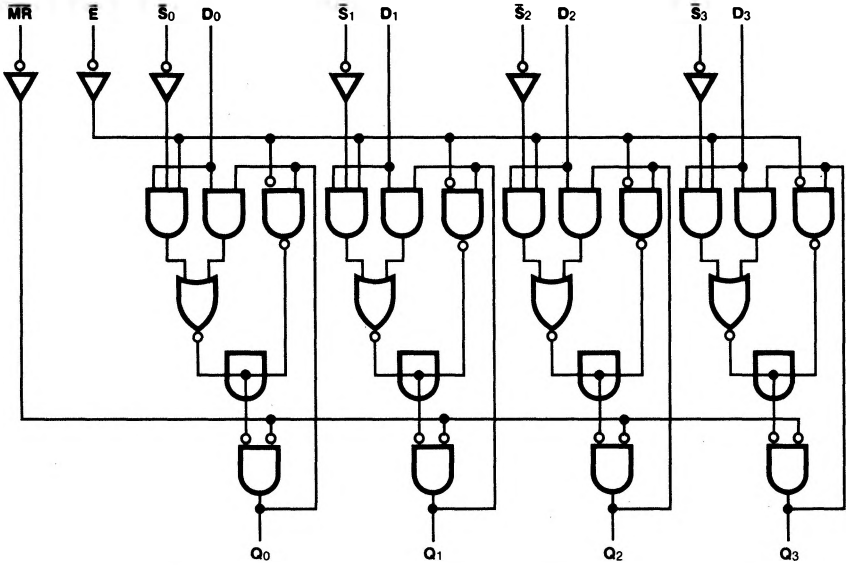
SET/RESET LATCH — During set/reset operation when the common Enable is LOW a latch is reset by a LOW on the D, input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. It both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch will be reset. When the Enable goes HIGH, the latch remains in the last state prior to disablement. The two modes of latch operation are shown in the Truth Table.

TRUTH TABLE

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_n	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	RESET

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Q_{n-1} = Previous Output State
Q_n = Present Output State

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		55		16.5	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		24 24		45 36	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		12 24		30 30	ns	Figs. 3-1, 3-5
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n		18		30	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{S}_n$ to Q_n		24		33	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{E}$	5.0 18		10 20		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to $\overline{E}$	0 5.0		0 10		ns	
t_s (H)	Setup Time HIGH, D_n to $\overline{S}_n$	8.0		15		ns	Fig. 3-13
t_h (L)	Hold Time LOW, D_n to $\overline{S}_n$	8.0		5.0		ns	
t_w (L)	$\overline{E}$ Pulse Width LOW	18		30		ns	Fig. 3-9
t_w (L)	$\overline{MR}$ Pulse Width LOW	18		25		ns	Fig. 3-16
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}$	0		5.0		ns	Fig. 3-16