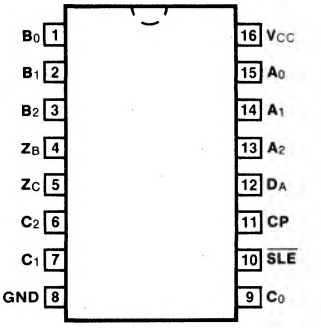
9338
93L38

8-BIT MULTIPLE PORT REGISTER

DESCRIPTION — The '38 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously. The circuit uses TTL technology and is compatible with all TTL families.

- **MASTER/SLAVE OPERATION PERMITTING SIMULTANEOUS WRITE/READ WITHOUT RACE PROBLEMS**
- **SIMULTANEOUSLY READ TWO BITS AND WRITE ONE BIT IN ANY ONE OF EIGHT BIT POSITIONS**
- **READILY EXPANDABLE TO ALLOW FOR LARGER WORD SIZES**

CONNECTION DIAGRAM
PINOUT A



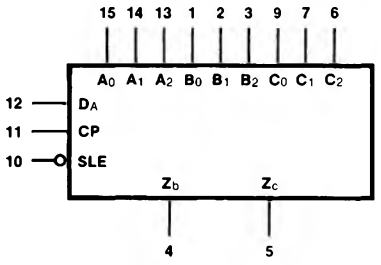
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9338PC, 93L38PC		9B
Ceramic DIP (D)	A	9338DC, 93L38DC	9338DM, 93L38DM	7B
Flatpak (F)	A	9338FC, 93L38FC	9338FM, 93L38FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

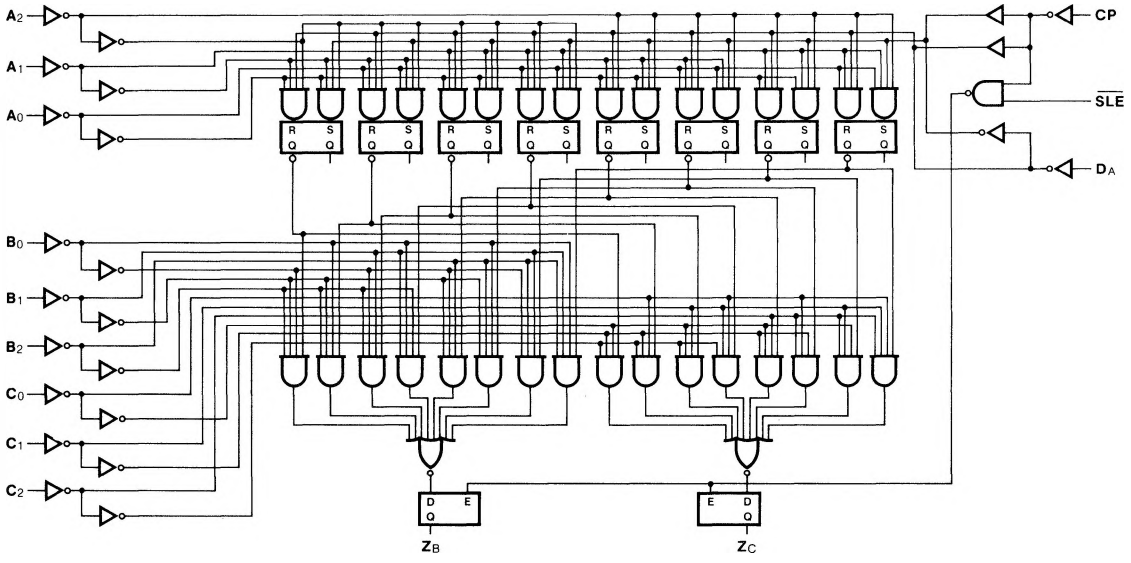
PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
A_0 — A_2	Write Address Inputs	0.67/0.68	0.33/0.17
D_A	Data Input	0.67/0.68	0.33/0.17
B_0 — B_2	B Read Address Inputs	0.67/0.68	0.33/0.17
C_0 — C_2	C Read Address Inputs	0.67/0.68	0.33/0.17
$\overline{CP}$	Clock Pulse Input (Active Rising Edge)	0.67/0.68	0.33/0.17
$\overline{SLE}$	Slave Enable Input (Active LOW)	0.67/0.68	0.33/0.17
Z_B	B Output	20/10	10/5.0 (3.0)
Z_C	C Output	20/10	10/5.0 (3.0)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The '38 8-bit multiple port register can be considered a 1-bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line (D_A) enters the selected master. This selection is accomplished by coding the three write input select lines (A_0 — A_2) appropriately. Data is stored synchronously with the rising edge of the clock pulse.

The information for each of the two slaved (output) latches is selected by two sets of read address inputs (B_0 — B_2 and C_0 — C_2). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW ($\overline{SLE}$), the slave latches are continuously enabled. The signals are available on the output pins (Z_B and Z_C). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.

The method of parallel expansion is shown in *Figure a*. One '38 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time, where n devices are connected in parallel.

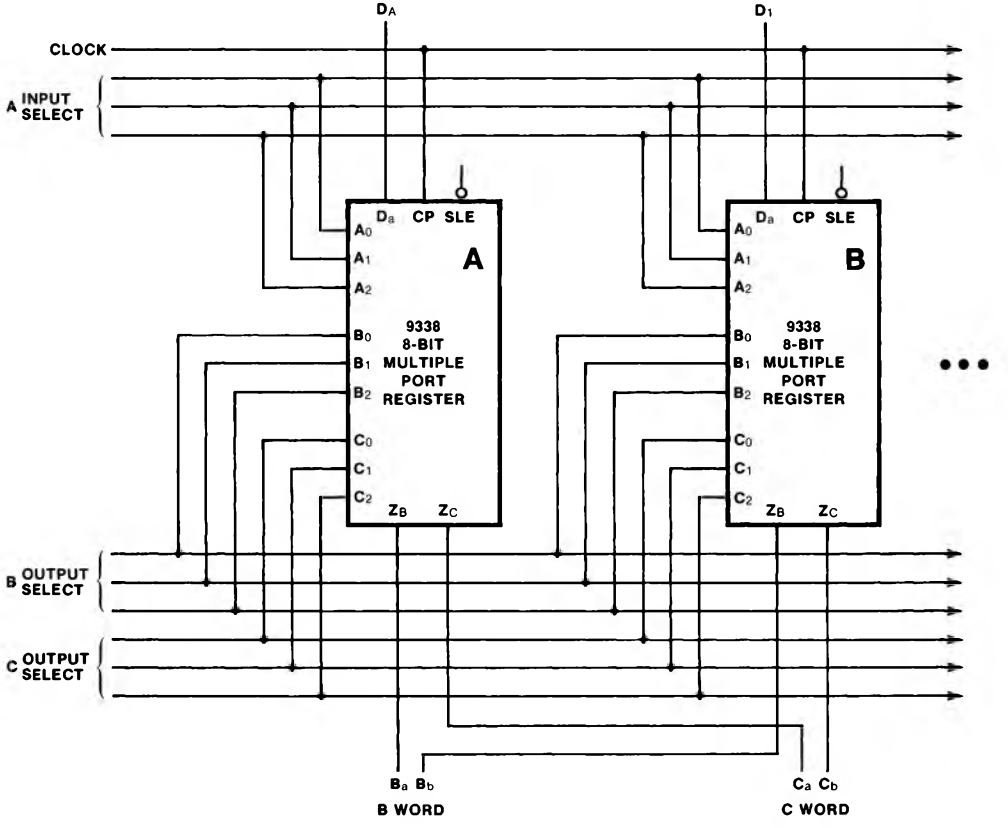


Fig. a Parallel Expansion

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	-10	-70	-2.5	-25	mA	V_{CC} = Max
I_{CC}	Power Supply Current		135		33	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay B_n or C_n to Z_n	13 18	40 35		68 95	ns	Figs.3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay D_A to Z_n	25 25	45 50		70 92	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay CP to Z_n	18 13	35 30		65 57	ns	Figs. 3-1, 3-8

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_A to CP	20 12		30 22		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_A to CP	0 -8.0		0 -4.0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to CP	10 10		0 0		ns	Fig. 3-21
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to CP	0 0		0 0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	23 13		40 30		ns	Fig. 3-8