64-BIT FIFO BUFFER MEMORY (16×4) 9403

FEATURES

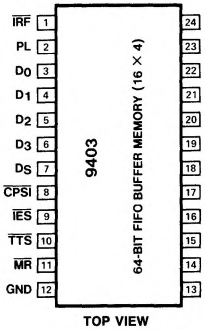
- **10MHz Serial or Parallel Data Rate**
- **Serial or Parallel Input and Output**
- **Expandable Without External Logic**
- **Three-State Outputs**
- **Fully TTL-Compatible**
- **Slim (0.4 in.) 24-Pin DIP**

PRODUCT DESCRIPTION

The 9403 is an expandable fall-through type First-In First-Out (FIFO) Buffer Memory that is optimized for high-speed disc/tape controllers and communication-buffer applications. In multiples of four, the device can be expanded to any number of bits and subsequently, to any number of words. Serial or parallel data can be asynchronously entered or retrieved which makes the 9403 *the* cost-effective solution for implementing buffer memories.

PIN DESIGNATIONS & DESCRIPTIONS

N PACKAGE



TOP VIEW

ORDER NUMBER

N9403N

MNEMONIC AND FUNCTION		DESCRIPTION
$\overline{IRF}$	= Input register full output	Low when input register is full
PL	= Parallel load input	High on PL enables D_0-D_3, not edge-triggered, 1's catching
D_0-D_3	= Parallel data input	—
D_S	= Serial data input	—
$\overline{CPSI}$	= Serial input clock	Edge-triggered and activates on falling edge
$\overline{IES}$	= Serial input enable	When low, serial input is enabled
$\overline{TTS}$	= Transfer to stack input	When low, initiates fall-through
$\overline{MR}$	= Master Reset	Active low
TOP	= Transfer out parallel input	When high and $\overline{TOS}$ is low, enables word transfer from stack to output register—not edge-triggered

MNEMONIC AND FUNCTION		DESCRIPTION
$\overline{TOS}$	= Transfer out serial input	When low and TOP is high, enables word transfer from stack to output register—not edge-triggered
$\overline{OES}$	= Serial output enable input	When low, enables serial output
$\overline{CPSO}$	= Serial output clock input	Edge-triggered and activates on falling edge
$\overline{EO}$	= Output enable	Active low
Q_0-Q_3	= Parallel data output	
Q_S	= Serial data output	
$\overline{ORE}$	= Output register empty output	When high, output register contains valid data
GND	= Ground	—
V_{CC}	= Supply voltage	+5 volts

FUNCTIONAL DESCRIPTION

As shown in Figure 1, the 9403 consists of three parts which operate asynchronously and are virtually independent. These parts are:

- **Input Register**—with serial and parallel data inputs and control signals that permit easy expansion and a handshake interface.
- **FIFO Stack**—4-bit wide, 14-word deep fall-through type with self-contained control logic.
- **Output Register**—with serial and parallel data outputs and control signals that permit easy expansion and a handshake interface.

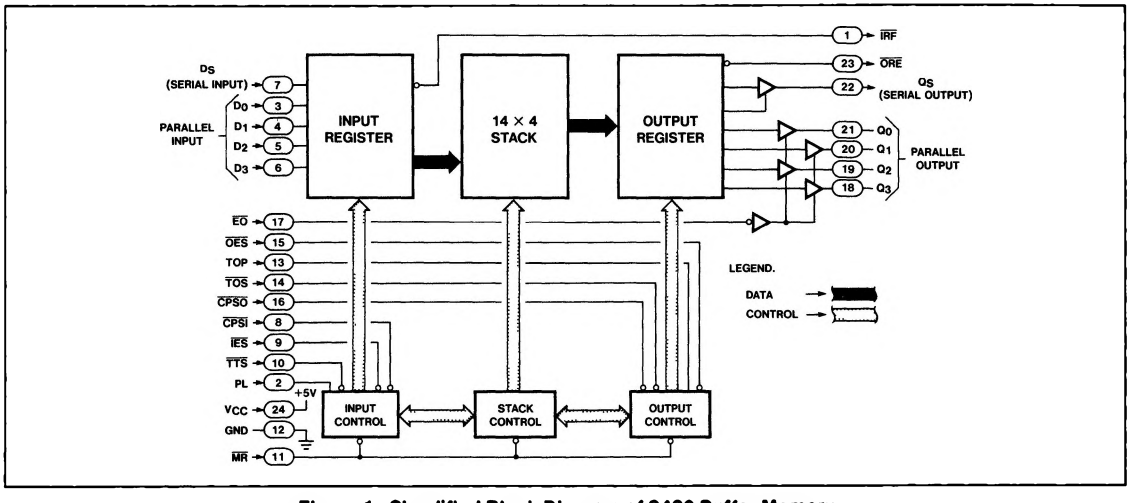


Figure 1. Simplified Block Diagram of 9403 Buffer Memory

INPUT REGISTER

Data can be entered serially or, using the parallel mode of operation, data is entered in 4-bit increments. In either case, the data is subsequently transferred to the fall-through stack; the functional equivalent of this register is shown in Figure 2. The Input Register Full ($\overline{IRF}$) status signal is internally generated by the Register Status (RS) flip-flop; when initialized, the $\overline{Q}$ ($\overline{IRF}$) output of this flip-flop is high.

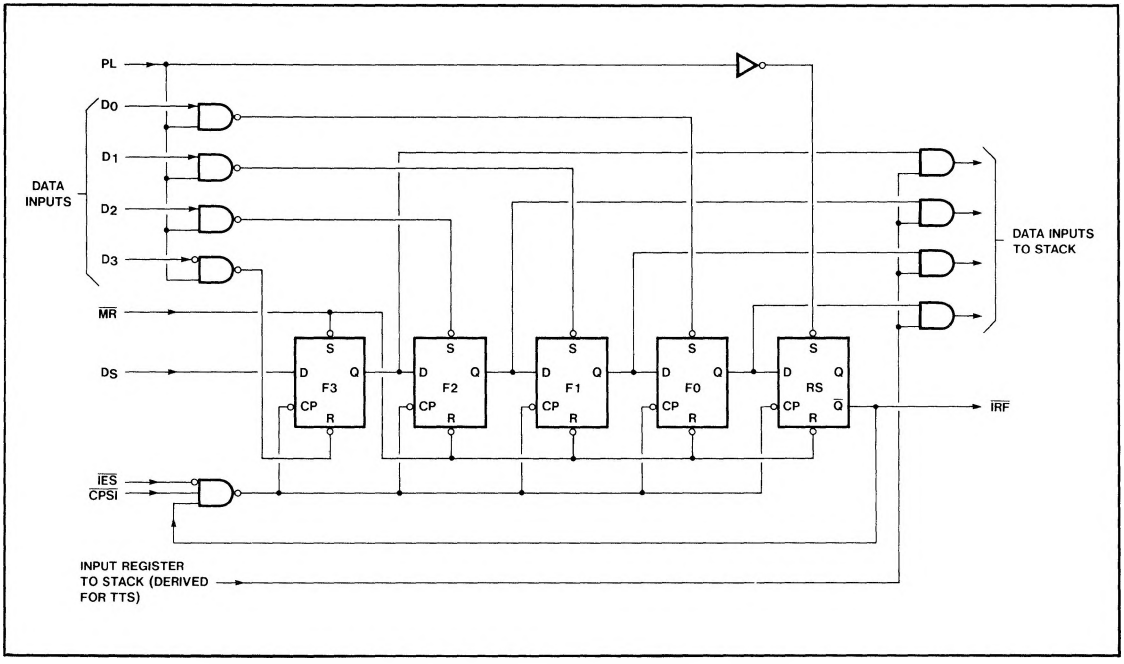


Figure 2. Functional Equivalent of Input Register

Serial Entry (Input Register)

Serial data is entered via the D_S input and is handled by a 5-bit shift register consisting of flip-flops F3, F2, F1, F0, and RS. With $\overline{IES}$ and PL both low, each high-to-low transition of the serial input clock ($\overline{CPSI}$) shifts the input data in domino order from F3 to F2 to F1 to F0. After the fourth clock transition, the four bits of serial data are aligned in F3 through F0 and RS is set, forcing $\overline{IRF}$ low and inhibiting $\overline{CPSI}$ until contents of the input register are transferred to the stack. Figure 3 shows how a serial train of 64-bits would appear in the 9403—four bits (B60-B63) in the input register, 56 bits (B4-B59) in the stack, and four bits (B0-B3) in the output register.

Parallel Entry (Input Register)

When PL is high and $\overline{CPSI}$ is low (Figure 2), flip-flops F0-F3 are loaded with data and $\overline{IRF}$ is forced low. This condition remains until current data is transferred to the stack. Once the data is transferred, $\overline{IRF}$ is driven high and new data can again be clocked into the input flip-flops. If parallel expansion is not being implemented, $\overline{IES}$ must be low to establish row mastership—refer to discussion of parallel expansion.

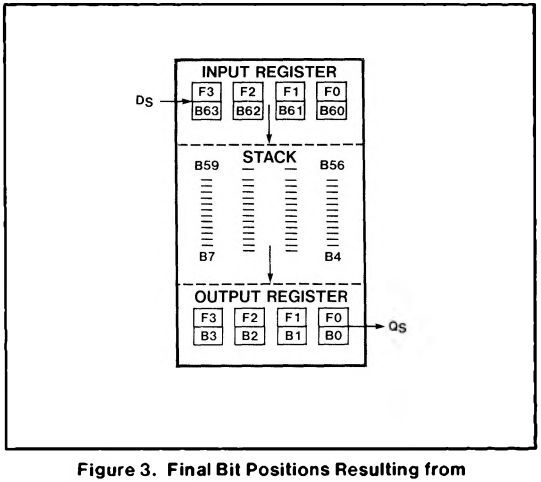


Figure 3. Final Bit Positions Resulting from a Serial Train of 64-Bits

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STACK OPERATION

As shown in Figure 2, the outputs of F0-F3 are applied to the stack under control of a signal derived from $\overline{TTS}$. When $\overline{TTS}$ is low, an attempt to initiate a fall-through action is made. If the top location of stack is empty, data is loaded and the input register is re-initialized provided PL is low. Note that initialization is postponed until PL is again low. Thus, automatic FIFO action is achieved by connecting the $\overline{TTS}$ input to the $\overline{IRF}$ output.

The RS flip-flop (Figure 2) records the fact that data has been transferred to the stack; this flip-flop is not cleared until PL goes low. Therefore, if a particular data word is transferred to the stack and falls to the second location before PL goes low, the same word will not be re-transferred even though $\overline{IRF}$ and $\overline{TTS}$ are still low. Once data enters the stack, "fall-through" is automatic; a delay is necessary only when waiting for the next stack location to empty. In the 9403, as in most modern FIFO designs, the $\overline{MR}$ input initializes the stack control section and does not clear the data.

OUTPUT REGISTER

This register receives and stores 4-bits of data from the bottom stack location and, on demand, outputs the data onto a three-state 4-bit parallel data bus or a three-state serial data bus. The Output Register Full ($\overline{ORE}$) status signal is internally-generated by the FX flip-flop, when data is transferred from the stack to the output register, $\overline{ORE}$ goes high. The functional equivalent of the output register is shown in Figure 4.

Retrieval of Parallel Data

With the stack empty and $\overline{MR}$ in the active-low state, the $\overline{ORE}$ output goes low, signifying that the output register is also empty. When new data is entered and has fallen through to bottom location of the stack, it is automatically transferred to the output register, provided the Transfer Out Parallel (TOP) input is high. When the data is transferred from stack-to-register, $\overline{ORE}$ goes high and valid data appears at Q_0-Q_3 (Figure 4), provided the three-state buffers are enabled, that is, $\overline{EO}$ is active-low. When TOP goes low, $\overline{ORE}$ is driven low which indicates that the data output cycle is complete; however, the original data remains latched in the flip-flops until the next word (if available) is transferred from the stack to the output register.

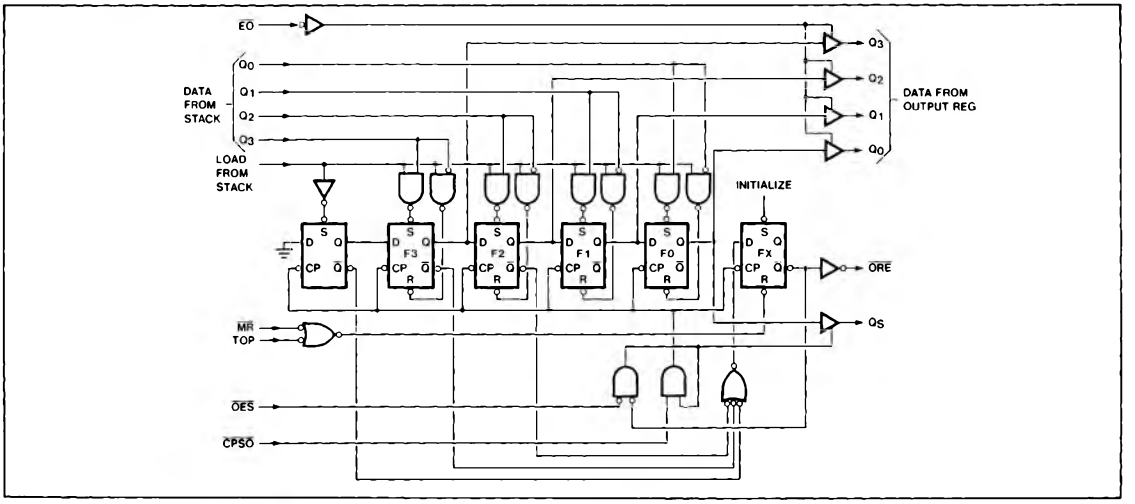

Figure 4. Functional Equivalent of Output Register

Retrieval of Serial Data

When the FIFO stack is empty and $\overline{MR}$ is driven low, the $\overline{ORE}$ output goes low to indicate that the output register is ready to accept new data from the stack. After new data is entered and falls through to the bottom stack location, it is transferred to the output register provided $\overline{TOS}$ is low and TOP is high. As a result of the data transfer, $\overline{ORE}$ goes high indicating valid data in the output register. Subsequently, the $\overline{Q}_S$ output is automatically enabled and the first data bit is transmitted to the three-state serial data bus. Henceforth, a serial shift of data occurs on each high-to-low transition of $\overline{CPSO}$. On the fourth transition, the register is emptied, $\overline{ORE}$ is forced low, and serial output $\overline{Q}_S$ is disabled. To request a new word from the stack, the $\overline{TOS}$ input can be connected to the $\overline{ORE}$ output.

For parallel operation, $\overline{CPSO}$ must be low, whereas, $\overline{TOS}$ should be grounded for single-slice operation or connected to the appropriate $\overline{ORE}$ for expanded operation. The TOP input is not edge-triggered, therefore, if it goes high before data is available from stack but data becomes available before it goes low, the data will be transferred to the output register. However, internal control circuits prevent the same data from being transferred twice. If TOP goes high and returns to low before data is available from the stack, $\overline{ORE}$ will remain low, indicating the absence of valid output data.

VERTICAL EXPANSION

In a vertical structure, the 9403 can be expanded to achieve greater word capacity without any external parts; a 46-word by 4-bit FIFO is shown in Figure 5. Using the same technique and similar connections, any FIFO of 15n+1 words (where *n* is the number of devices) can be constructed. Observe that word expansion does not sacrifice flexibility of the 9403 FIFO as regards serial/parallel input and output.

HORIZONTAL EXPANSION

The 9403 can be horizontally expanded to store long words in multiples of 4-bits, again without external logic. Connections required to form a 16-word by 12-bit FIFO are shown in Figure 6, using similar techniques, any 16-word by 4n-bit FIFO (where *n* is the number of devices) can be constructed.

For horizontal or bit expansion, it is good practice to connect, respectively, the $\overline{IRF}$ and $\overline{ORE}$ outputs of the right-most device (most significant device) to the $\overline{TTS}$ and $\overline{TOS}$ inputs of all devices to the left (least significant devices) to guarantee that no operation is initiated before each and every device is ready Word expansion does not affect the ability of the 9403 to handle serial/parallel inputs and outputs, however, the ripple form of expansion shown in Figure 6 does extract a penalty in speed of operation Whereas a single 9403 is guaranteed to operate at 10MHz, an array of four FIFOs connected as shown is guaranteed to operate at 4 3MHz

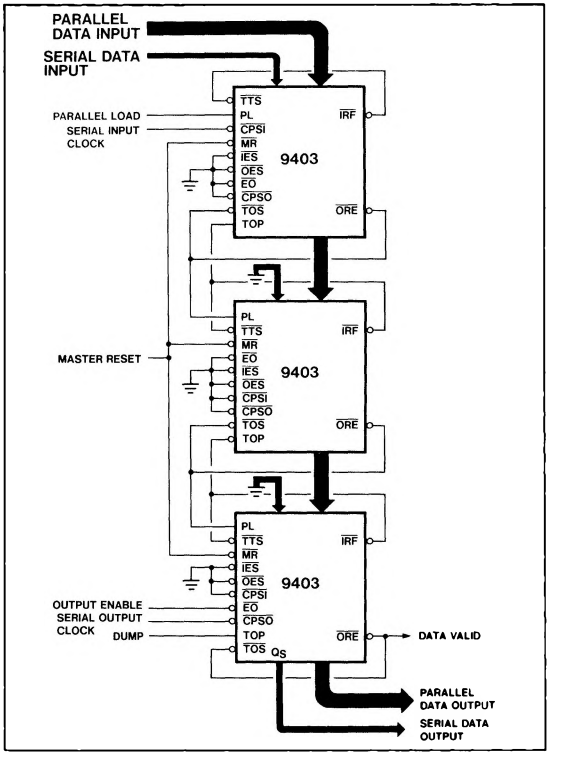

Figure 5. Word Expansion

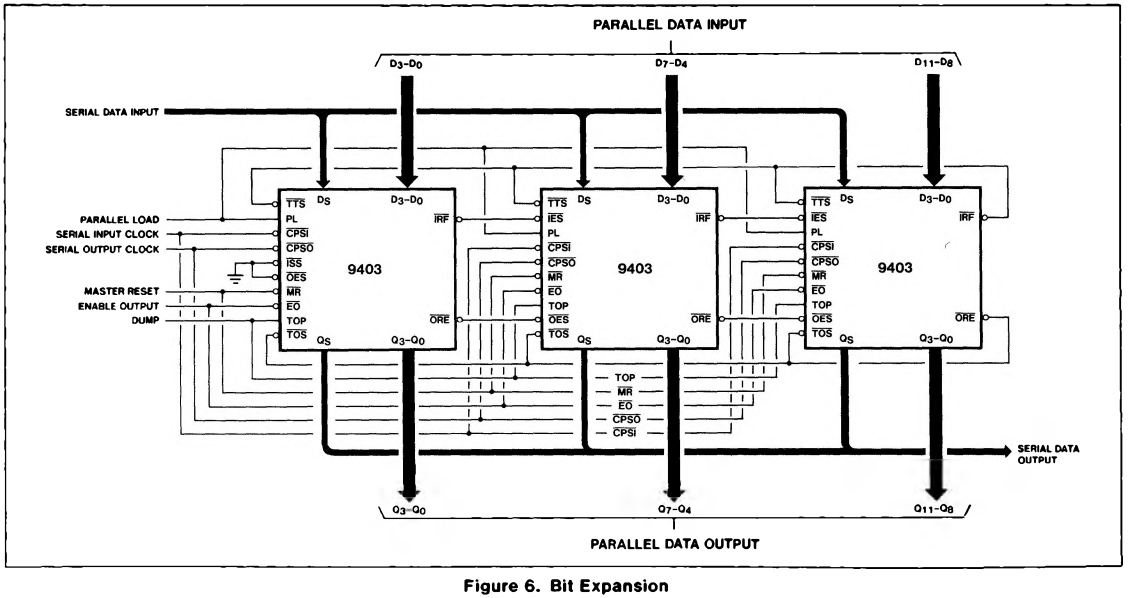

Figure 6. Bit Expansion

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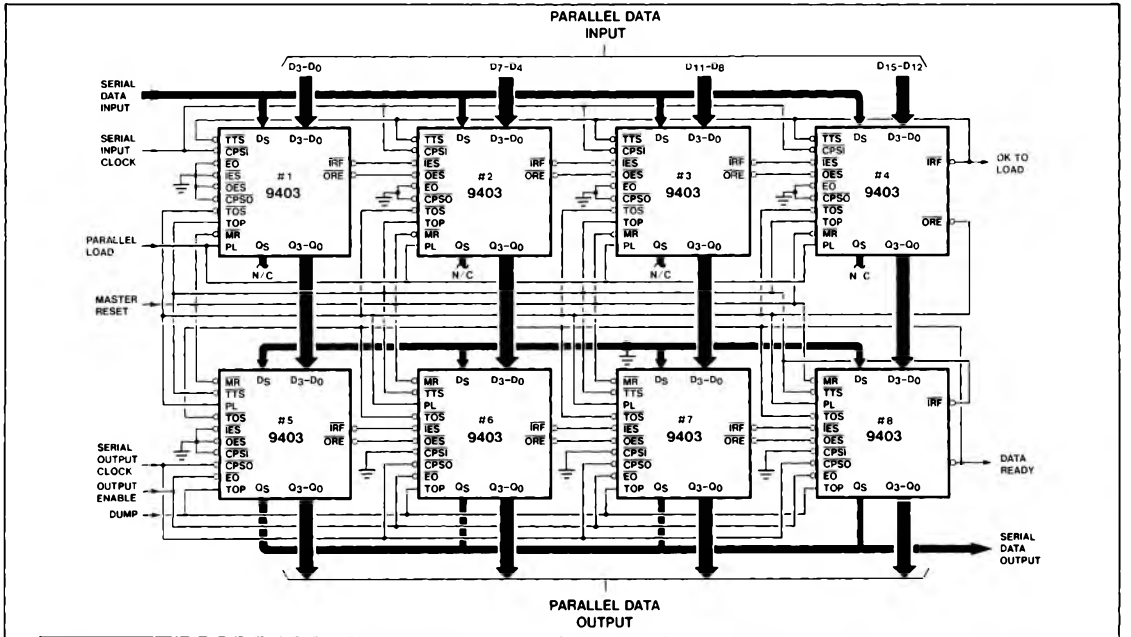
HORIZONTAL AND VERTICAL EXPANSION

In addition to bit-or-word expansion, the 9403 can be used to expand in both the horizontal and vertical directions; a 31-word by 16-bit FIFO is shown in Figure 7. Using the same or similar techniques, any FIFO of 15m+1 words by 4n-bits can be constructed, where *m* is the number of devices in a column and *n* is the number of devices in a row.

The chart appended to Figure 7 shows the final positions for a contiguous serial entry of 496 bits. Figures 8 and 9, respectively, show the timing relationships involved for data-entry and data-retrieval pertaining to the 31-word by 16-bit array.



INPUT REGISTER	UNIT NUMBER & ORDER OF SERIAL BITS #1	#2	#3	#4	OUTPUT REGISTER	UNIT NUMBER & ORDER OF SERIAL BITS #5	#6	#7	#8
D_3	BIT 483	BIT 487	BIT 491	BIT 495	Q_3	BIT 3	BIT 7	BIT 11	BIT 15
D_2	482	486	490	494	Q_2	2	6	10	14
D_1	481	485	489	493	Q_1	1	5	9	13
D_0	480	484	488	492	Q_0	0	4	8	12

Figure 7. Horizontal and Vertical Expansion—31X16 FIFO

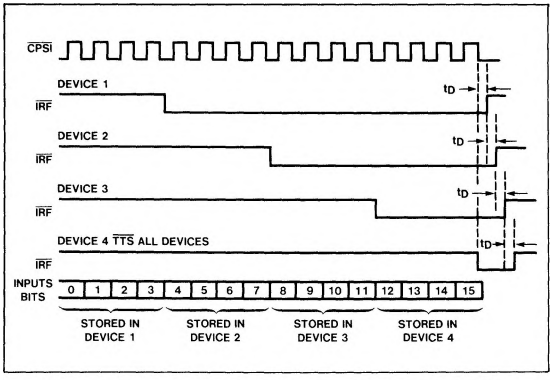


Figure 8. Entry of Serial Data for Array of Figure 7

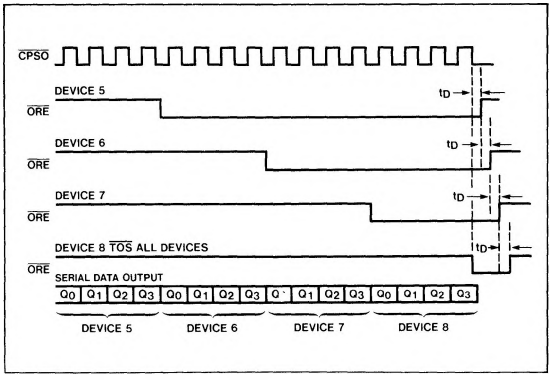


Figure 9. Retrieval of Serial Data for Array of Figure 7

INTERLOCKING CIRCUITS

Most conventional FIFO designs provide the status-signal counterparts of $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are used in arrays, variations in unit-to-unit operating speeds require the use of external gating to ensure that all devices have, in fact, completed the last operation. The 9403 incorporates simple but effective master/slave interlocking circuits to eliminate these gating requirements.

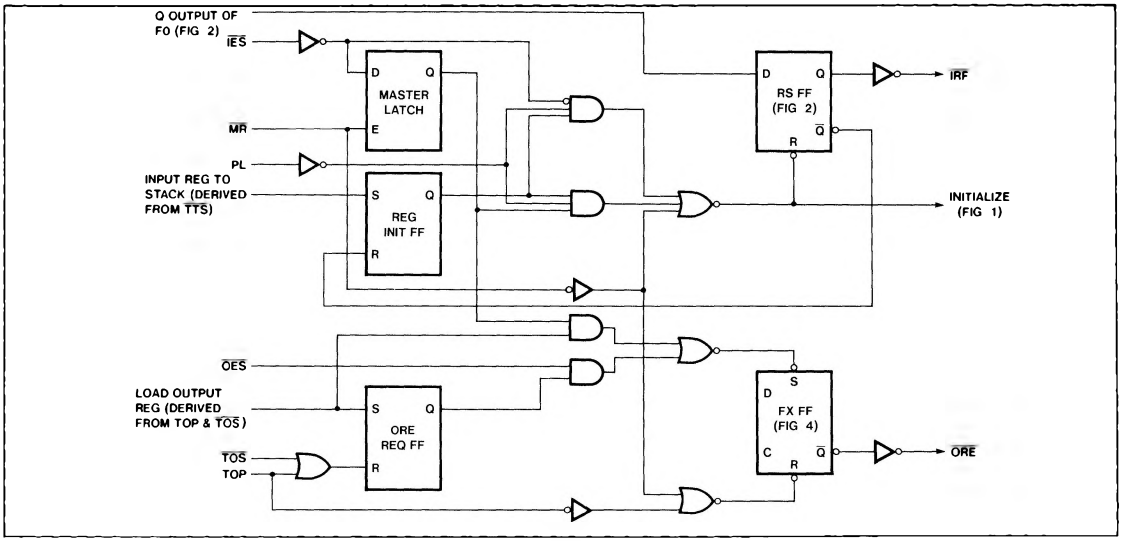


Figure 10. Functional Equivalent of Interlocking Circuits

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5 5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
T_A	Operating temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS Over operating temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ	Max	
V_{IH}	Input high voltage	Guaranteed input high voltage	2.0			V
V_{IL}	Input low voltage	Guaranteed input low voltage			0.8	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = −18mA		−0.9	−1.5	V
V_{OH}	Output high voltage, $\overline{ORE}$, $\overline{IRF}$	V_{CC} = Min, I_{OH} = −400μA	2 4	3.4		V
V_{OH}	Output high voltage, Q_0-Q_3, Q_S	I_{OH} = −5.7mA, V_{CC} = Min	2.4	3.1		V
V_{OL}	Output low voltage, Q_0-Q_3, Q_S	V_{CC} = Min, I_{OL} = 16mA		0.35	0.5	V
V_{OL}	Output low voltage, $\overline{ORE}$, $\overline{IRF}$	V_{CC} = Min, I_{OL} = 8.0mA		0.35	0.5	V
I_{OZH}	Output off current high, Q_0-Q_3, Q_S	V_{CC} = Max, V_{OUT} = 2.4V, V_E = 2V			100	μA
I_{OZL}	Output off current low, Q_0-Q_3, Q_S	V_{CC} = Max, V_{OUT} = 0.5V, V_E = 2V			−100	μA
I_{IH}	Input high current	V_{CC} = Max, V_{IN} = 2.7V		1.0	40	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
I_{IL}	Input low current, all except $\overline{OES}$ & $\overline{IES}$	V_{CC} = Max, V_{IN} = 0 4V			−0.36 −0.96	mA
I_{OS}	Output short circuit current, Q_0-Q_3, Q_S $\overline{ORE}$, $\overline{OES}$	V_{CC} = Max, V_{OUT} = 0, (Note 3)	−30		−130	mA
I_{CC}	Supply Current	V_{CC} Max, Inputs open		115	170	mA

NOTES
1 Operating temperature ranges are guaranteed after terminal equilibrium has been reached
2 All voltages measured with respect to ground terminal
3 No more than one output should be shorted at a time

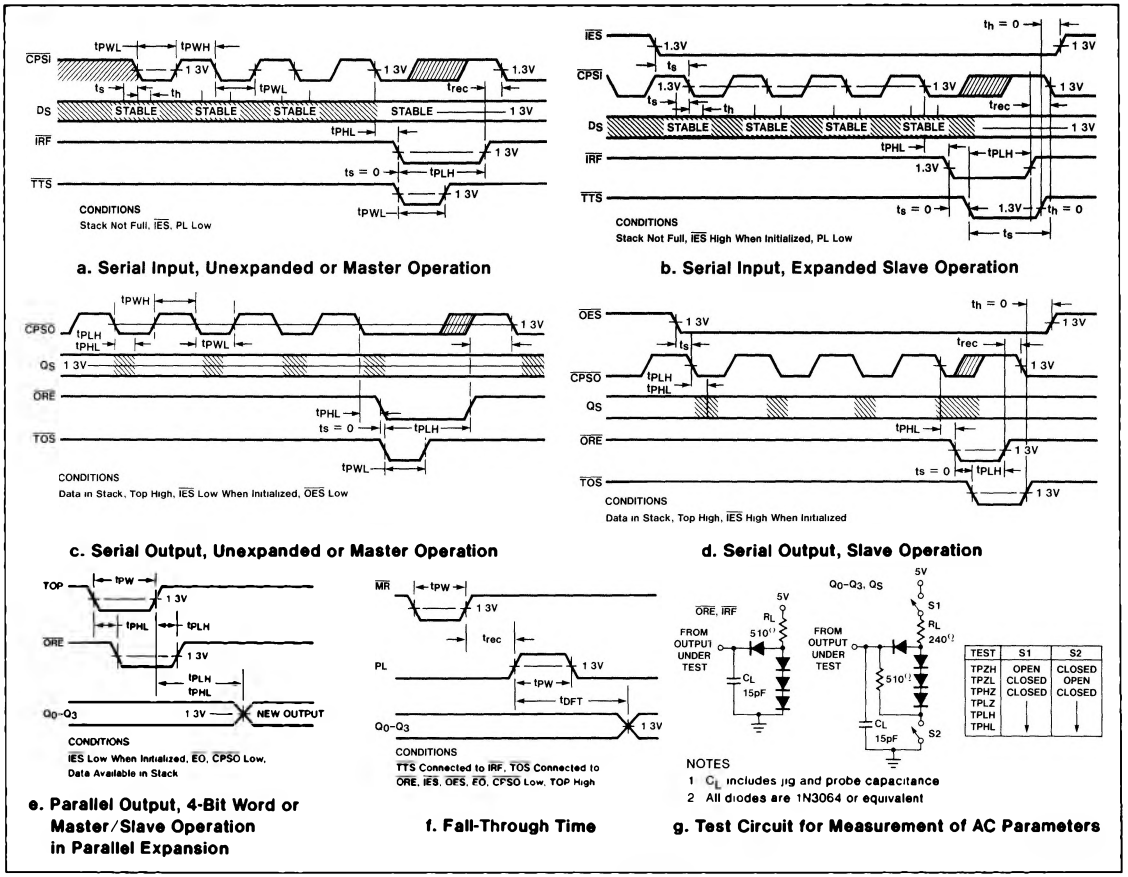
AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V, C_L = 15pF, T_A = 25° C

PARAMETER	FROM INPUT	TO OUTPUT	TEST CONDITIONS[1,2,3]	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
FALL-THROUGH TIME t_{DFT}	Positive going PL	Q_0-Q_3	$\overline{TTS}$ connected to $\overline{IRF}$, $\overline{TOS}$ connected to $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ low, TOP high (f, Fig 11)		450	600	ns
PROPAGATION DELAY							ns
t_{PLH} Low-to-high	Negative going $\overline{TTS}$	$\overline{IRF}$	Stack not full, PL low (a & b, Fig 11)		48	64	
t_{PHL} High-to-low	Negative going $\overline{CPSI}$	$\overline{IRF}$			18	25	
t_{PLH} Low-to-high	Negative going $\overline{CPSO}$	Q_S	Serial output $\overline{OES}$ low, TOP high (c & d, Fig 11)		30	40	ns
t_{PHL} High-to-low					17	28	
t_{PHL} High-to-low	Negative going $\overline{CPSO}$	$\overline{ORE}$			32	42	ns
t_{PLH} Low-to-high	Positive going TOP	Q_0-Q_3	$\overline{EO}$, $\overline{CPSO}$ low (e, Fig 11)		40	56	ns
t_{PHL} High-to-low					31	45	
t_{PLH} Low-to-high	Positive going TOP	$\overline{ORE}$	Parallel output, $\overline{EO}$, $\overline{CPSO}$ low (e, Fig 11)		51	68	ns
t_{PHL} High-to-low	Negative going TOP	$\overline{ORE}$			40	54	
t_{PLH} Low-to-high	Negative going $\overline{TOS}$	Positive going $\overline{ORE}$	Data in stack, TOP high, (c & d, Fig 11)		41	56	ns
t_{PHL} High-to-low	Positive going PL	Negative going $\overline{IRF}$	Stack not full (g & h, Fig 11)		20	33	ns
t_{PLH} Low-to-high	Negative going PL	Positive going $\overline{IRF}$			33	46	ns
t_{PLH} Low-to-high	Positive going $\overline{OES}$	$\overline{ORE}$			26	44	
t_{PLH} Low-to-high	Positive going $\overline{IES}$	Positive going $\overline{IRF}$			31	40	
ENABLE DELAY							ns
t_{PZH} High	$\overline{EO}$	Q_0-Q_3	Out of high impedance state		9	14	
t_{PZL} Low						20	
t_{PZL} Low	Negative going $\overline{OES}$	Q_S			13	25	ns
t_{PZH} High						20	
DISABLE DELAY							ns
t_{PLZ} Low	$\overline{EO}$	Q_0-Q_3	Into high impedance state		7	14	
t_{PHZ} High							
t_{PLZ} Low	Negative going $\overline{OES}$	Q_S			7	14	ns
t_{PHZ} High							
APPEARANCE TIME							ns
t_{AP} Parallel	$\overline{ORE}$	Q_0-Q_3	Time elapsed between $\overline{ORE}$ going high and valid data appearing at output, negative number indicates data available before $\overline{ORE}$ goes high		−12	−5	
t_{AS} Serial	$\overline{ORE}$	Q_S			6	10	
PULSE WIDTH							ns
t_{PWL} $\overline{CPSI}$ low			Stack not full, PL low (a & b, Fig 11)	20	11		
t_{PWH} $\overline{CPSI}$ high				33	19		
t_{PWL} TOP low			$\overline{CPSO}$ low, data available in stack (e, Fig 11)	30	17		ns
t_{PWH} TOP high				26	13		
t_{PWL} $\overline{CPSO}$ low			TOP high, data in stack, (c & d, Fig 11)	30	16		ns
t_{PWH} $\overline{CPSO}$ high				32	18		
t_{PWH} PL high			Stack not full (g & h, Fig 11)	40	29		ns
t_{PWL} $\overline{TTS}$ low (serial or parallel mode)			Stack not full (a, b, g, & h, Fig 11)	20	9		ns
t_{PWL} $\overline{MR}$ low			(f, Fig 11)	25	13		ns
SETUP and HOLD TIME							ns
t_s Setup time	D_S	Negative $\overline{CPSI}$	PL low (a & b, Fig 11)	28	17		
t_h Hold time	D_S	$\overline{CPSI}$		0	−6		

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V, C_L = 15pF, T_A = 25° C (Cont'd)

PARAMETER	FROM	TO	TEST CONDITIONS[1,2,3]	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_s Setup time	Parallel inputs	PL	Length of time parallel inputs must be applied prior to rising edge of PL	0	−22		ns
t_h Hold time	Parallel inputs	PL	Length of time parallel inputs must remain applied after falling edge of PL	2			ns
t_s Set up time (serial or parallel mode)	$\overline{TTS}$	$\overline{IRF}$	(a, b, g, & h, Fig 11)	0	−20		ns
t_s Setup time	Negative going $\overline{ORE}$	Negative going $\overline{TOS}$	TOP high (c & d, Fig 11)	0	−24		ns
t_s Setup time t_s Setup time	Negative going $\overline{IES}$ Negative $\overline{TTS}$	$\overline{CPSI}$ $\overline{CPSI}$	(b, Fig 11)	45 84	23 58		ns
RECOVERY TIME t_{rec}	$\overline{MR}$	Any input	(f, Fig 11)	15	5		ns

NOTES
1 Initialization requires a master reset to occur after power has been applied
2 $\overline{TTS}$ normally connected to $\overline{IRF}$
3 If stack is full, $\overline{IRF}$ will stay low



a. Serial Input, Unexpanded or Master Operation

b. Serial Input, Expanded Slave Operation

c. Serial Output, Unexpanded or Master Operation

d. Serial Output, Slave Operation

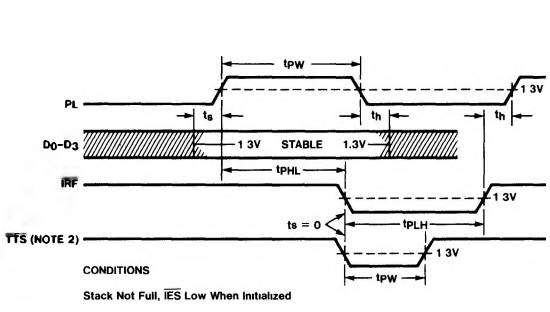
e. Parallel Output, 4-Bit Word or Master/Slave Operation in Parallel Expansion

f. Fall-Through Time

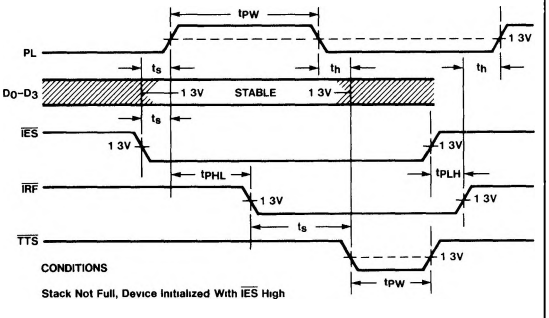
g. Test Circuit for Measurement of AC Parameters

NOTES
1 C_L includes jig and probe capacitance
2 All diodes are 1N3064 or equivalent

Figure 11. 9403 Timing and Parameter-Measurement Information



h. Parallel Load Mode, 4-BIT Word (Unexpanded) or Master/Slave Operation in Parallel Expansion



j. Parallel Load, Slave Mode

Figure 11. 9403 Timing and Parameter-Measurement Information (Cont'd)

LOGIC DIAGRAM