Data Sheet | July 1999 | FN4610.1

High Reliability, Radiation Hardened Octal Buffer/Line Driver, Three-State, Inverting

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil ACTS240T is a Radiation Hardened High Reliability, High-Speed CMOS/SOS Octal Buffer/Line Driver with three-state outputs having two active low enable inputs. Each enable input controls a set of four inverting buffer/line drivers. A HIGH on the enable input places the outputs in a high impedance state.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ACTS240T are contained in SMD 5962-96717. For more information, visit us at our website at: **www.intersil.com/**

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (^oC)
5962R9671701TRC	ACTS240DTR	-55 to 125
5962R9671701TXC	ACTS240KTR	-55 to 125

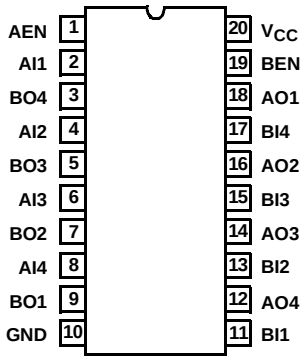
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

Features

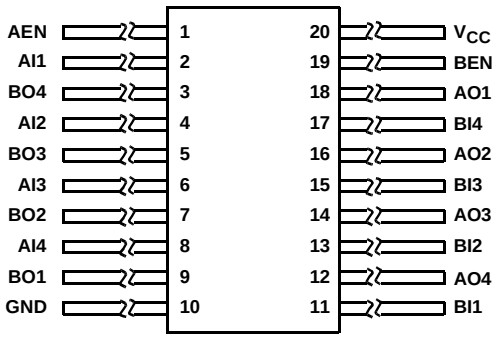
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - Latch-Up Free Under Any Conditions
  - Single Event Upset (SEU) Immunity: <1 x 10^{-10} Errors/Bit/Day (Typ)
  - SEU LET Threshold . . . . . .>100 MEV-cm^2/mg
- 1.25 Micron Radiation Hardened SOS CMOS
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range . . . . . 4.5V to 5.5V
- Input Logic Levels
  - V_{IL} = 0.8V Max
  - V_{IH} = $V_{CC/2}$ Min
- Fast Propagation Delay . . . . . 17.5ns (Max), 12ns (Typ)

Pinouts

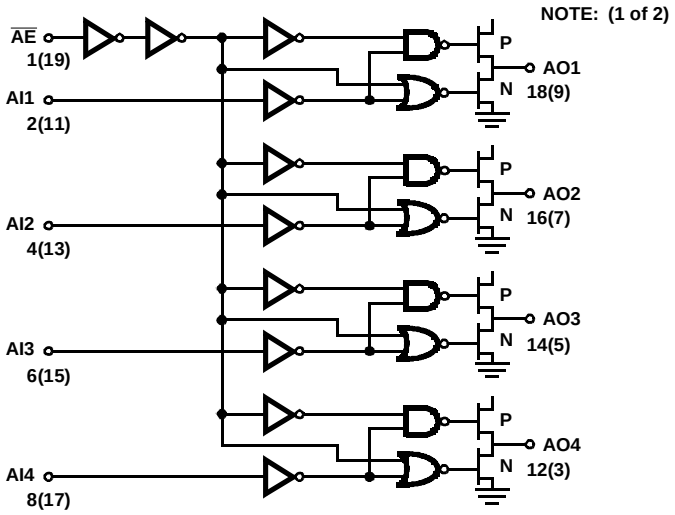
ACTS240T (SBDIP), CDIP2-T20
TOP VIEW



ACTS240T (FLATPACK), CDFP4-F20
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS		OUTPUT
$\overline{AE}$, $\overline{BE}$	AIn, BIn	AOn, BOn
L	L	H
L	H	L
H	X	Z

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Immaterial, Z = High Impedance

Die Characteristics

DIE DIMENSIONS:

(2540µm x 2540µm x 533µm ±51µm)
100 x 100 x 21mils ±2mil

METALLIZATION:

Type: Al Si Cu
Thickness: 10.0kÅ ±2kÅ

SUBSTRATE POTENTIAL:

Unbiased (Silicon on Sapphire)
Bond Pad #20 (V_{CC}) First
Bond Pad #10 (Gnd) Uses Two Bond Wires
Bond Pad #20 (V_{CC}) Uses Two Bond Wires

BACKSIDE FINISH:

Sapphire

PASSIVATION:

Type: Silox (S_iO_2)
Thickness: 8.0kÅ ±1.0kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

164

PROCESS:

CMOS SOS

Metallization Mask Layout

ACTS240T