ANALOG DEVICES

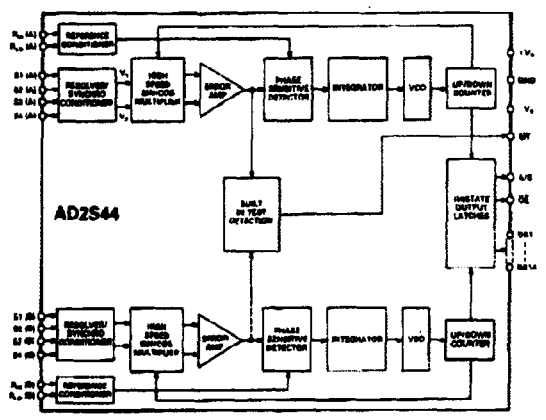
Low Cost, 14-Bit, Dual Channel Synchro/Resolver-to-Digital Converter

AD2S44

FEATURES
Low Cost/Channel
32-Pin DIL Hybrid Package
2.6 Arc Minute Accuracy
14-Bit Resolution
Built-In Test
Independent Reference Inputs
High Tracking Rate

APPLICATIONS
Gimbal/Gyro Control Systems
Robotics
Engine Controllers
Coordinate Conversion
Military Servo Control Systems
Fire Control Systems
Avionic Systems
Antenna Monitoring
CNC Machine Tooling

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S44 series are 14-bit dual channel, continuous tracking synchro/resolver-to-digital converters. They have been designed specifically for applications where space, weight and cost are at a premium. Each 32-pin hybrid device contains two independent Type II servo loop tracking converters. The ratiometric conversion technique employed provides excellent noise immunity and tolerance of long lead lengths.

The core of each conversion is performed by state-of-the-art monolithic integrated circuits manufactured in Analog Devices' proprietary BiMOS II process which combines the advantages of low power CMOS digital logic with bipolar linear circuits. The use of these ICs keeps the internal component count low and ensures high reliability.

The built-in test ($\overline{BIT}$) facility can be used in failsafe systems to provide an indication of whether the converter is tracking accurately.

Each channel incorporates a high accuracy differential conditioning circuit for signal inputs providing more than 74 dB of common mode rejection. Options are available for both synchro and resolver format inputs. The converter output is via a tristate transparent latch allowing data to be read without interruption of converter operation. The A/$\overline{B}$ and $\overline{OE}$ control lines select the channel and present the digital position to the common data outputs.

The AD2S44 also features independent reference inputs. Consequently, different reference frequencies may be used for each channel.

MODELS AVAILABLE

The AD2S44 series is available in three accuracy grades:

AD2S44UM	14-Bits	±4.0 Arc Mins −55°C to +125°C (±2.6 Arc Mins −25°C to +85°C)
AD2S44TM	14-Bits	±4.0 Arc Mins −55°C to +125°C
AD2S44SM	14-Bits	±5.2 Arc Mins −55°C to +125°C

Each grade has options available which will interface to synchros and resolvers of standard voltage and frequency.

All components are 100% tested at −55°C, +25°C, and +125°C. Devices processed to high reliability screening standards (Suffix B) receive further levels of testing and screening to ensure high levels of reliability. Full ordering information is given on the back page of this data sheet.

REV. A

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AD2S44—SPECIFICATIONS (typical @ +25°C unless specified otherwise)

Parameter		AD2S44	Units	Comments
PERFORMANCE				
Accuracy[1]	AD2S44UM	±4.0 (max)	Arc Min	−55°C to +125°C
		±2.6 (max)	Arc Min	−25°C to +85°C
	AD2S44TM	±4.0 (max)	Arc Min	−55°C to +125°C
	AD2S44SM	±5.2 (max)	Arc Min	−55°C to +125°C
Tracking Rate		20	rev/s	
Resolution		14 (1 LSB = 1.3 arc mins)	Bits	Output Coding Parallel Natural Binary
Repeatability		1	LSB	
Signal/Reference Frequency		400-2600	Hz	
Bandwidth		100	Hz	
SIGNAL INPUTS				
Signal Voltage		2, 11.8, 26, 90	V rms	See Ordering Information
Input Impedance				
90 V Signal		200	kΩ	Resistive, Tolerance ±2%
26 V Signal		58	kΩ	
11.8 V Signal		26	kΩ	
2 V Signal		4.4	kΩ	
Common Mode Rejection		74 (min)	dB	
Common Mode Range				
90 V Signal		±250	V dc	
26 V Signal		±120	V dc	
11.8 V Signal		±60	V dc	
2 V Signal		±12	V dc	
REFERENCE INPUTS				
Reference Voltage		2, 11.8, 26, 115	V rms	See Ordering Information
Input Impedance				
115 V Reference		270	kΩ	Resistive, Tolerance ±5%
26 V Reference		270	kΩ	
11.8 V Reference		25	kΩ	
2 V Reference		25	kΩ	
Common Mode Range				
115 V Reference		±210	V dc	
26 V Reference		±210	V dc	
11.8 V Reference		±35	V dc	
2 V Reference		±35	V dc	
ACCELERATION CONSTANT		62000	sec^{-2}	

Parameter	AD2S44	Units	Comments
STEP RESPONSE			
Large Step[1]	63 (typ), 75 (max)	ms	179° to 1 LSB of Error
Small Step[1]	25 (typ), 30 (max)	ms	2° to 1 LSB of Error
POWER LINES			
$+V_S$ = + 15V[1]	85 (typ), 100 (max)	mA	Quiescent Condition
$-V_S$ = −15 V[1]	55 (typ), 70 (max)	mA	Quiescent Condition
Power Dissipation	2.1 (typ), 2.6 (max)	W	Quiescent Condition
DIGITAL INPUTS			
$\overline{OE}$ V_{IL}	0.7 (max)	V dc	I_{IL} = 5 μA
V_{IH}	2.0 (min)	V dc	I_{IH} = 5 μA
A/$\overline{B}$ V_{IL}	0.7 (max)	V dc	I_{IL} = 1.2 mA
V_{IH}	2.0 (min)	V dc	I_{IH} = −60 μA
DIGITAL OUTPUTS (DB1–DB14)			
V_{OL}[1]	0.4 (max)	V dc	I_{IL} = 1.2 mA
V_{OH}[1]	2.4 (min)	V dc	I_{OH} = 60 μA
Tristate Leakage Current	±40	μA	
Drive Capability	3 (max)	LSTTL Loads	
DATA TRANSFER			See Figure 3
Time to Data Stable (After Negative Edge of $\overline{OE}$ or Change of Level of A/$\overline{B}$)	640 (max)	ns	t_S
Time to Data in High Impedance State (After Positive Edge of $\overline{OE}$)	200 (max)	ns	t_R
Time for Repetitive Strobing of Selected Channel	200 (min)	ns	t_P
BUILT-IN TEST OUTPUT (BIT)			
Sense	Active Low		Low = Error Condition
V_{OL}	0.4 (max)	V dc	I_{OL} = 3.2 mA
V_{OH}	2.4 (min)	V dc	I_{OH} = −160 μA
Drive Capability	8 (max)	LSTTL Loads	
Error Condition Set	55 (max)	LSB	
Error Condition Cleared	45 (min)	LSB	
DIMENSIONS	1.75 × 1.05 × 0.225	inch	See Package Information
	44.45 × 28.07 × 5.72	mm	
WEIGHT	0.65 (max)	oz	
	18.2 (max)	grams	

NOTES

[1]Specified over temperature range, −55°C to +125°C, and for: (a) ±10% signal and reference amplitude variation; (b) ±10% signal and reference harmonic distortion; (c) ±5% power supply variation; (d) ±10% variation in reference frequency.

Bold face type indicates parameters which are 100% tested at nominal values of power supplies, input signal voltages and operating frequency. All other parameters are guaranteed by design, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to GND . . . . . +17.25 V dc
$-V_S$ to GND . . . . . −17.25 V dc
Any Logic Input to GND (max) . . . . . +6.0 V dc
Any Logic Input to GND (min) . . . . . −0.4 V dc
Maximum Junction Temperature . . . . . +150°C
S1, S2, S3, S4 (Line to Line)[1]
  90 V Option . . . . . ±600 V dc
  26 V Option . . . . . ±160 V dc
  11.8 V Option . . . . . ± 80 V dc
  2 V Option . . . . . ±14 V dc
S1, S2, S3, S4 to GND
  90 V Option . . . . . ±600 V dc
  26 V Option . . . . . ±160 V dc
  11.8 V Option . . . . . ±80 V dc
  2 V Option . . . . . ±14 V dc
R_{HI} to R_{LO}
  26 V, 115 V Options . . . . . ±600 V dc
  2 V, 11.8 V Options . . . . . ±50 V dc
R_{HI}, R_{LO} to GND
  26 V, 115 V Options . . . . . ±600 V dc
  2 V, 11.8 V Options . . . . . ±50 V dc
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . −55°C to +125°C

NOTE
[1]On synchro input options, line-to-line voltage refers to the S2–S1, S1–S3 and S3–S2 differential voltages. On resolver input options line-to-line levels refer to the S1–S3 and S2–S4 voltages.

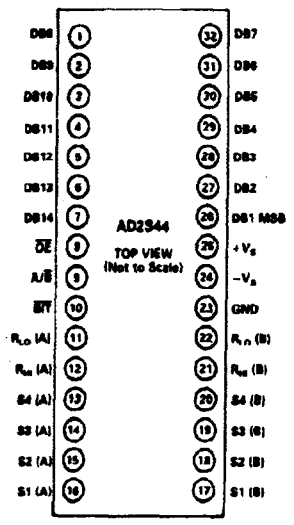
CAUTION

1. Absolute maximum ratings are the limits beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
3. The +15 V power supply must never go below GND.

Table I. Bit Weight Table

Bit Number	Weight (Degrees)
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0439
14 (LSB for 2S44)	0.0220

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

Pin	Mnemonic	Description
1–7	DB8–DB14	Parallel Output Data Bits
26–32	DB1–DB7	Parallel Output Data Bits
8	$\overline{OE}$	Output Enable Input
9	A/$\overline{B}$	Channel A or B Select Input
10	$\overline{BIT}$	Built-In Test Error Output
11	R_{LO} (A)	Input Pin for Channel A Reference Low
12	R_{HI} (A)	Input Pin for Channel A Reference High
13–16	S4–S1 (A)	Channel A Input Signal
17–20	S1–S4 (B)	Channel B Input Signal
21	R_{HI} (B)	Input Pin for Channel B Reference High
22	R_{LO} (B)	Input Pin for Channel B Reference Low
23	GND	Power Supply Ground (Note: This Pin Is Electrically Connected to the Case.)
24	$-V_S$	Negative Power Supply
25	$+V_S$	Positive Power Supply

ESD SENSITIVITY

The AD2S44 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model).

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

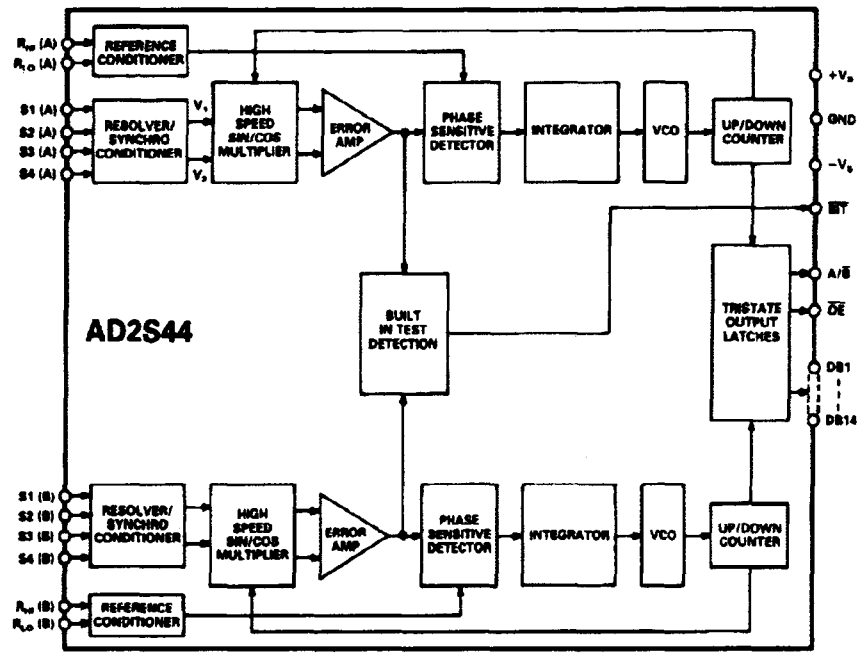


Figure 1. Functional Block Diagram of AD2S44

PRINCIPLES OF OPERATION

The AD2S44 series operate on a tracking principle. The output digital word continually tracks the position of the resolver/synchro shaft without the need for external convert commands and status wait loops. As the transducer moves through a position equivalent to the least significant bit weighting, the output digital word is updated.

A functional diagram of the AD2S44 is shown in Figure 1.

Each channel is identical in operation, sharing power supply and output pins. Both channels operate continuously and independently of each other–the digital output from either channel is available after switching the channel select and output enable inputs.

If the device is a synchro-to-digital converter, the 3-wire synchro output will be connected to S1, S2 and S3 on the unit, and a solid-state Scott-T input conditioner will convert these signals into resolver format, i.e.,

$$V_1 = K E_0 \sin \omega\tau \sin \theta$$
$$V_2 = K E_0 \sin \omega\tau \cos \theta$$

Where θ is the angle of the synchro shaft, $E_0 \sin \omega\tau$ is the reference signal and K is the transformation ratio of the input signal conditioner. If the unit is a resolver-to digital converter, the 4-wire resolver output will be connected directly to S1, S2, S3 and S4 on the unit.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ. V_1 is multiplied by $\cos\phi$ and V_2 is multiplied by $\sin\phi$ to give:

$$K E_0 \sin \omega\tau \sin \theta \cos \phi$$
$$K E_0 \sin \omega\tau \cos \theta \sin \phi.$$

These signals are subtracted by the error amplifier to give:

$$K E_0 \sin \omega\tau (\sin \theta \cos \phi - \cos \theta \sin \phi)$$

or

$$K E_0 \sin \omega\tau \sin (\theta - \phi).$$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null $\sin(\theta - \phi)$. When this is accomplished, the word state of the up-down counter, ϕ, equals, to within the rated accuracy of the converter, the synchro-resolver shaft angle, θ.

CONNECTING THE CONVERTER

The power supply voltages connected to $-V_S$ and $+V_S$ pins should be ± 15 V and must not be reversed.

It is suggested that a parallel combination of a 100 nF (ceramic) and a 6.8 μF (tantalum) capacitor be placed from each of the supply pins to GND.

The pin marked GND is connected electrically to the case and should be taken to the zero volt potential in the system.

The digital output is taken from Pins 26–32 and Pins 1–7. Pin 26 is the MSB, Pin 7 the LSB.

The reference connections are made to REF HI and REF LO. In the case of a synchro, the signals are connected to S1, S2 and S3 according to the following convention:

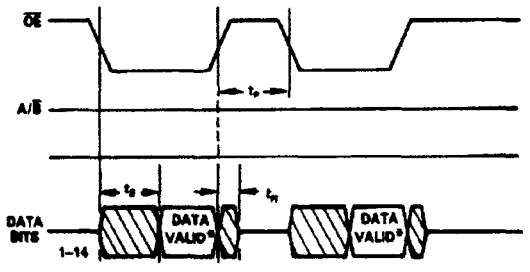
$$E_{S1\text{-}S3} = E_{RLO\text{-}RHI} \sin \omega\tau \sin \theta$$
$$E_{S3\text{-}S2} = E_{RLO\text{-}RHI} \sin \omega\tau \sin (\theta - 120°)$$
$$E_{S2\text{-}S1} = E_{RLO\text{-}RHI} \sin \omega\tau \sin (\theta - 240°).$$

For a resolver, the signals are connected to S1, S2, S3 and S4 according to the following convention:

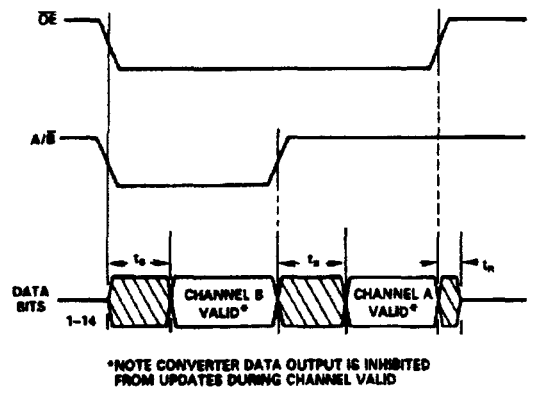
$$E_{S1\text{-}S3} = E_{RLO\text{-}RHI} \sin \omega\tau \sin \theta$$
$$E_{S2\text{-}S4} = E_{RLO\text{-}RHI} \sin \omega\tau \cos \theta$$

CHANNEL SELECT (A/$\overline{B}$)
A/$\overline{B}$ is the channel select input. A logic high selects channel A and a logic low selects channel B. Data becomes valid 640 ns after A/$\overline{B}$ is toggled. Timing information is shown in Figure 2.

OUTPUT ENABLE ($\overline{OE}$)
$\overline{OE}$ is the output enable input; the signal is active low. When set to a logic high, DB1 to DB14 are in the high impedance state. When $\overline{OE}$ is set to logic low, DB1 to DB14 represent the angle of the transducer shaft (see bit weights in Table I) to within the stated accuracy of the converter. Data becomes valid 640 ns after the $\overline{OE}$ is switched. Timing information is shown in Figure 2 and detailed in the "Data Transfer" section of SPECIFICATIONS.



a. Repetitive Reading of One Channel



b. Alternate Reading of Each Channel
Figure 2. AD2S44 Timing Diagrams

BUILT-IN TEST ($\overline{BIT}$)
$\overline{BIT}$ is the built-in test error output. This provides an over velocity or fault indication signal for the channel selected via A/$\overline{B}$. The error voltage of each channel is continuously monitored; and when the error exceeds ±50 bits for the currently selected channel, the $\overline{BIT}$ output goes low indicating that an error greater than approximately 1 angular degree exists and that the data is therefore invalid.

The $\overline{BIT}$ signal has a built-in hysterisis, i.e., the error required to set $\overline{BIT}$ is greater than that required for it to be cleared. $\overline{BIT}$ is set when the error exceeds 55 LSBs and is cleared when the error goes below 45 LSBs. This mode of operation guarantees that $\overline{BIT}$ will not flicker when the error threshold is crossed.

$\overline{BIT}$ is valid for the selected channel approximately 50 ns after the change in state of A/$\overline{B}$. In most instances, the error condition which sets $\overline{BIT}$ must persist for at least 1 period of the reference signal prior to $\overline{BIT}$ responding to the condition.

Conditions which cause the $\overline{BIT}$ output to show a fault are:

1. Power-Up Transient Response
   $\overline{BIT}$ will return to a logic high state after the AD2S44 position output synchronizes with the angle input to within 1 degree. Normally, $\overline{BIT}$ will be low at power-up for a period less than or equal to the large signal step response settling time of the AD2S44 after the $\pm V_S$ supplies have stabilized to within 5% of their final values.
2. Step Input > 1 Degree
   $\overline{BIT}$ will return to a logic high state after the selected channel of the AD2S44 has settled to with 1 degree of the input angle resulting from an instantaneous step.
3. Excessive Velocity
   $\overline{BIT}$ will be driven to a logic low if the maximum tracking rate of the AD2S44 is exceeded (20 RPS typical).
4. Signal Failure
   $\overline{BIT}$ may be driven to a logic low state if all signal voltages to the selected channel are lost.
5. Converter/System Failure
   Any failure which causes the AD2S44 to fail to track the input synchro/resolver angles will drive $\overline{BIT}$ to a logic low. This may include, but is not necessarily limited to, acceleration conditions, poor supply voltage regulation or excessive noise on the signal connections.

SCALING FOR NONSTANDARD SIGNALS
A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate nonstandard input signal and reference voltages which are outside the nominal ±10% limits of the converter. Using this technique, it is possible to use a standard converter with a "personality card" in systems where a wide range of input and reference voltages are encountered.

NOTE: The accuracy of the converter will be affected by the matching accuracies of resistors used for external scaling. For resolver format options, it is critical that the value of the resistors on the S1–S3 signal input pair be precisely matched to the S4–S2 input pair. For synchro options, the three resistors on S1, S2, S3 must be matched. In general, a 0.1% mismatch between resistor values will contribute an additional 1.7 arc minutes of error to the conversion. In addition, imbalances in resistor values can greatly reduce the common mode rejection ratio of the signal inputs.

To calculate the values of the external scaling resistors add 2.222 kΩ extra per volt of signal in series with S1, S2, S3 and S4 (no resistor required on S4 for synchro options), and 3 kΩ in extra per volt of reference in series with R_{LO} and R_{HI}.

DYNAMIC PERFORMANCE
The transfer function of the converter is given below.

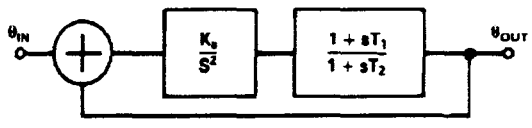


Figure 3. Transfer Function of AD2S44

Open loop transfer function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{s^2} \cdot \frac{1 + sT_1}{1 + sT_2}$$

Closed loop transfer function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + s^2/K_a + s^3\, T_2/K_a}$$

where K_a = 62000 sec^{-2}
T_1 = 0.0061 sec
T_2 = 0.001 sec.

The gain and phase diagrams are shown in Figures 4 and 5.

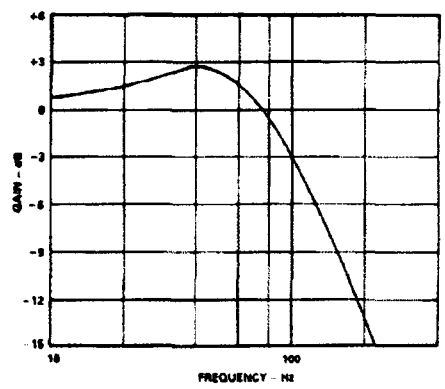


Figure 4. AD2S44 Gain Plot

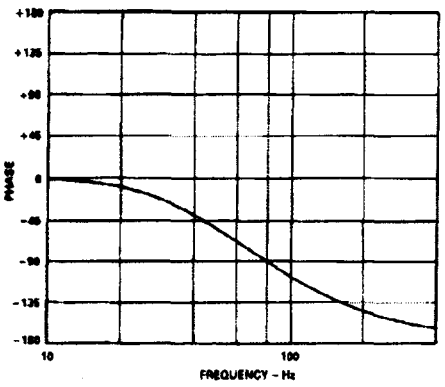


Figure 5. AD2S44 Phase Plot

ACCELERATION ERROR

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{Input\ Acceleration}{Error\ in\ Output\ Angle}$$

The numerator and denominator must have consistant angular units. For example, if K_a is in sec^{-2}, then the input acceleration may be specified in degrees/sec^2 and the error in output angle in degrees. Alternatively, the angular unit of measure may be in radians, minutes of arc, LSBs, etc.

K_a does not define maximum acceleration, only the error due to acceleration. The maximum acceleration for which the AD2S44 will not lose track is on the order of 5° × K_a = 310,000 °/sec^2 or about 800 revolutions/sec^2.

K_a can be used to predict the output position error due to input acceleration. For eaxample, for an acceleration of 50 revolutions/sec^2 with K_a = 62000,

$$\text{Error in LSBs} = \frac{\text{Input Acceleration [LSB/sec}^2\text{]}}{K_a\ [sec^{-2}]}$$

$$= \frac{50\ [rev/sec^2] \cdot 2^{14}\ [LSB/rev]}{62000\ [sec^{-2}]} = 13.2\ LSBs.$$

RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available on request.

Figure 6 shows the MTBF in years vs. case temperature for Naval Sheltered conditions calculated in accordance with MIL-HDBK-217E.

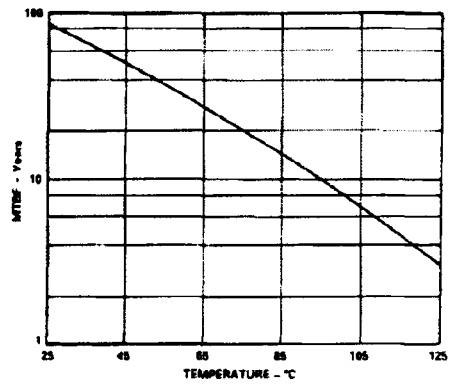
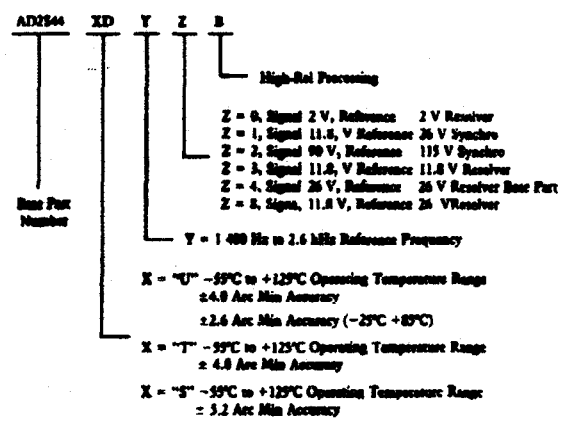


Figure 6. 2S44 MTBF vs. Temperature

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by a two letter code defining the accuracy grade, and a two digit numeric code defining the signal/reference voltage and frequency. All the standard options and their option codes are shown below. For nonstandard configurations, please contact Analog Devices.

For example, the correct part number for a component to operate with 90 V signal, 115 V reference synchro format inputs and yield a ±5.2 arc minute accuracy over the −55°C to +125° temperature range would be AD2S44SM12. The same part, processed to high reliability standards would carry the designator AD2S44SM12B.



OTHER PRODUCTS

Many other products concerned with the conversion of synchro/resolver data are manufactured by Analog Devices, some of which are listed below.

The SDC/RDC1740/41/42 are hybrid synchro/resolver to digital converters with internal isolating micro transformers.

The SDC/RDC1767/68 are identical to the SDC/RDC1740 series but with the additional features of analog velocity output and dc error output.

The OSC1758 is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts. The device operates over a frequency range of 1 kHz to 10 kHz.

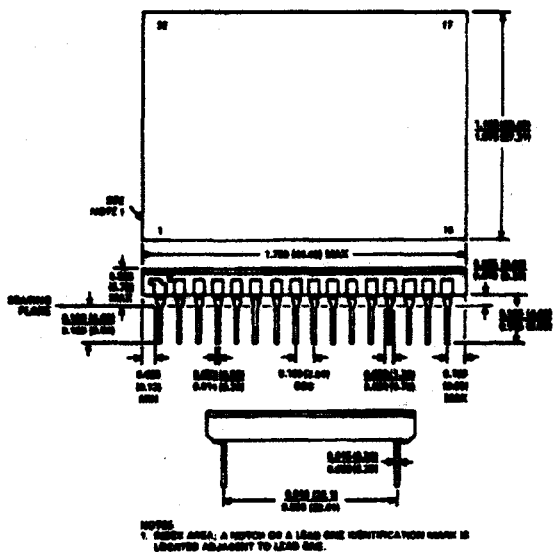
The DRC1745 and DRC1746 are 14- and 16-bit natural binary latched output high power hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc minutes, and the outputs can supply 2 VA at 7 V rms. Transformers are available to convert the output to synchro or resolver format at high voltage levels.

The AD2S65/66 are similar to the DRC1745/46 but do not include the power output stage. These devices are available in accuracy grades to 1 arc minute.

The 2S80 series are monolithic ICs performing resolver to digital conversion with accuracies up to ±2 arc minutes and 16-bit resolution.

OUTLINE DIMENSION

Dimensions shown in inches and (mm).



NOTES
1. INDEX AREA; A NOTCH OR A LEAD ONE IDENTIFICATION MARK IS LOCATED ADJACENT TO LEAD ONE.