Nonvolatile Memory, Dual 1024-Position Digital Potentiometers

AD5235*

FEATURES
Dual, 1024-Position Resolution
25 kΩ, 250 kΩ Nominal Resistance
Low Temperature Coefficient: 35 ppm/°C
Nonvolatile Memory[1] Preset Maintains Wiper Settings
Permanent Memory Write-Protection
Wiper Settings Read Back
Resistance Tolerance Stored in EEMEM[1]
Linear Increment/Decrement
Log Taper Increment/Decrement
SPI-Compatible Serial Interface
3 V to 5 V Single Supply or ±2.5 V Dual Supply
26 Bytes User Nonvolatile Memory for Constant Storage
100-Year Typical Data Retention T_A = 55°C

APPLICATIONS
SONET, SDH, ATM, Gigabit Ethernet
DWDM Laser Diode Driver, Optical Supervisory Systems
Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Programmable Voltage to Current Conversion
Programmable Filters, Delays, Time Constants
Line Impedance Matching
Power Supply Adjustment
Low Resolution DAC Replacement

GENERAL DESCRIPTION
The AD5235 provides a dual channel, digitally controlled digital potentiometer[2] with resolution of 1024 positions. These devices perform the same electronic adjustment function as a mechanical potentiometer with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance. The AD5235's versatile programming via a standard serial interface allows 16 modes of operation and adjustment, including scratch pad programming, memory storing and retrieving, increment/decrement, log taper adjustment, wiper setting readback, and extra user-defined EEMEM.

Another key feature of the AD5235 is that the actual resistance tolerance is stored in the EEMEM. The actual end-to-end resistance can therefore be known, which is valuable for calibration, tolerance matching and precision applications.

In the scratch pad programming mode, a specific setting can be programmed directly to the RDAC[2] register, which sets the resistance between terminals W–A and W–B. The RDAC register can also be loaded with a value previously stored in the EEMEM register. The value in the EEMEM can be changed or protected.
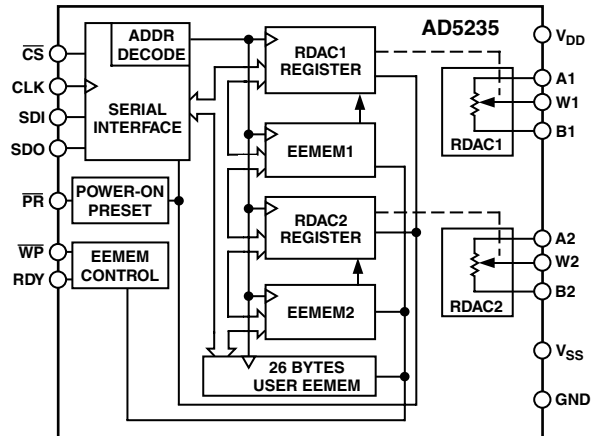
*Patent pending

NOTES
[1]The terms nonvolatile memory and EEMEM are used interchangeably.
[2]The terms digital potentiometer and RDAC are used interchangeably.

FUNCTIONAL BLOCK DIAGRAM

When changes are made to the RDAC register, the value of the new setting can be saved into the EEMEM. Thereafter, it will be transferred automatically to the RDAC register during system power ON, which is enabled by the internal preset strobe. EEMEM can also be retrieved through direct programming and external preset pin control.

The linear step increment and decrement commands cause the setting in the RDAC register to be moved UP or DOWN, one step at a time. For logarithmic changes in wiper setting, a left/right bit shift command adjusts the level in ±6 dB steps.

The AD5235 is available in a thin TSSOP-16 package. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C.
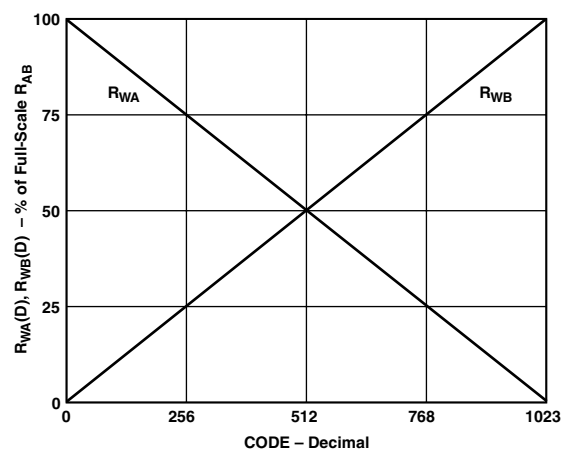

Figure 1. (D) and R_{WB}(D) vs. Decimal Code

REV. A

AD5235–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, 25 kΩ AND 250 kΩ VERSIONS

(V_{DD} = 3 V to 5.5 V, –40°C < T_A < +85°C, unless otherwise noted.[1])

Parameter	Symbol	Conditions	Min	Typ[2]	Max	Unit
DC CHARACTERISTICS–RHEOSTAT MODE Specifications Apply to All RDACs						
Resistor Differential Nonlinearity[3]	R-DNL	R_{WB}	–2		+2	LSB
Resistor Integral Nonlinearity[3]	R-INL	R_{WB}	–4		+4	LSB
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$			35		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V, I_W = 1 V/R_{WB}, Code = 200$_H$		50	100	Ω
		V_{DD} = 3 V, I_W = 1 V/R_{WB}, Code = 200$_H$		200		Ω
Channel Resistance Matching	$\Delta R_{WB}/R_{WB}$	Ch 1 and 2 R_{WB}, Dx = 3 FF$_H$		0.1		%
Nominal Resistor Tolerance	ΔR_{WB}	Dx = 3 FF$_H$	–30		+30	%
DC CHARACTERISTICS–POTENTIOMETER DIVIDER MODE Specifications Apply to All VRs						
Resolution	N		10			Bits
Differential Nonlinearity[4]	DNL		–2		+2	LSB
Integral Nonlinearity[4]	INL		–4		+4	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = Half Scale		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = Full Scale	–6		0	LSB
Zero-Scale Error	V_{WZSE}	Code = Zero Scale	0		4	LSB
RESISTOR TERMINALS						
Terminal Voltage Range[5]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[6] Ax, Bx	$C_{A, B}$	f = 1 MHz, measured to GND, Code = Half Scale		11		pF
Capacitance[6] Wx	C_W	f = 1 MHz, measured to GND, Code = Half Scale		80		pF
Common-Mode Leakage Current[6, 7]	I_{CM}	V_W = V_{DD}/2		0.01	±2	μA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	With respect to GND, V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	With respect to GND, V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = 3 V			0.6	V
Input Logic High	V_{IH}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = –2.5 V	2.0			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = –2.5 V			0.5	V
Output Logic High (SDO, RDY)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to 5 V	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{DD}			±2.25	μA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0V	3.0		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = GND, T_A = 25°C		2	4.5	μA
Positive Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = GND		3.5	6.0	μA
Programming Mode Current	$I_{DD(PG)}$	V_{IH} = V_{DD} or V_{IL} = GND		35		mA
Read Mode Current[8]	$I_{DD(XFR)}$	V_{IH} = V_{DD} or V_{IL} = GND	0.3	3	9	mA
Negative Supply Current	I_{SS}	V_{IH} = V_{DD} or V_{IL} = GND, V_{DD} = +2.5 V, V_{SS} = – 2.5 V		3.5	6.0	μA
Power Dissipation[9]	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = GND		18	50	μW
Power Supply Sensitivity[6]	P_{SS}	ΔV_{DD} = 5 V ± 10%		0.002	0.01	%/%

REV. A

Parameter	Symbol	Conditions	Min	Typ[2]	Max	Unit
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth –3 dB	BW	$V_{DD}/V_{SS} = \pm2.5$ V, $R_{AB} = 25$ kΩ/250 kΩ		125/12		kHz
Total Harmonic Distortion	THD_W	$V_A = 1$ Vrms, $V_B = 0$ V, f =1 kHz		0.05		%
V_W Settling Time	t_S	$V_A = V_{DD}$, $V_B = 0$ V, $V_W = 0.50\%$ Error Band, Code 000_H to 200_H, $R_{AB} = 25$ kΩ/250 kΩ		4/36		µs
Resistor Noise Spectral Density	e_{N_WB}	$R_{AB} = 25$ kΩ/250 kΩ, $T_A = 25°C$		20/64		nV/$\sqrt{Hz}$
Crosstalk (C_{W1}/C_{W2})	C_T	$V_A = V_{DD}$, $V_B = 0$ V, Measured V_{W1} with V_{W2} Making Full-Scale Change		90/21		nV–s
Analog Crosstalk	C_{TA}	$V_{DD} = V_{A1} = +2.5$ V, $V_{SS} = V_{B1} = -2.5$ V, Measure V_{W1} with $V_{W2} = 5$ V p-p @ f = 1 kHz, Code 1 = 200_H, Code 2 = 3 FF_H, $R_{AB} = 25$ kΩ/250 kΩ		–81/–62		dB
INTERFACE TIMING CHARACTERISTICS Applies to All Parts[6, 11]						
Clock Cycle Time (t_{CYC})	t_1		20			ns
$\overline{CS}$ Setup Time	t_2		10			ns
CLK Shutdown Time to $\overline{CS}$ Rise	t_3		1			t_{CYC}
Input Clock Pulsewidth	t_4, t_5	Clock Level High or Low	10			ns
Data Setup Time	t_6	From Positive CLK Transition	5			ns
Data Hold Time	t_7	From Positive CLK Transition	5			ns
$\overline{CS}$ to SDO-SPI Line Acquire	t_8				40	ns
$\overline{CS}$ to SDO-SPI Line Release	t_9				50	ns
CLK to SDO Propagation Delay[12]	t_{10}	$R_P = 2.2$ kΩ, $C_L < 20$pF			50	ns
$\overline{CS}$ High Pulsewidth[13]	t_{12}		10			ns
$\overline{CS}$ High to $\overline{CS}$ High[13]	t_{13}		4			t_{CYC}
RDY Rise to $\overline{CS}$ Fall	t_{14}		0			ns
$\overline{CS}$ Rise to RDY Fall Time	t_{15}			0.15	0.3	ms
Read/Store to Nonvolatile EEMEM[14]	t_{16}	Applies to Command 2_H, 3_H, 9_H		30		ms
$\overline{CS}$ Rise to Clock Rise/Fall Setup	t_{17}		10			ns
Preset Pulsewidth (Asynchronous)	t_{PRW}	Not Shown in Timing Diagram	50			ns
Preset Response Time to Wiper Setting	t_{PRESP}	$\overline{PR}$ Pulsed Low to Refreshed Wiper Positions		140		µs
FLASH/EE MEMORY RELIABILITY						
Endurance[15]			100			K Cycles
Data Retention[16]				100		Years

NOTES

[1] Parts can be operated at 2.7 V single supply, except from 0°C to –40°C where minimum 3 V is needed.

[2] Typicals represent average readings at 25°C and $V_{DD} = 5$ V.

[3] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. $I_W \sim 50$ mA for $V_{DD} = 2.7$ V and $I_W \sim 400$ mA for $V_{DD} = 5$ V. See Test Circuit 1.

[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. VA = V_{DD} and VB = V_{SS}. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions. See Test Circuit 2.

[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar ac signal adjustment.

[6] Guaranteed by design and not subject to production test.

[7] Common-mode leakage current is a measure of the dc leakage from any terminal B and W to a common-mode bias level of $V_{DD}/2$.

[8] Transfer (XFR) mode current is not continuous. Current consumed while EEMEM locations are read and transferred to the RDAC register. See TPC 19.

[9] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.

[10] All dynamic characteristics use $V_{DD} = +2.5$ V and $V_{SS} = -2.5$ V.

[11] See Timing Diagrams for location of measured values. All input control voltages are specified with tR = tF = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both $V_{DD} = 3$ V and 5 V.

[12] Propagation delay depends on value of V_{DD}, R_{PULL_UP}, and C_L.

[13] Valid for commands that do not activate the RDY pin.

[14] RDY pin low only for commands 2, 3, 8, 9, 10, and PR software pulse: CHD_8 ~ 1 ms; CHD_9, 10 ~ 0.1 ms; CHD_2, 3 ~ 20 ms. Device operational at $T_A = -40°C$ and $V_{DD} < 3$ V extends the save time to 35 ms.

[15] Endurance is qualified to 100,000 cycles as per JEDEC Standard 22, Method A117 and measured at –40°C, +25°C, and +85°C. Typical endurance at +25°C is 700,000 cycles.

[16] Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 0.6 V derates with junction temperature in the Flash/EE memory. See General Description section.

Specifications subject to change without notice.

The AD5235 contains 16,000 transistors. Die size: 99 mil × 103 mil, 10,197 square mil.
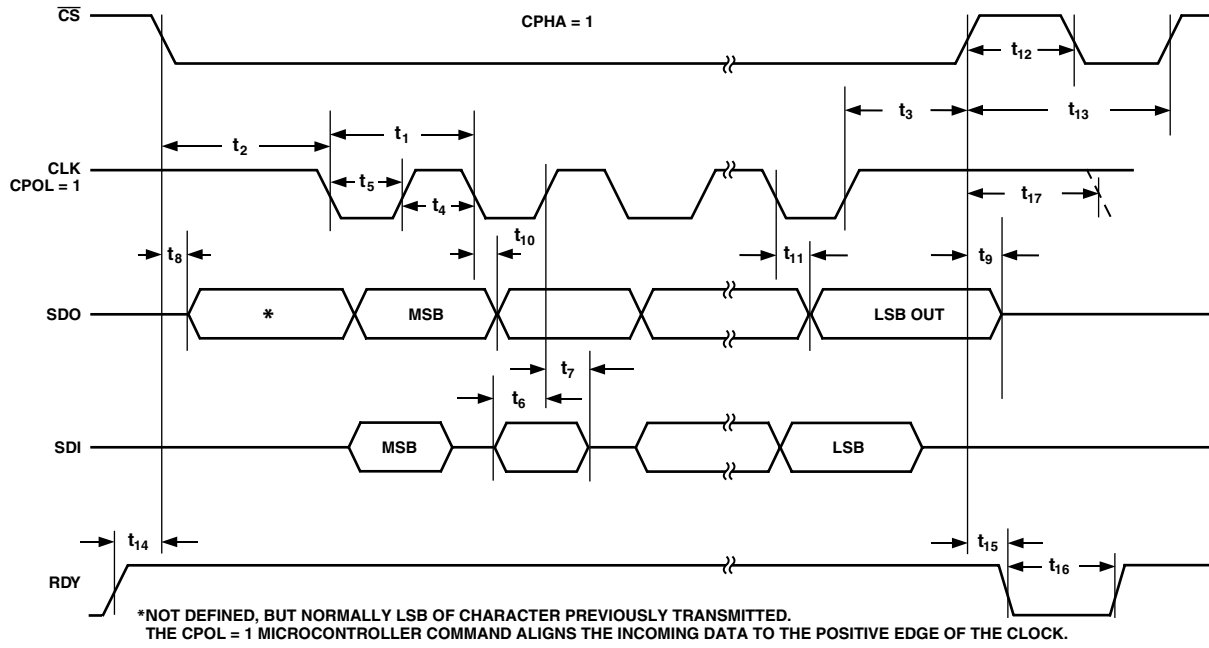
AD5235

TIMING DIAGRAMS
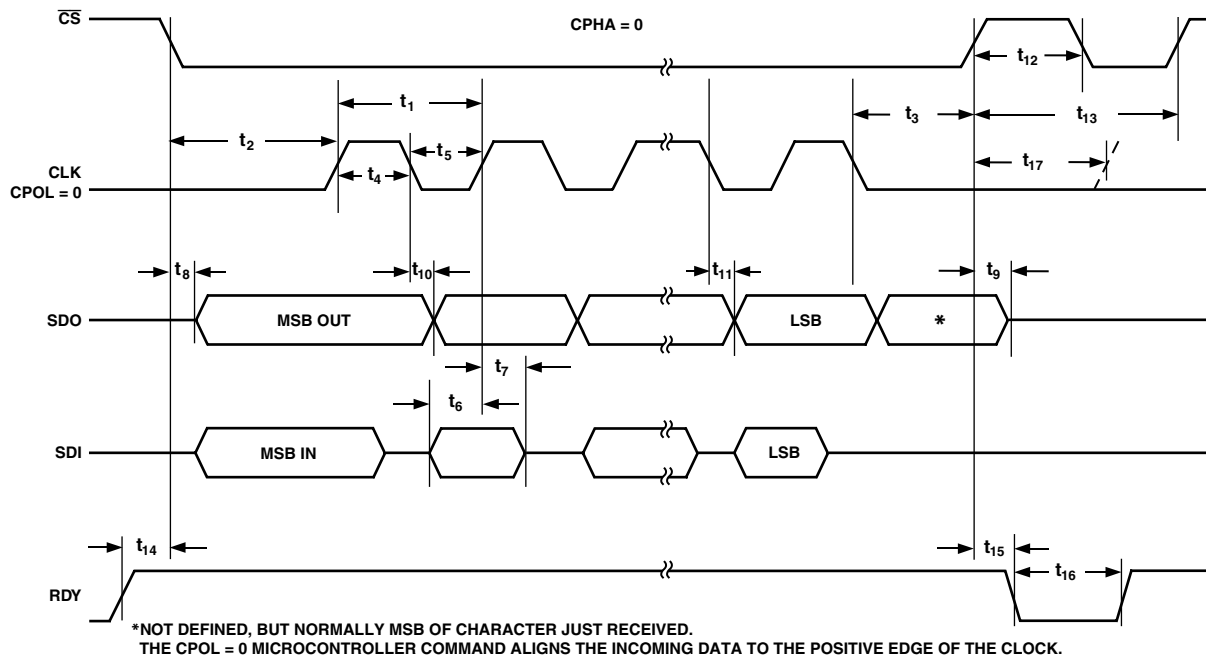

Figure 2a. CPHA = 1 Timing Diagram

Figure 2b. CPHA = 0 Timing Diagram

REV. A

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND . . . . −0.3 V, +7 V
V_{SS} to GND . . . . +0.3 V, −7 V
V_{DD} to V_{SS} . . . . +7 V
V_A, V_B, V_W to GND . . . . V_{SS} − 0.3 V, V_{DD} + 0.3 V
I_A, I_B, I_W
    Intermittent[2] . . . . ±20 mA
    Continuous . . . . ±2 mA
Digital Inputs and Output Voltage to GND . . −0.3 V, V_{DD} + 0.3 V
Operating Temperature Range[3] . . . . −40°C to +85°C
Maximum Junction Temperature ($T_{J MAX}$) . . . . 150°C
Storage Temperature . . . . −65°C to +150°C
Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . 215°C
    Infrared (15 sec) . . . . 220°C

Thermal Resistance Junction-to-Ambient θ_{JA}
    TSSOP-16 . . . . 150°C/W
Thermal Resistance Junction-to-Case θ_{JC}
    TSSOP-16 . . . . 28°C/W
    Package Power Dissipation = ($T_{J MAX}$ − T_A)/θ_{JA}

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[3] Includes programming of nonvolatile memory.

ORDERING GUIDE

Model	R_{WB_FS} kΩ	RDNL	RINL	Temperature Range (°C)	Package Description	Package Option	Ordering Quantity	Top Mark*
AD5235BRU25	25	±2	±4	−40 to +85	TSSOP-16	RU-16	96	5235B25
AD5235BRU25-RL7	25	±2	±4	−40 to +85	TSSOP-16	RU-16	1,000	5235B25
AD5235BRU250	250	±2	±4	−40 to +85	TSSOP-16	RU-16	96	5235BD
AD5235BRU250-RL7	250	±2	±4	−40 to +85	TSSOP-16	RU-16	1,000	5235BD
AD5235EVAL25	25						1	
AD5235EVAL250	250						1	

*Line 1 contains ADI logo symbol and date code YYWW, line 2 branding contains differentiating detail by part type.
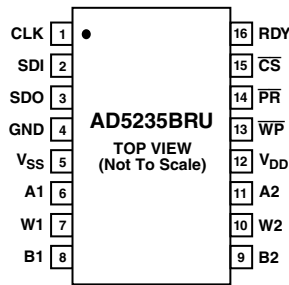
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5235 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

AD5235

PIN CONFIGURATION

```
        ┌─────────────────┐
CLK  1  │ ●               │ 16  RDY
SDI  2  │                 │ 15  C̄S̄
SDO  3  │                 │ 14  P̄R̄
GND  4  │   AD5235BRU     │ 13  W̄P̄
        │   TOP VIEW      │
Vss  5  │  (Not To Scale) │ 12  VDD
A1   6  │                 │ 11  A2
W1   7  │                 │ 10  W2
B1   8  │                 │  9  B2
        └─────────────────┘
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PIN FUNCTION DESCRIPTIONS

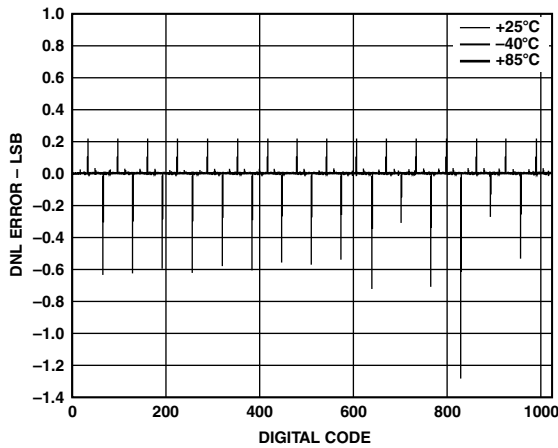| Pin No.	Mnemonic	Description
1	CLK	Serial Input Register Clock Pin. Shifts in one bit at a time on positive clock edges.
2	SDI	Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loads first.
3	SDO	Serial Data Output Pin. Open-drain output requires external pull-up resistor. CMD_9 and CMD_10 activate the SDO output. See Table II, Command Operation Truth Table. Other commands shift out the previously loaded SDI bit pattern delayed by 24 clock pulses. This allows daisy-chain operation of multiple packages.
4	GND	Ground Pin, Logic Ground Reference
5	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications.
6	A1	A Terminal of RDAC1
7	W1	Wiper Terminal of RDAC1. ADDR(RDAC1) = 0_H.
8	B1	B Terminal of RDAC1
9	B2	B Terminal of RDAC2
10	W2	Wiper Terminal of RDAC2. ADDR(RDAC2) = 1_H.
11	A2	A Terminal of RDAC2
12	V_{DD}	Positive Power Supply Pin
13	$\overline{WP}$	Write Protect Pin. When active low, $\overline{WP}$ prevents any changes to the present contents, except $\overline{PR}$ strobe. CMD_1 and CMD_8 will refresh the RDAC register from EEMEM. Execute a NOP command before returning to $\overline{WP}$ high.
14	$\overline{PR}$	Hardware Override of Preset Pin. Refreshes the scratch pad register with current contents of the EEMEM register. Factory default to midscale 512_{10} until EEMEM loaded with a new value by the user ($\overline{PR}$ is activated at the logic high transition).
15	$\overline{CS}$	Serial Register Chip Select Active Low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
16	RDY	Ready. Active-high open-drain output. Identifies completion of commands 2, 3, 8, 9, 10, and $\overline{PR}$.
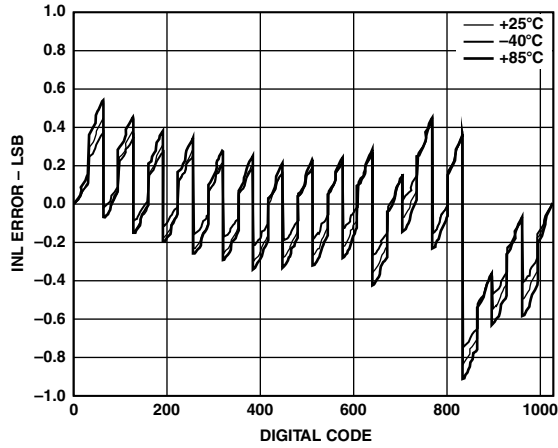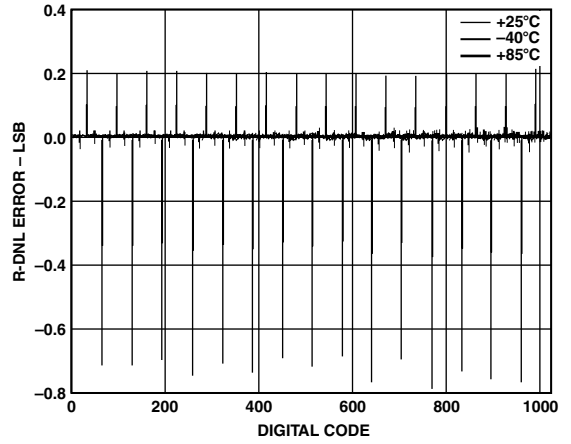
TPC 1. INL vs. Code, $T_A = -40°C$, $+25°C$, $+85°C$ Overlay, $R_{AB} = 25 k\Omega$

TPC 2. DNL vs. Code, $T_A = -40°C$, $+25°C$, $+85°C$ Overlay, $R_{AB} = 25 k\Omega$

TPC 3. RINL vs. Code, $T_A = -40°C$, $+25°C$, $+85°C$ Overlay, $R_{AB} = 25 k\Omega$

TPC 4. R-DNL vs. Code, $T_A = -40°C$, $+25°C$, $+85°C$ Overlay, $R_{AB} = 25 k\Omega$
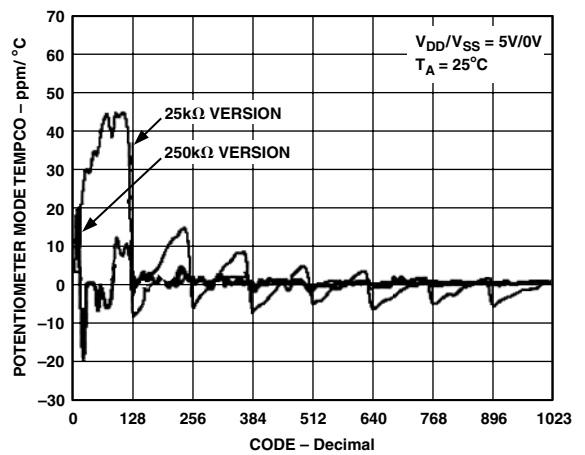
TPC 5. $\Delta V_{WB}/\Delta T$ Potentiometer Mode Tempco
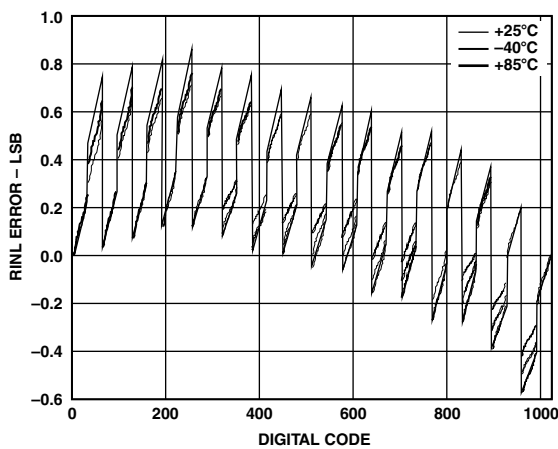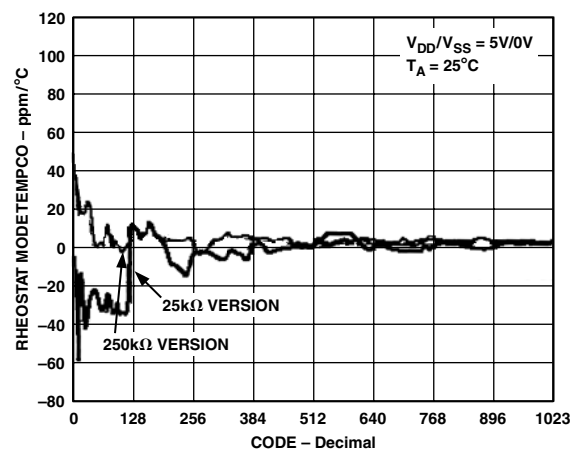
TPC 6. $\Delta R_{WB}/\Delta T$ Rheostat Mode Tempco

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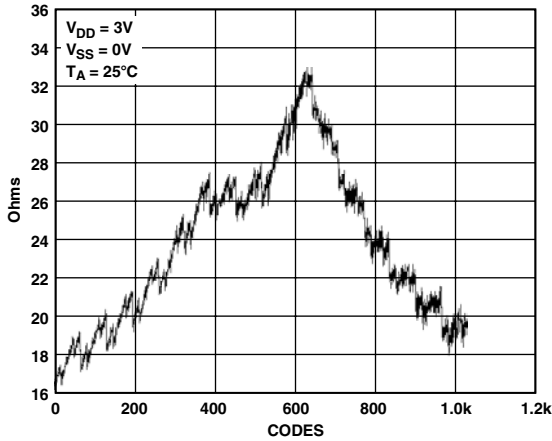
TPC 7. Wiper ON Resistance vs. Code
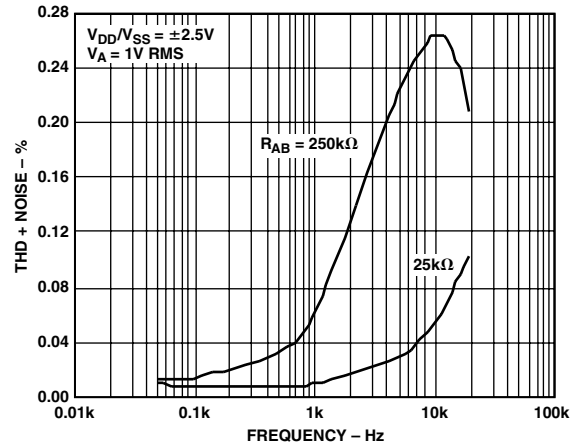
TPC 10. Total Harmonic Distortion vs. Frequency
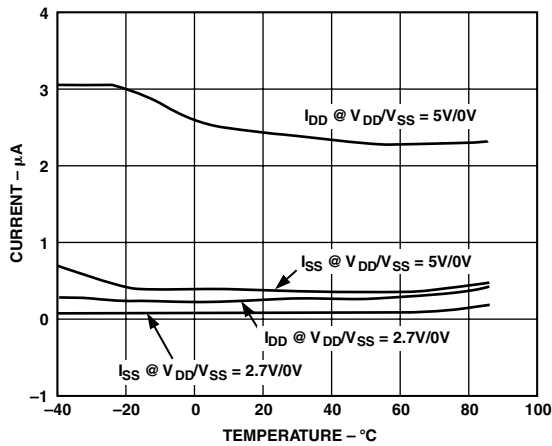
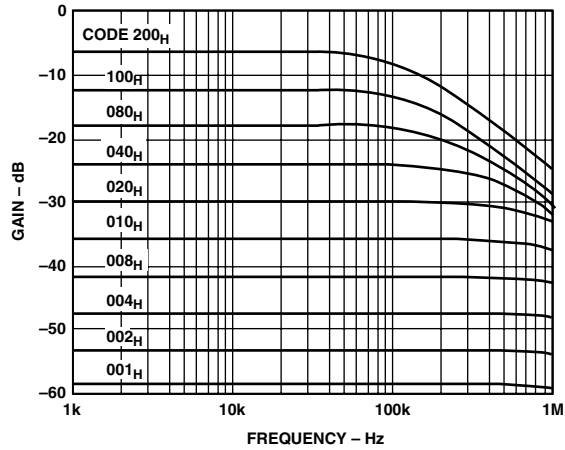TPC 8. I_{DD} vs. Temperature, $R_{AB} = 25\ k\Omega$
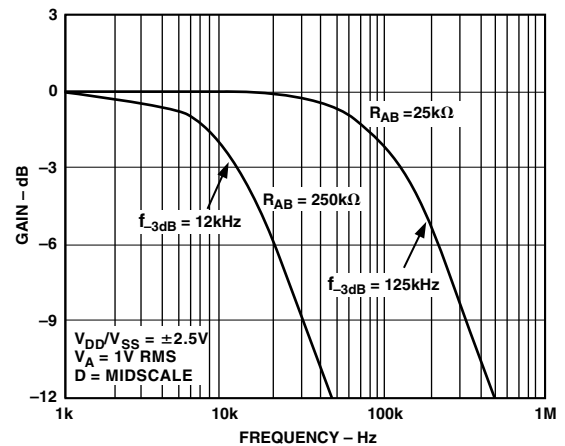
TPC 11. –3 dB Bandwidth vs. Resistance
(Test Circuit 7)
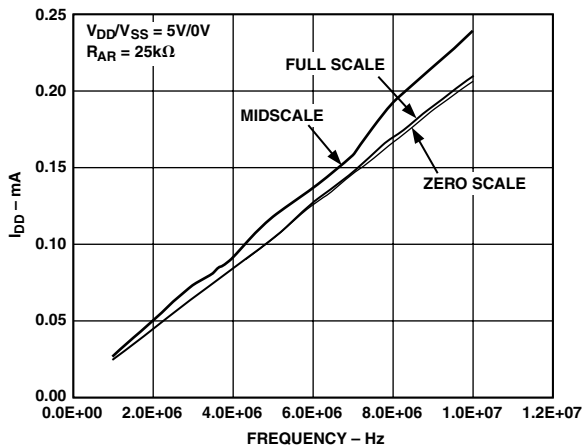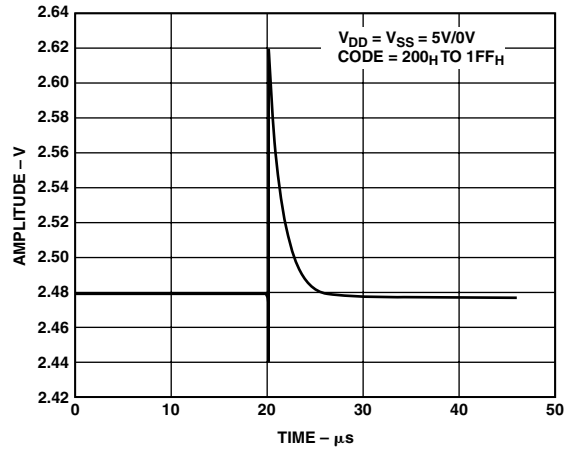

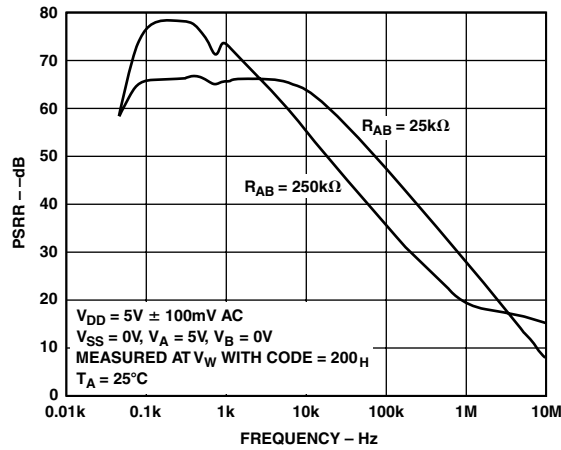TPC 9. I_{DD} vs. Clock Frequency, $R_{AB} = 25\ k\Omega$
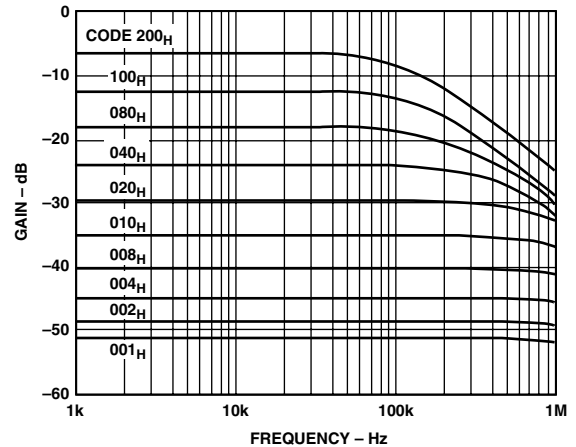
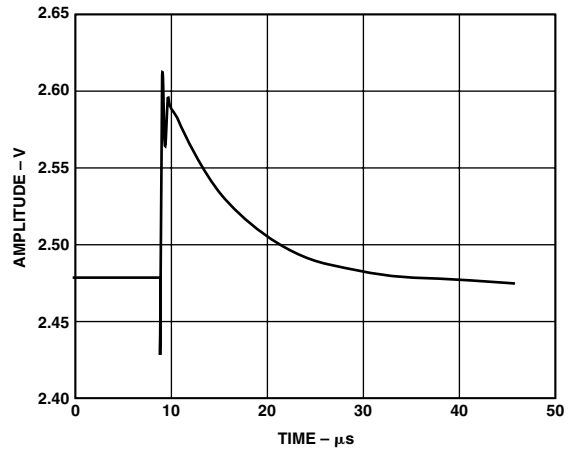TPC 12. Gain vs. Frequency vs. Code, $R_{AB} = 25\ k\Omega$
(Test Circuit 7)

REV. A

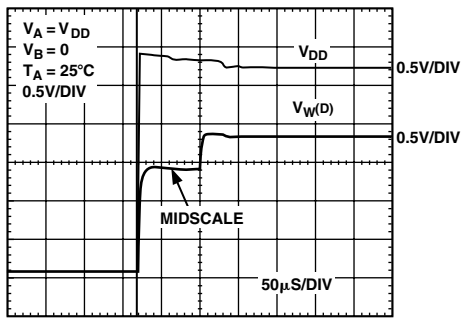TPC 13. Gain vs. Frequency vs. Code, R_{AB} = 250 kΩ (Test Circuit 7)

TPC 14. PSRR vs. Frequency

TPC 15. Power-On Reset, V_{DD} = 2.25 V, Previously Stored Code, D = 2AA $_H$

TPC 16. Midscale Glitch Energy, R_{AB} = 25 kΩ, Code 200_H to 1 FF_H

TPC 17. Midscale Glitch Energy, R_{AB} = 250 kΩ, Code 200_H to 1 FF_H
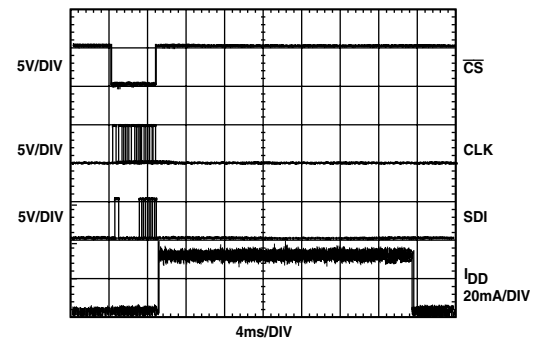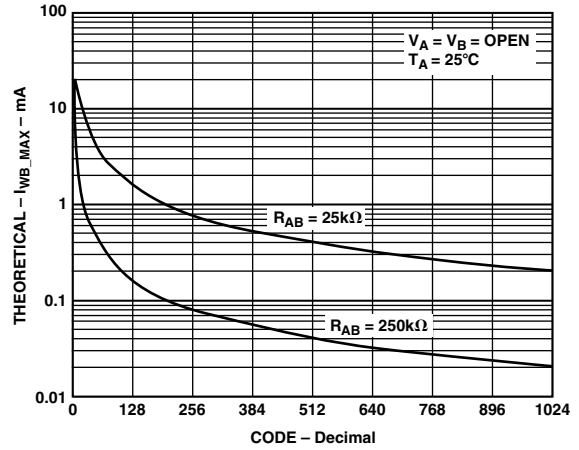

TPC 18. I_{DD} vs. Time (Save) Program Mode

AD5235
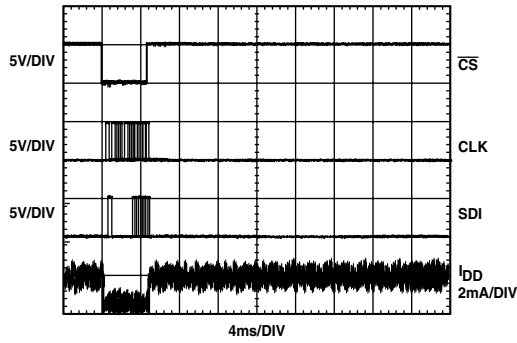
*SUPPLY CURRENT RETURNS TO MINIMUM POWER
CONSUMPTION IF INSTRUCTION #0 (NOP) IS EXECUTED
IMMEDIATELY AFTER INSTRUCTION #1 (READ EEMEM)

TPC 19. I_{DD} vs. Time (Read) Program Mode*

TPC 20. I_{WB_MAX} vs. Code

TEST CIRCUITS

Test Circuits 1 to 10 define the test conditions used in the product specification table.
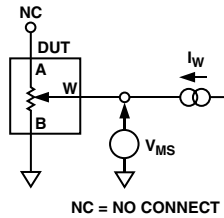
*Test Circuit 1. Resistor Position Nonlinearity
Error (Rheostat Operation; R-INL, R-DNL)*

*Test Circuit 2. Potentiometer Divider
Nonlinearity Error (INL, DNL)*

Test Circuit 3. Wiper Resistance

$V+ = V_{DD} \pm 10\%$

$PSRR (dB) = 20\ LOG \left(\dfrac{\Delta V_{MS}}{\Delta V_{DD}} \right)$

$PSS (\%/\%) = \dfrac{\Delta V_{MS}\%}{\Delta V_{DD}\%}$

Test Circuit 4. Power Supply Sensitivity (PSS, PSRR)

Test Circuit 5. Inverting Gain
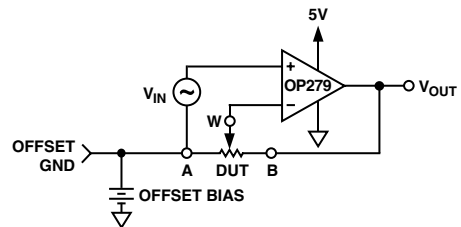
Test Circuit 6. Noninverting Gain

REV. A

TEST CIRCUITS (continued)
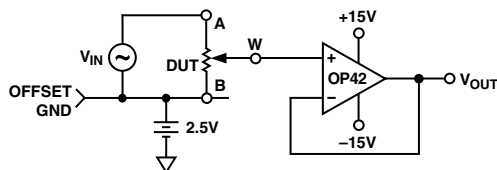
Test Circuit 7. Gain vs. Frequency
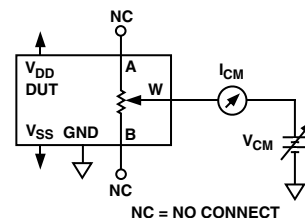
Test Circuit 9. Common-Mode Leakage Current
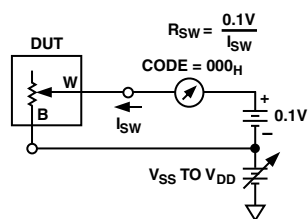
Test Circuit 8. Incremental ON Resistance

Test Circuit 10. Analog Crosstalk

OPERATIONAL OVERVIEW

The AD5235 digital potentiometer is designed to operate as a true variable resistor. The resistor wiper position is determined by the RDAC register contents. The RDAC register acts as a scratch pad register that allows unlimited changes of resistance settings. The scratch pad register can be programmed with any position setting using the standard SPI serial interface by loading the 24-bit data-word. The format of the data-word is that the first 4 bits are commands, the following 4 bits are addresses, and the l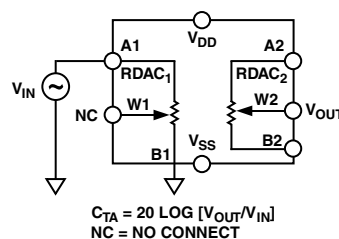ast 16 bits are data. Once a specific value is set, this value can be saved into a corresponding EEMEM register. During subsequent power-up, the wiper setting will automatically be loaded at that value. Saving data to the EEMEM takes about 25 ms and consumes approximately 20 mA. During this time, the shift register is locked, preventing any changes from taking place. The RDY pin indicates the completion of this EEMEM saving process. There are also 13 addresses, with 2 bytes each, of user-defined data that can be stored in EEMEM.

OPERATION DETAIL

There are 16 commands that facilitate users' programming needs. Refer to Table II. The commands are:

 0. Do Nothing
 1. Restore EEMEM Setting to RDAC
 2. Save RDAC Setting to EEMEM
 3. Save User Data or RDAC Setting to EEMEM
 4. Decrement 6 dB
 5. Decrement All 6 dB
 6. Decrement One Step

 7. Decrement All One Step
 8. Reset EEMEM Setting to RDAC
 9. Read EEMEM to SDO
10. Read Wiper Setting to SDO
11. Write Data to RDAC
12. Increment 6 dB
13. Increment All 6 dB
14. Increment One Step
15. Increment All One Step

Tables X to XVI provide programming examples by using some of these commands.

Scratch Pad and EEMEM Programming

The basic mode of setting the digital potentiometer wiper position (programming the scratch pad register) is accomplished by loading the serial data input register with the command 11, the corresponding address, and the data. Since the scratch pad register is a standard logic register, there is no restriction on the number of changes allowed. When the desired wiper position is determined, the user can load the serial data input register with the command 2, which stores the setting into the corresponding EEMEM register. The EEMEM value can be changed at any time or permanently protected by activating the $\overline{WP}$ command. Table III provides a programming example listing the sequence of serial data input (SDI) words and the corresponding serial data output (SDO) in hexadecimal format.

AD5235

Table I. 24-Bit Serial Data-Word

	MSB		Command Byte 0						Data Byte 1								Data Byte 0							LSB
RDAC	C3	C2	C1	C0	0	0	0	A0	X	X	X	X	X	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EEMEM	C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Command bits are C0 to C3. Address bits are A3 to A0. Data bits D0 to D9 are applicable to RDAC wiper register whereas D0 to D15 are applicable to EEMEM register. Command codes are defined in Table II.

Table II. Command Operation Truth Table[1, 2, 3]

Command Number	Command Byte 0 B23 • • • • • • • • • • • • • • • B16	Data Byte 1 B15 • • • • • B8	Data Byte 0 B7 • • • • • B0	Operation
	C3 C2 C1 C0 A3 A2 A1 A0	X • • • • D9 D8	D7 • • • • • D0	
0	0 0 0 0 X X X X	X • • • • X X	X • • • • • • X	NOP: Do nothing. See Table XII.
1	0 0 0 1 0 0 0 A0	X • • • • X X	X • • • • • • X	Write contents of EEMEM(A0) to RDAC(A0) Register. This command leaves device in the read program power state. To return part to the idle state, perform NOP command 0. See Table XII.
2	0 0 1 0 0 0 0 A0	X • • • • X X	X • • • • • • X	Save Wiper Setting: Write contents of RDAC(A0) to EEMEM(A0). See Table XI.
3[4]	0 0 1 1 A3 A2 A1 A0	D15 • • • • D8	D7 • • • • • D0	Write contents of Serial Register Data Bytes 0 and 1 (total 16-bit) to EEMEM(ADDR). See Table XIV.
4[5]	0 1 0 0 0 0 0 A0	X • • • • X X	X • • • • • • X	Decrement 6 dB: Right shift contents of RDAC(A0), register, stops at all "zeros."
5[5]	0 1 0 1 X X X X	X • • • • X X	X • • • • • • X	Decrement all 6 dB: Right shift contents of all RDAC registers, stops at all "zeros."
6[5]	0 1 1 0 0 0 0 A0	X • • • • X X	X • • • • • • X	Decrement contents of RDAC(A0) by "one," stops at all "zero."
7[5]	0 1 1 1 X X X X	X • • • • X X	X • • • • • • X	Decrement contents of all RDAC registers by "one," stops at all "zero."
8	1 0 0 0 0 0 0 0	X • • • • X X	X • • • • • • X	RESET: Load all RDACs with their corresponding EEMEM previously saved values.
9	1 0 0 1 A3 A2 A1 A0	X • • • • X X	X • • • • • • X	Transfer contents of EEMEM(ADDR) to Serial Register Data Bytes 0 and 1 and previously stored data can be read out from the SDO pin. See Table XV.
10	1 0 1 0 0 0 0 A0	X • • • • X X	X • • • • • • X	Transfer contents of RDAC(A0) to Serial Register Data Bytes 0 and 1 and wiper setting can be read out from SDO pin. See Table XVI.
11	1 0 1 1 0 0 0 A0	X • • • • D9 D8	D7 • • • • • D0	Write contents of Serial Register Data Bytes 0 and 1 (total 10-bit) to RDAC(A0). See Table X.
12[5]	1 1 0 0 0 0 0 A0	X • • • • X X	X • • • • • • X	Increment 6 dB: Left shift contents of RDAC(A0), stops at all "ones." See Table XIII.
13[5]	1 1 0 1 X X X X	X • • • • X X	X • • • • • • X	Increment All 6 dB: Left shift contents of all RDAC registers, stops at all "ones."
14[5]	1 1 1 0 0 0 0 A0	X • • • • X X	X • • • • • • X	Increment contents of RDAC(A0) by "one," stops at all "ones." See Table XI.
15[5]	1 1 1 1 X X X X	X • • • • X X	X • • • • • • X	Increment contents of all RDAC registers by "one," stops at all "ones."

NOTES
[1]The SDO output shifts out the last 24 bits of data clocked into the serial register for daisy-chain operation. Exception: for any command following command 9 or 10, the selected internal register data will be present in data bytes 0 and 1. The commands following 9 and 10 must also be a full 24-bit data-word to completely clock out the contents of the serial register.
[2]The RDAC register is a volatile scratch pad register that is refreshed at power ON from the corresponding nonvolatile EEMEM register.
[3]Execution of the above operations takes place when the $\overline{CS}$ strobe returns to logic high.
[4]Write two data bytes (total 16-bit) to EEMEM. But in the cases of addresses 0 and 1, only the last 10 bits are valid for wiper position setting.
[5]The increment, decrement, and shift commands ignore the contents of the shift register data bytes 0 and 1.

REV. A

Table III. Set and Save RDAC with Independent Data to EEMEM Registers

SDI	SDO	Action
B00100$_H$	XXXXXX$_H$	Loads data 100$_H$ into RDAC1 register, Wiper W1 moves to 1/4 full-scale position.
20xxxx$_H$	B00100$_H$	Saves copy of RDAC1 register content into corresponding EEMEM1 register.
B10200$_H$	20xxxx$_H$	Loads 200$_H$ data into RDAC2 register, Wiper W2 moves to 1/2 full-scale position.
21xxxx$_H$	B10200$_H$	Saves copy of RDAC2 register contents into corresponding EEMEM2 register.

At system power-on, the scratch pad register is automatically refreshed with the value previously saved in the corresponding EEMEM register. The factory preset EEMEM value is midscale. The scratch pad register can also be loaded with the contents of the EEMEM register in three different ways. First, executing command 1 retrieves the corresponding EEMEM value. Second, executing command 8 resets both channels' EEMEM values. Finally, pulsing the $\overline{PR}$ pin also refreshes both EEMEM settings. Operating the hardware control $\overline{PR}$ function, however, requires a complete pulse signal. When $\overline{PR}$ goes low, the internal logic sets the wiper at midscale. The EEMEM value will not be loaded until $\overline{PR}$ returns to high.

EEMEM Protection
The write-protect ($\overline{WP}$) disables any changes of the scratch pad register contents regardless of the software commands, except that the EEMEM setting can be refreshed and overwrite the $\overline{WP}$ by using commands 1, 8, and $\overline{PR}$ pulse. To disable $\overline{WP}$, it is recommended to execute a NOP command before returning $\overline{WP}$ to logic high.

Linear Increment and Decrement Commands
The increment and decrement commands (14, 15, 6, and 7) are useful for linear step adjustment applications. These commands simplify microcontroller software coding by allowing the controller to just send an increment or decrement command to the device. The adjustment can be individual or ganged control. For increment command, executing command 14 will automatically move the wiper to the next resistance segment position. The master increment command 15 will move all resistor wipers up by one position.

Logarithmic Taper Mode Adjustment (±6 dB/Step)
There are four programming commands that provide the logarithmic taper increment and decrement wiper position control by either individually or ganged control. 6 dB increment is activated by commands 12 and 13, and 6 dB decrement is activated by commands 4 and 5. For example, starting at zero scale, executing 12 times of the increment command 12 will move the wiper in 6 dB per step from 0% of the full-scale R_{AB} to the full-scale R_{AB}. The 6 dB increment command doubles the value of the RDAC register contents each time the command is executed. When the wiper position is near the maximum setting, the last 6 dB increment command will cause the wiper to go to the full-scale 1023-code position. Furthermore, 6 dB per increment command will no longer change the wiper position beyond its full scale (see Table IV).

6 dB step increment and decrement are achieved by shifting the bit internally to the left and right, respectively. The following information explains the nonideal ±6 dB step adjustment at certain conditions. Table IV illustrates the operation of the shifting function on the individual RDAC register data bits. Each line going down the table represents a successive shift operation. Note that the left shift 12 and 13 commands were modified such that if the data in the RDAC register is equal to zero, and the data is left shifted, the RDAC register is then set to code 1. Similarly, if the data in the RDAC register is greater than or equal to midscale, and the data is left shifted, then the data in the RDAC register is automatically set to full scale. This makes the left shift function as ideal a logarithmic adjustment as is possible.

The right shift 4 and 5 commands will be ideal only if the LSB is zero (i.e., ideal logarithmic—no error). If the LSB is a 1, the right shift function generates a linear half LSB error that translates to a number of bits dependent logarithmic error as shown in Figure 3. The plot shows the error of the odd numbers of bits for AD5235.

Table IV. Detail Left and Right Shift Functions for 6 dB Step Increment and Decrement

	Left Shift	Right Shift	
	00 0000 0000	11 1111 1111	
	00 0000 0001	01 1111 1111	
	00 0000 0010	00 1111 1111	
Left Shift +6 dB/step	00 0000 0100	00 0111 1111	Right Shift +6 dB/step
	00 0000 1000	00 0011 1111	
	00 0001 0000	00 0001 1111	
	00 0010 0000	00 0000 1111	
	00 0100 0000	00 0000 0111	
	00 1000 0000	00 0000 0011	
	01 0000 0000	00 0000 0001	
	10 0000 0000	00 0000 0000	
	11 1111 1111	00 0000 0000	
	11 1111 1111	00 0000 0000	

Actual conformance to a logarithmic curve between the data contents in the RDAC register and the wiper position for each right shift 4 and 5 command execution contains an error only for odd numbers of bits. Even numbers of bits are ideal. The graph in Figure 3 shows plots of Log_Error [i.e., $20 \times \log_{10}$ (error/code)] for the AD5235. For example, code 3 Log_Error = $20 \times \log_{10}$ (0.5/3) = –15.56 dB, which is the worst case. The plot of Log_Error is more significant at the lower codes.
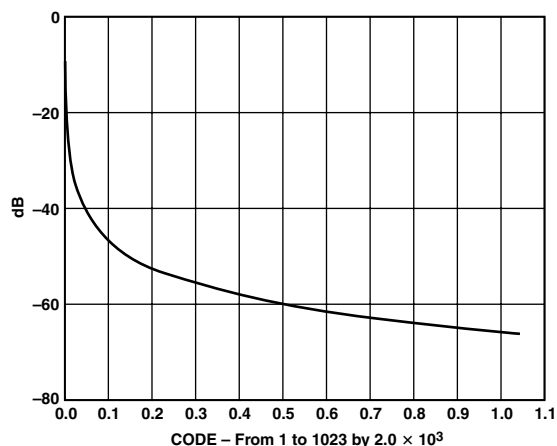
Figure 3. Plot of Log_Error Conformance for Odd Numbers of Bits Only (Even Numbers of Bits Are Ideal)

AD5235

Push Button Configurable for Previous Command Execution
Another subtle feature of AD5235 is that subsequent $\overline{CS}$ strobes repeat previous commands. This feature can be used to configure push button control that is particularly useful for increment/decrement or ±6 dB step adjustments.

Using Additional Internal Nonvolatile EEMEM
The AD5235 contains additional internal user storage registers (EEMEM) for saving constants and other 16-bit data. Table V provides an address map of the internal storage registers shown in the functional block diagram as EEMEM1, EEMEM2, and 26 bytes (13 addresses × 2 bytes each) of USER EEMEM.

Table V. EEMEM Address Map

EEMEM Number	Address	EEMEM Content For
1	0000	RDAC1[1, 2]
2	0001	RDAC2
3	0010	USER1[3]
4	0011	USER2
:	:	:
15	1110	USER13
16	1111	R_{AB1_ACTUAL}[4]

NOTES
[1]RDAC data stored in EEMEM locations are transferred to their corresponding RDAC Register at power-on, or when commands 1, 8, and $\overline{PR}$ are executed.
[2]Execution of command 1 leaves the device in the Read Mode power consumption state. After the last command 1 is executed, the user should perform a NOP, command 0 to return the device to the low power idling state.
[3]USER <data> are internal nonvolatile EEMEM registers available to store and retrieve constants and other 16-bit information using commands 3 and 9, respectively.
[4]Read only.

Calculating Actual End-to-End Terminal Resistance
The resistance tolerance is stored in the EEMEM register during factory testing. The actual end-to-end resistance can therefore be calculated, which is valuable for calibration, tolerance matching, and precision applications. Notice this value is read only and the R_{AB2} matches with R_{AB1} of typically 0.1%.

The resistance tolerance in percentage is contained in the last 16 bits of data in the EEMEM Register 15. The format is the sign magnitude binary format with the MSB designate for sign (0 = positive and 1 = negative), the next 7 MSB designates for the

integer number, and the 8 LSB designates for the decimal number (See Table VI).

Daisy-Chain Operation
The serial data output pin (SDO) can be used to read out the contents of the wiper setting and EEMEM value under commands 10 and 9, respectively. If these commands are not used, SDO can be used for daisy-chaining multiple devices for simultaneous operations (see Figure 4). The SDO pin contains an open-drain N-Ch FET and requires a pull-up resistor if SDO function is used. Users need to tie the SDO pin of one package to the SDI pin of the next package. Users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO-SDI interface may induce time delay to the subsequent devices (see Figure 4).

If two AD5235s are daisy-chained, this requires a total of 48 bits of data. The first 24 bits (formatted 4-bit command, 4-bit address, and 16-bit data) go to U2, and the second 24 bits with the same format go to U1. The $\overline{CS}$ should be kept low until all 48 bits are clocked into their respective serial registers. The $\overline{CS}$ is then pulled high to complete the operation.
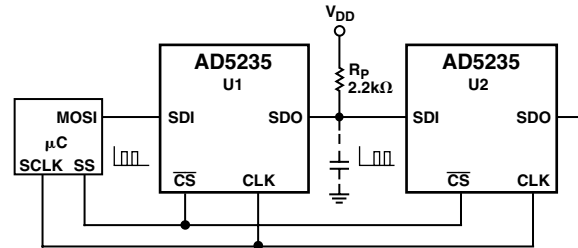

Figure 4. Daisy-Chain Configuration

DIGITAL INPUT/OUTPUT CONFIGURATION
All digital inputs are ESD protected. Digital inputs are high impedance and can be driven directly from most digital sources. Active at logic low, $\overline{PR}$ and $\overline{WP}$ should be biased to V_{DD} if they are not used. There are no internal pull-up resistors on any digital input pin. To avoid floating digital pins that may cause false triggering in the noisy environment, pull-up resistors should be added. This is applicable in cases where the device will be detached from the driving source once it is programmed.

Table VI. Calculating End-to-End Terminal Resistance

Bit	D15	D14	D13	D12	D11	D10	D9	D8	●	D7	D6	D5	D4	D3	D2	D1	D0
Sign Mag	Sign	2^6	2^5	2^4	2^3	2^2	2^1	2^0		2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	Sign			7 Bits for Integer Number					Decimal Point				8 Bits for Decimal Number				

For example, if R_{AB_RATED} = 250 kΩ and the data in the SDO shows XXXX XXXX 0001 1100 0000 1111, R_{AB_ACTUAL} can be calculated as follows:

MSB: 0 = Positive
Next 7 MSB: 001 1100 = 28
8 LSB: 0000 1111 = 15 × 2^{-8} = 0.06
% Tolerance = 28.06%
Hence, R_{AB_ACTUAL} = 320.15 kΩ

The SDO and RDY pins are open-drain digital outputs. Similarly, pull-up resistors are needed if these functions are used. To optimize the speed and power trade-off, use 2.2 kΩ pull-up resistors.

The equivalent serial data input and output logic is shown in Figure 5. The open-drain output SDO is disabled whenever chip select $\overline{CS}$ is logic high. ESD protection of the digital inputs is shown in Figures 6a and 6b.
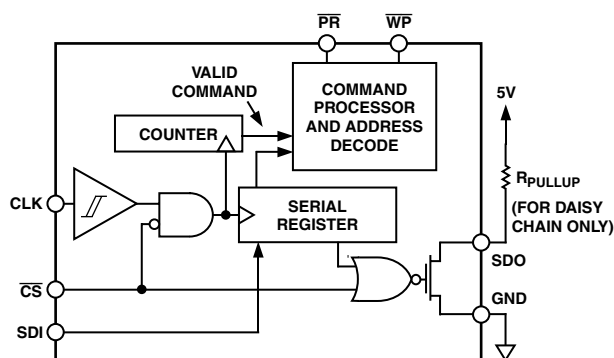

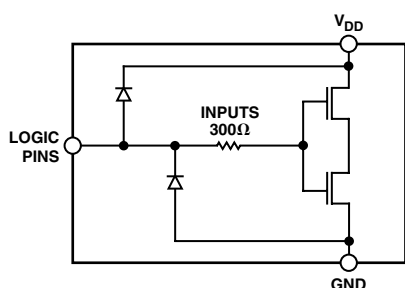Figure 5. Equivalent Digital Input-Output Logic
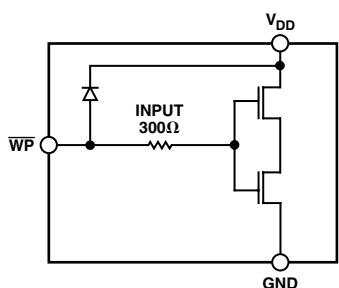

Figure 6a. Equivalent ESD Digital Input Protection

Figure 6b. Equivalent $\overline{WP}$ Input Protection

SERIAL DATA INTERFACE
The AD5235 contains a 4-wire SPI-compatible digital interface (SDI, SDO, $\overline{CS}$, and CLK). The 24-bit serial word must be loaded with MSB first, and the format of the word is shown in Table I. The command bits (C0 to C3) control the operation of the digital potentiometer according to the command shown in Table II. A0 to A3 are assigned for address bits. A0 is used to address RDAC1 or RDAC2. Addresses 2 to 14 are accessible by users. Address 15 is reserved for factory usage. Table V provides an address map of the EEMEM locations. The data bits (D0 to D9) are the values that are loaded into the RDAC registers at command 11. The data bits (D0 to D15) are the values that are loaded into the EEMEM registers at command 3.

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The last command prior to a period of no programming activity should be applied with the no operation (NOP), command 0. It is recommended to do so to ensure minimum power consumption in the internal logic circuitry.

The SPI interface can be used in two slave modes CPHA = 1, CPOL = 1 and CPHA = 0, CPOL = 0. CPHA and CPOL refer to the control bits that dictate the SPI timing in these MicroConverter® and microprocessor parts: ADUC812/824, M68HC11, and MC68HC16R1/916R1.

TERMINAL VOLTAGE OPERATING RANGE
The AD5235 positive V_{DD} and negative V_{SS} power supply defines the boundary conditions for proper three-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} or V_{SS} will be clamped by the internal forward biased diodes (see Figure 7).
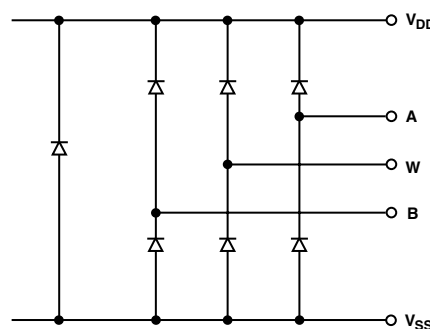

Figure 7. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the AD5235 device is primarily used as a digital ground reference. To minimize the digital ground bounce, the AD5235 ground terminal should be joined remotely to the common ground (see Figure 8). The digital input control signals to the AD5235 must be referenced to the device ground pin (GND) and must satisfy the logic level defined in the specification table of this data sheet. An internal level shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD}, regardless of the digital input level. In addition, V_{AB}, V_{WA}, and V_{WB} have no polarity constraint. Their magnitudes are bounded by their applied voltages and $V_{DD} - V_{SS}$, whichever is the smallest.

Power-Up Sequence
Since there are diodes to limit the voltage compliance at terminals A, B, and W (see Figure 7), it is important to power V_{DD}/V_{SS} first before applying any voltage to terminals A, B, and W. Otherwise, the diode will be forward biased such that V_{DD}/V_{SS} will be powered unintentionally. For example, applying 5 V across terminals A and B prior to V_{DD} will cause the V_{DD} terminal to exhibit 4.3 V. It is not destructive to the device, but it may affect the rest of the user's system. As a result, the ideal power-up sequence is in the following order: GND, V_{DD}/V_{SS}, digital Inputs, and V_A, V_B, and V_W. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}/V_{SS}.

Regardless of the power-up sequence and the ramp rates of the power supplies, once V_{DD}/V_{SS} are powered, the power-on reset activates, which retrieves EEMEM saved values to the RDAC registers (see TPC 15).

AD5235

Layout and Power Supply Bypassing

It is a good practice to employ compact, minimum-lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 μF to 0.1 μF disc or chip ceramic capacitors. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance (Figure 8).
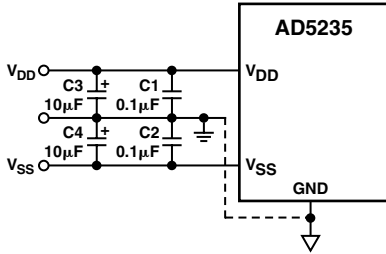

Figure 8. Power Supply Bypassing

RDAC STRUCTURE

The patent pending RDAC contains multiple strings of equal resistor segments with an array of analog switches that acts as the wiper connection. The number of positions is the resolution of the device. The AD5235 has 1024 connection points, allowing it to provide better than 0.1% setability resolution. Figure 9 shows an equivalent structure of the connections between the three terminals of the RDAC. The SW_A and SW_B will always be on, while one of the switches $SW(0)$ to $SW(2^N - 1)$ will be on one at a time depending on the resistance position decoded from the data bits. Since the switch is not ideal, there is a 50 Ω wiper resistance, R_W. Wiper resistance is a function of supply voltage and temperature. The lower the supply voltage or the higher the temperature, the higher the resulting wiper resistance. Users should be aware of the wiper resistance dynamics if accurate prediction of the output resistance is needed.
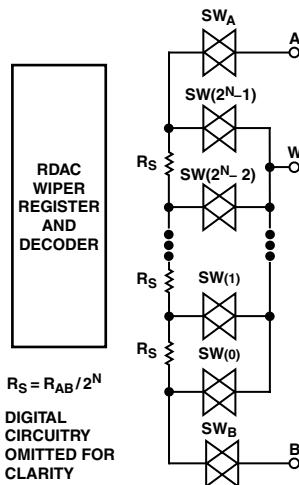

Figure 9. Equivalent RDAC Structure

Table VII. Nominal Individual Segment Resistor Values

Device Resolution	25 kΩ	250 kΩ
1024-Step	24.4	244

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B, R_{AB}, is available with 25 kΩ and 250 kΩ with 1024 positions (10-bit resolution). The final digits of the part number determine the nominal resistance value, e.g., 25 kΩ = 25; 250 kΩ = 250.

The 10-bit data-word in the RDAC latch is decoded to select one of the 1024 possible settings. The following discussion describes the calculation of resistance R_{WB} at different codes of a 25 kΩ part. The wiper's first connection starts at the B terminal for data 000_H. $R_{WB}(0)$ is 50 Ω because of the wiper resistance, and it is independent of the nominal resistance. The second connection is the first tap point where $R_{WB}(1)$ becomes 24.4 Ω + 50 Ω = 74.4 Ω for data 001_H. The third connection is the next tap point representing $R_{WB}(2) = 48.8 + 50 = 98.8$ Ω for data 002_H and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at $R_{WB}(1023) = 25026$ Ω. See Figure 9 for a simplified diagram of the equivalent RDAC circuit. When R_{WB} is used, the A terminal can be left floating or tied to the wiper.
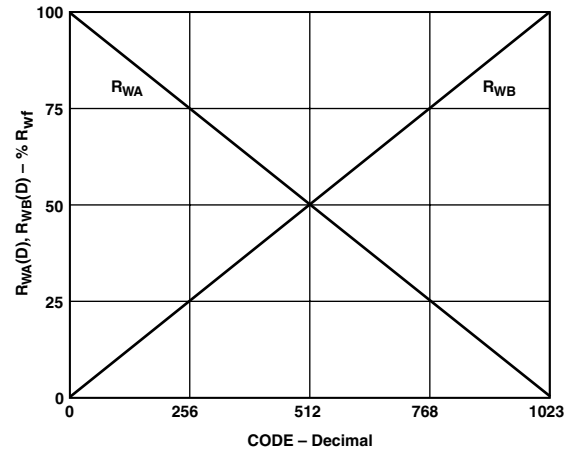

Figure 10. $R_{WA}(D)$ and $R_{WB}(D)$ vs. Decimal Code

The general equation that determines the programmed output resistance between Wx and Bx is:

$$R_{WA}(D) = \frac{D}{1024} \times R_{AB} + R_W \qquad (1)$$

Where D is the decimal equivalent of the data contained in the RDAC register, R_{AB} is the nominal resistance between terminals A and B, and R_W is the wiper resistance.

For example, the following output resistance values will be set for the following RDAC latch codes (applies to R_{AB} = 25 kΩ digital potentiometers).

Table VIII. $R_{WB}(D)$ at Selected Codes (R_{AB} = 25 kΩ)

D (DEC)	$R_{WB}(D)$ (Ω)	Output State
1023	25026	Full Scale
512	12550	Midscale
1	74.4	1 LSB
0	50	Zero Scale (Wiper Contact Resistance)

Note that in the zero-scale condition, a finite wiper resistance of 50 Ω is present. Care should be taken to limit the current flow between W and B in this state to no more than 20 mA to avoid degradation or possible destruction of the internal switches.

Like the mechanical potentiometer the RDAC replaces, the AD5235 parts are totally symmetrical. The resistance between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. Figure 10 shows the symmetrical programmability of the various terminal connections. When R_{WA} is used, the B terminal can be left floating or tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general transfer equation for this operation is:

$$R_{WA}(D) = \frac{1024 - D}{1024} \times R_{AB} + R_W \qquad (2)$$

For example, the following output resistance values will be set for the following RDAC latch codes (applies to $R_{AB} = 25$ kΩ digital potentiometers).

Table IX. $R_{WA}(D)$ at Selected Codes ($R_{AB} = 25$ kΩ)

D (DEC)	$R_{WA}(D)$ (Ω)	Output State
1023	74.4	Full Scale
512	12550	Midscale
1	25026	1 LSB
0	25050	Zero Scale (Wiper Contact Resistance)

The typical distribution of R_{AB} from channel-to-channel matches to ±0.2% within the same package. Device-to-device matching is process lot dependent upon the worst case of ±30% variation. On the other hand, the change in R_{AB} with temperature has a 35 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER
Voltage Output Operation
The digital potentiometer can be configured to generate an output voltage at the wiper terminal that is proportional to the input voltages applied to terminals A and B. For example, connecting terminal A to 5 V and terminal B to ground produces an output voltage at the wiper that can be any value from 0 V to 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 2^N position resolution of the potentiometer divider.

Since AD5235 can also be supplied by dual supplies, the general equation defining the output voltage at V_W with respect to ground for any given input voltages applied to terminals A and B is:

$$V_W(D) = \frac{D}{1024} \times V_{AB} + V_B \qquad (3)$$

Equation 3 assumes V_W is buffered so that the effect of wiper resistance is nulled. Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here, the output voltage is dependent on the ratio of the internal resistors, not the absolute value; therefore, the drift improves to 15 ppm/°C. There is no voltage polarity restriction between terminals A, B, and W as long as the terminal voltage (V_{TERM}) stays within $V_{SS} < V_{TERM} < V_{DD}$.

PROGRAMMING EXAMPLES
The following programming examples illustrate the typical sequence of events for various features of the AD5235. Users should refer to Table II for the commands and data-word format. The command numbers, addresses, and data appearing at the SDI and SDO pins are displayed in hexadecimal format in the following examples.

Table X. Scratch Pad Programming

SDI	SDO	Action
B00100$_H$	XXXXXX$_H$	Loads data 100$_H$ into RDAC1 register, Wiper W1 moves to 1/4 full-scale position.
B10200$_H$	B00100$_H$	Loads data 200$_H$ into RDAC2 register, Wiper 2 moves to 1/2 full-scale position.

Table XI. Incrementing RDAC Followed by Storing the Wiper Setting to EEMEM

SDI	SDO	Action
B00100$_H$	XXXXXX$_H$	Loads data 100$_H$ into RDAC1 register, Wiper W1 moves to 1/4 full-scale position.
E0XXXX$_H$	B00100$_H$	Increments RDAC1 register by one to 101$_H$.
E0XXXX$_H$	E0XXXX$_H$	Increments RDAC1 register by one to 102$_H$. Continue until desired wiper position reached.
20XXXX$_H$	XXXXXX$_H$	Saves RDAC1 data into EEMEM1. Optionally tie $\overline{WP}$ to GND to protect EEMEM values.

Table XII. Restoring EEMEM Values to RDAC Registers

EEMEM values for RDACs can be restored by: Power-on or Strobing $\overline{PR}$ pin or two different commands shown below

SDI	SDO	Action
10XXXX$_H$	XXXXXX$_H$	Restores EEMEM1 value to RDAC1 register.
00XXXX$_H$	10XXXX$_H$	NOP. Recommended step to minimize power consumption.
8XXXXX$_H$	00XXXX$_H$	Reset EEMEM1 and EEMEM2 values to RDAC1 and RDAC2 registers, respectively.

Table XIII. Using Left Shift by One to Increment 6 dB Steps

SDI	SDO	Action
C0XXXX$_H$	XXXXXX$_H$	Moves wiper 1 to double the present data contained in RDAC1 register.
C1XXXX$_H$	C0XXXX$_H$	Moves wiper 2 to double the present data contained in RDAC2 register.

AD5235

Table XIV. Storing Additional User Data in EEMEM

SDI	SDO	Action
$32AAAA_H$	$XXXXXX_H$	Stores data $AAAA_H$ into spare EEMEM location USER1. (Allowable to address in 13 locations with maximum 16 bits of data.)
335555_H	$32AAAA_H$	Stores data 5555_H into spare EEMEM location USER2. (Allowable to address 13 locations with maximum 16 bits of data.)

Table XV. Reading Back Data From Various Memory Locations

SDI	SDO	Action
$92XXXX_H$ $00XXXX_H$	$XXXXXX_H$ $92AAAA_H$	Prepares data read from USER1 location. NOP command 0 sends 24-bit word out of SDO where the last 16 bits contain the contents of USER1 location. NOP command ensures device returns to idle power dissipation state.

Table XVI. Reading Back Wiper Setting

SDI	SDO	Action
$B00200_H$	$XXXXXX_H$	Sets RDAC1 to midscale.
$C0XXXX_H$	$B00200_H$	Doubles RDAC1 from midscale to full scale.
$A0XXXX_H$	$C0XXXX_H$	Prepares reading wiper setting from RDAC1 register.
$XXXXXX_H$	$A003FF_H$	Readback full-scale value from RDAC1 register.

Analog Devices offers a user-friendly AD5235EVAL evaluation kit that can be controlled by a personal computer through the printer port. The driving program is self-contained, so no programming languages or skills are needed.

APPLICATIONS

Bipolar Operation From Dual Supplies

The AD5235 can be operated from dual supplies ± 2.5 V, which enables control of ground referenced ac signals or bipolar operation. AC signals, as high as V_{DD}/V_{SS}, can be applied directly across terminals A to B with the output taken from terminal W. See Figure 11 for a typical circuit connection.
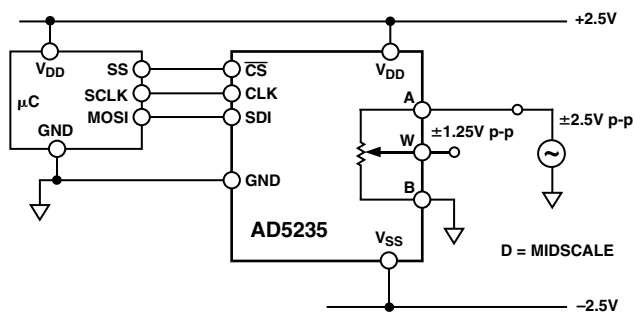

Figure 11. Bipolar Operation from Dual Supplies

Gain Control Compensation

A digital potentiometer is commonly used in gain control, such as in the noninverting gain amplifier shown in Figure 12.
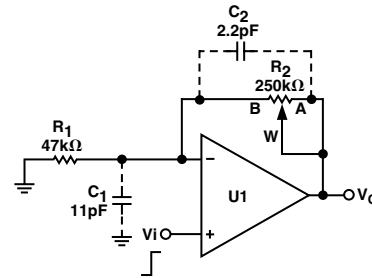

Figure 12. Typical Noninverting Gain Amplifier

Notice the RDAC B terminal parasitic capacitance is connected to the op amp noninverting node; it introduces a zero for the $1/\beta_O$ term with 20 dB/dec, whereas a typical op amp GBP has –20 dB/dec characteristics. A large R_2 and finite C_1 can cause this zero's frequency to fall well below the crossover frequency. Hence, the rate of closure becomes 40 dB/dec and the system has 0° phase margin at the crossover frequency. The output may ring or oscillate if an input is a rectangular pulse or step functions. Similarly, it is also likely to ring when switching between two gain values; this is equivalent to a step change at the input.

Depending on the op amp GBP, reducing the feedback resistor may extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor, C_2, to cancel the effect caused by C_1. Optimum compensation occurs when $R_1 \times C_1 = R_2 \times C_2$. This is not an option because of the variation of R_2. As a result, one may use the relationship above and scale C_2 as if R_2 is at its maximum value. Doing so may overcompensate and compromise the performance when R_2 is set at low values. On the other hand, it will avoid the ringing or oscillation at the worst case. For critical applications, C_2 should be found empirically to suit the need. In general, C_2 in the range of a few pF to no more than a few tenths of pF is usually adequate for the compensation.

Similarly, there are W and A terminal capacitances connected to the output (not shown). Fortunately their effect at this node is less significant and the compensation can be avoided in most cases.

High Voltage Operation

As shown in the previous example, the digital potentiometer can be placed directly in the feedback or input path of an op amp for gain control, provided that the voltage across terminals A–B, W–A, or W–B does not exceed $|5 V|$. When high voltage gain is needed, users should set a fixed gain in an op amp and let the digital potentiometer control the adjustable input. Figure 13 shows a simple implementation. Similarly, a compensation capacitor C may be needed to dampen the potential ringing whenever the digital potentiometer changes steps. This effect is prominent when stray capacitance at the inverting node is augmented by a large feedback resistor. In general, a picofarads capacitor C is adequate to combat the problem.
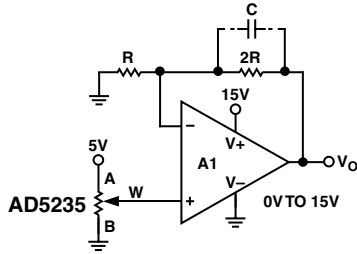
Figure 13. 15 V Voltage Span Control

Programmable Voltage Reference

For voltage divider mode operation, Figure 14, it is common to buffer the output of the digital potentiometer unless the load is much larger than R_{WB}. Not only does the buffer serve the purpose of impedance conversion, it also allows a heavier load to be driven.
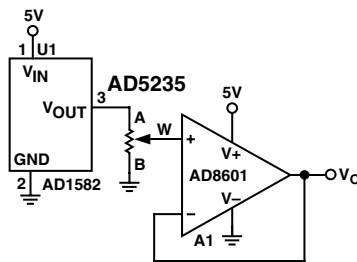

Figure 14. Programmable Voltage Reference

Bipolar Programmable Gain Amplifier

For applications requiring bipolar gain, Figure 15 shows one implementation. Digital potentiometer U1 sets the adjustment range. The wiper voltage VW2 can therefore be programmed between V_i and $-KV_i$ at a given U2 setting. Configure A2 as a noninverting amplifier that yields a transfer function

$$\frac{V_O}{V_i} = \left(1 + \frac{R_2}{R_1}\right) \times \left(\frac{D_2}{1024} \times (1+K) - K\right) \quad (4)$$

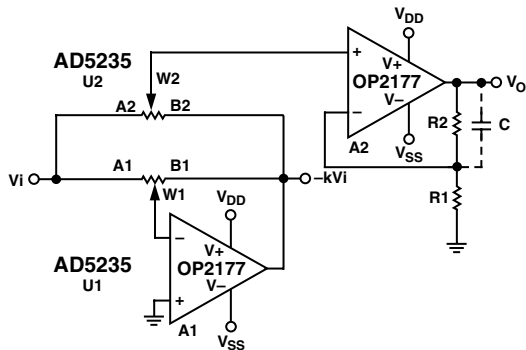where K is the ratio of R_{WB1}/R_{WA1} set by U1.

Figure 15. Bipolar Programmable Gain Amplifier

In the simpler (and much more usual) case, where $K = 1$, V_O simplifies to:

$$V_O = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{2D_2}{1024} - 1\right) \times V_i \quad (5)$$

Table XVII shows the result of adjusting D_2, with A2 configured as a unity gain, a gain of 2, and a gain of 10. The result is a bipolar amplifier with linearly programmable gain and 1024-step resolution.

Table XVII. Result of Bipolar Gain Amplifier

D	$R_1 = \infty$, $R_2 = 0$	$R_1 = R_2$	$R_2 = 9R_1$
0	−1	−2	−10
256	−0.5	−1	−5
512	0	0	0
768	0.5	1	5
1023	0.992	1.984	9.92

10-Bit Bipolar DAC

If we change the circuit in Figure 15 with the input taken from a precision reference, set U1 to midscale, and configure A2 as a buffer, a 10-bit bipolar DAC can be realized (Figure 16). Compared to the conventional DAC, this circuit offers comparable resolution but not the precision because of the wiper resistance effects. Degradation of the nonlinearity and temperature coefficient is prominent near the low values of the adjustment range. On the other hand, this circuit offers a unique nonvolatile memory feature that in some cases outweighs the shortfall of nonprecision. Without considering the wiper resistance, the output of this circuit is approximately:

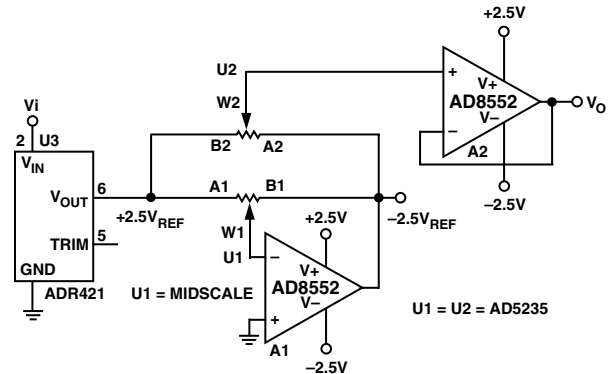$$V_O = \left(\frac{2D_2}{1024} - 1\right) \times V_{REF} \quad (6)$$

Figure 16. 10-Bit Bipolar DAC

Programmable Voltage Source with Boosted Output

For applications requiring high current adjustment, such as a laser diode driver or turnable laser, a boosted voltage source can be considered (Figure 17).
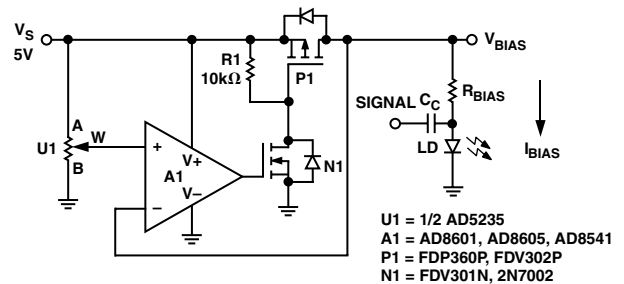

Figure 17. Programmable Boosted Voltage Source

In this circuit, the inverting input of the op amp forces the V_{BIAS} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the P-Ch FET P1. The N-Ch FET N_1 simplifies the op amp driving requirement. A1 needs to be rail-to-rail input type. Resistor R_1 is needed

AD5235

to prevent P1 from not turning off once it is on. The choice of R_1 is a balance between the power loss of this resistor and the output turn off time. N1 can be any general-purpose signal FET; on the other hand, P1 is driven in the saturation state and therefore its power handling must be adequate to dissipate $(V_S - V_{BIAS}) \times I_{BIAS}$ power. This circuit can source maximum of 100 mA at 5 V supply. Higher current can be achieved with P1 in larger package. Note a single N-Ch FET can replace P1, N1, and R_1 altogether. However, the output swing will be limited unless separate power supplies are used. For precision applications, a voltage reference, such as ADR423, ADR292, and AD1584, can be applied at the input of the digital potentiometer.

Programmable 4 to 20 mA Current Source

A programmable 4 to 20 mA current source can be implemented with the circuit shown in Figure 18. REF191 is a unique low supply headroom and high current handling precision reference that can deliver 20 mA at 2.048 V. The load current is simply the voltage across terminals B to W of the digital potentiometer divided by R_S:

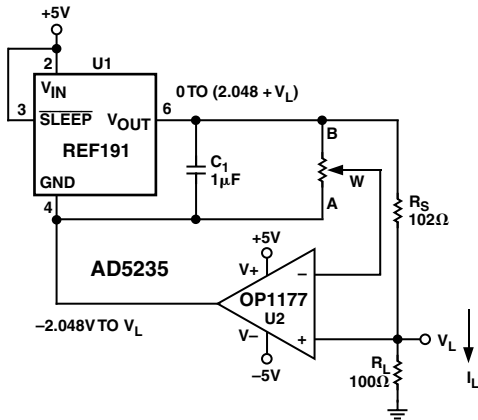$$I_L = \frac{V_{REF} \times D}{R_S} \qquad (7)$$

Figure 18. Programmable 4 mA to 20 mA Current Source

The circuit is simple but beware of two things. First, dual-supply op amps are ideal because the ground potential of REF191 can swing from –2.048 V at zero scale to V_L at full scale of the potentiometer setting. Although the circuit works under single supply, the programmable resolution of the system will be reduced. Second, the voltage compliance at V_L is limited to 2.5 V or equivalently a 125 Ω load. Should higher voltage compliance be needed, users may consider digital potentiometers AD5260, AD5280, and AD7376. Figure 19 shows an alternate circuit for high voltage compliance.

Programmable Bidirectional Current Source

For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be a solution (see Figure 19). If the resistors are matched, the load current is:

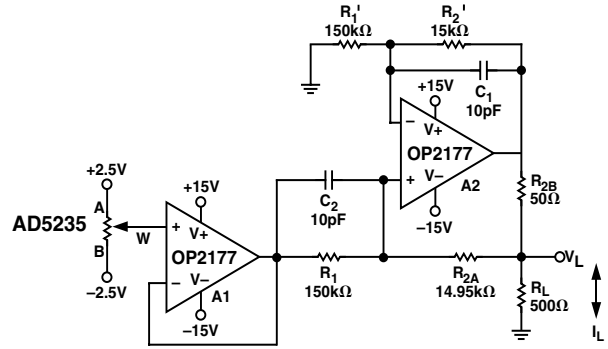$$I_L = \frac{\dfrac{R_{2A} + R_{2B}}{R_1}}{R_{2B}} \times V_W \qquad (8)$$

Figure 19. Programmable Bidirectional Current Source

R2B in theory can be made as small as needed to achieve the current needed within A2 output current driving capability. In this circuit, OP2177 can deliver ±5 mA in either direction and the voltage compliance approaches +15 V. Without the additions of C_1 and C_2, the output impedance (looking into V_L) can be shown as:

$$Z_O = \frac{R_1' R_{2B} (R_1 + R_{2A})}{R_1 R_2' - R_1' (R_{2A} + R_{2B})} \qquad (9)$$

This output impedance can be infinite if resistors R_1' and R_2' match precisely with R_1 and $R_{2A} + R_{2B}$, respectively, which is desirable. On the other hand, it can be negative if the resistors are not matched and cause oscillation. As a result, C_1 and C_2, in the range of a few pF, are needed to prevent the oscillation.

Programmable Low-Pass Filter

In A to D conversion applications, it is common to include an antialiasing filter to band limit the sampling signal. The dual channel AD5235 can therefore be used to construct a second order Sallen key low-pass filter (Figure 20). The design equations are:

$$\frac{V_O}{V_i} = \frac{w_f^2}{S^2 + \dfrac{w_f}{Q} S + w_f^2} \qquad (10)$$

$$\omega_O = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \qquad (11)$$

$$Q = \frac{1}{R_1 C_1} + \frac{1}{R_2 C_2} \qquad (12)$$

Users can first select some convenient values for the capacitors. To achieve maximally flat bandwidth where Q = 0.707, let C_1 be twice the size of C_2 and let $R_1 = R_2$. As a result, the user can adjust R_1 and R_2 concurrently to the same setting to achieve the desirable bandwidth.
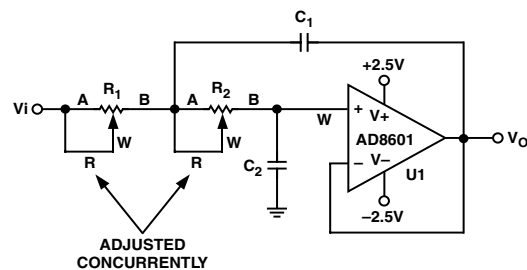
Figure 20. Sallen Key Low Pass Filter

Programmable Oscillator

In a classic Wien-bridge oscillator, Figure 21, the Wien network (R, R′, C, C′) provides positive feedback, while R_1 and R_2 provide negative feedback. At the resonant frequency, f_O, the overall phase shift is zero, and the positive feedback causes the circuit to oscillate. With R = R′, C = C′, and $R_2 = R_{2A}/(R_{2B} + R_{diode})$, the oscillation frequency is:

$$\omega_O = \frac{1}{RC} \quad \text{or} \quad f_O = \frac{1}{2\pi RC} \tag{13}$$

where R is equal to R_{WA} such that:

$$R = \frac{1024 - D}{1024} R_{AB} \tag{14}$$

At resonance, setting:

$$\frac{R_2}{R_1} = 2 \tag{15}$$

balances the bridge. In practice, R_2/R_1 should be set slightly larger than 2 to ensure the oscillation can start. On the other hand, the alternate turn-on of the diodes D_1 and D_2 ensures that R_2/R_1 are smaller than 2, momentarily stabilizing the oscillation.

Once the frequency is set, the oscillation amplitude can be tuned by R_{2B} since:

$$\frac{2}{3} V_O = I_D R_{2B} + V_D \tag{16}$$

V_O, I_D, and V_D are interdependent variables. With proper selection of R_{2B}, an equilibrium will be reached such that V_{wf} converges. R_{2B} can be in series with a discrete resistor to increase the amplitude, but the total resistance cannot be too large to saturate the output.
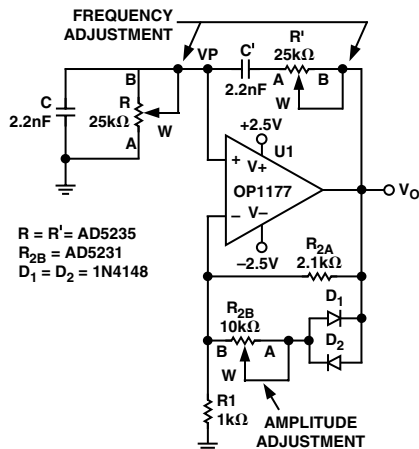

Figure 21. Programmable Oscillator with Amplitude Control

In both circuits in Figures 20 and 21, the frequency tuning requires both RDACs to be adjusted concurrently to the same settings. Since the two channels will be adjusted one at a time, an intermediate state will occur that may not be acceptable for certain applications. Of course, the increment/decrement commands 5, 7, 13, and 15 can all be used. Different devices can also be used in daisy-chain mode so that parts can be programmed to the same settings simultaneously.

Optical Transmitter Calibration with ADN2841

Together with the multirate 2.7 Gbps laser diode driver ADN2841, the AD5235 forms an optical supervisory system where the dual digital potentiometers can be used to set the laser average optical power and extinction ratio (Figure 22). AD5235 is particularly ideal for the optical parameter settings because of its high resolution and superior temperature coefficient characteristics.

The ADN2841 is a 2.7 Gbps laser diode driver that uses a unique control algorithm to manage both the laser average power and extinction ratio after the laser initial factory calibration. It stabilizes the laser data transmission by continuously monitoring its optical power and correcting the variations caused by temperature and the laser degradation over time. In ADN2841, the I_{MPD} monitors the laser diode current. Through its dual loop power and extinction ratio control, calibrated by AD5235 dual RDACs, the internal driver controls the bias current I_{BIAS} and consequently the average power. It also regulates the modulation current, I_{MODP}, by changing the modulation current linearly with slope efficiency. Any changes in the laser threshold current or slope efficiency are therefore compensated. As a result, this optical supervisory system minimizes the laser characterization efforts and therefore enables designers to apply comparable lasers from multiple sources.
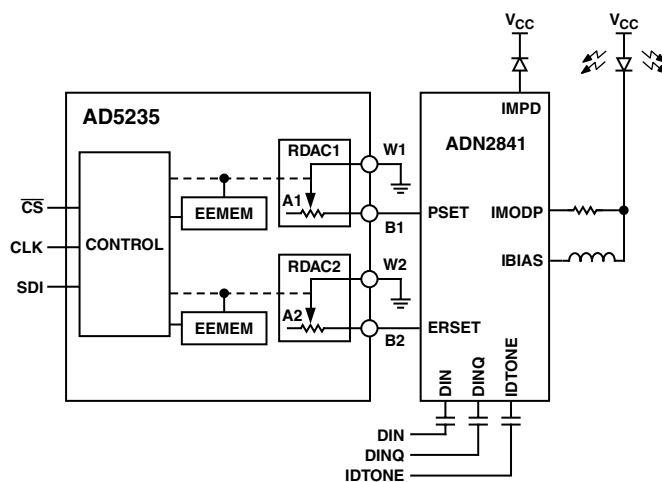

Figure 22. Optical Supervisory System

Resistance Scaling

AD5235 offers either 25 kΩ or 250 kΩ nominal resistance. For users who need lower resistance but must still maintain the number of step adjustments, they can parallel multiple devices. Figure 23 shows a simple scheme of paralleling both channels of RDACs. In order to adjust half of the resistance linearly per step, users need to program both RDACs coherently with the same settings.
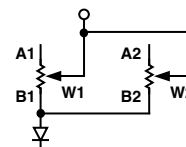

Figure 23. Reduce Resistance by Half with Linear Adjustment Characteristics

AD5235

Applicable only to the voltage divider mode operation, a much lower resistance can be achieved by paralleling a discrete resistor as shown in Figure 24. The equivalent resistance becomes:

$$R_{WB_{eq}} = \frac{D}{1024}\left(R_1 // R_2\right) + R_W \qquad (17)$$

$$R_{WA_{eq}} = \left(1 - \frac{D}{1024}\right)\left(R_1 // R_2\right) + R_W \qquad (18)$$
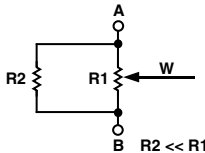
Figure 24. Lowering the Nominal Resistance

Figures 23 and 24 show that the digital potentiometers change steps linearly. On the other hand, pseudo log taper adjustment is usually preferred in applications like audio control. Figure 25 shows another way of resistance scaling. In this approach, the smaller the R2 with respect to R_{AB}, the more the pseudo log taper characteristic behaves. The equation is approximated as:

$$R_{eq} = \frac{D \times R_{AB} + 51200}{D \times R_{AB} + 51200 + 1024 \times R} \qquad (19)$$
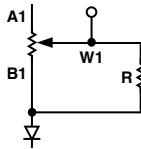
Figure 25. Resistor Scaling with Pseudo Log Adjustment Characteristics

Users should also be aware of the need for tolerance matching as well as for temperature coefficient matching of the components.

RESISTANCE TOLERANCE, DRIFT, AND TEMPERATURE COEFFICIENT MISMATCH CONSIDERATIONS

In the rheostat mode operation, such as gain control (Figure 26), the tolerance mismatch between the digital potentiometer and the discrete resistor can cause repeatability issues among various systems. Because of the inherent matching of the silicon process, it is practical to apply the dual channel device in this type of application. As such, R_1 can be replaced by one of the channels of the digital potentiometer and programmed to a specific value. R_2 can be used for the adjustable gain. Although it adds cost, this approach minimizes the tolerance and temperature coefficient mismatch between R_1 and R_2. In addition, this approach also tracks the resistance drift over time. As a result, these less than ideal parameters become less sensitive to the system variations.
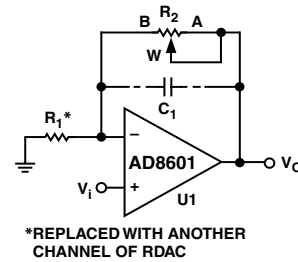
Figure 26. Linear Gain Control with Tracking Resistance Tolerance, Drift, and Temperature Coefficient.

Notice the circuit in Figure 27 can track the tolerance, temperature coefficient, and drift in this particular application. The characteristic of the transfer function is, however, a pseudo-logarithmic, rather than linear, gain function.
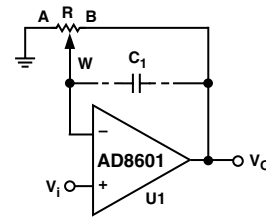
Figure 27. Nonlinear Gain Control with Tracking Resistance Tolerance and Drift

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RDACs. Configured as a potentiometer divider, the –3 dB bandwidth of the AD5235 (25 kΩ resistor) measures 125 kHz at half scale. TPC 11 provides the large signal BODE plot characteristics of the two available resistor versions, 25 kΩ and 250 kΩ. A parasitic simulation model is shown in Figure 28.
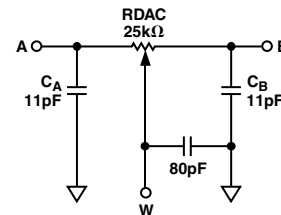
Figure 28. RDAC Circuit Simulation Model (RDAC = 25 kΩ)

Listing I provides a macro model net list for the 25 kΩ RDAC.

Listing I. Macro Model Net List for RDAC

```
.PARAM D = 1024, RDAC = 25E3
*
.SUBCKT DPOT (A, W, B)
*
CA      A       0       11E–12
RWA     A       W       {(1–D/1024) × RDAC + 50}
CW      W       0       80E–12
RWB     W       B       {D/1024 × RDAC + 50}
CB      B       0       11E–12
*
.ENDS DPOT
```

DIGITAL POTENTIOMETER FAMILY SELECTION GUIDE*

Part Number	Number of VRs per Package	Terminal Voltage Range (V)	Interface Data Control	Nominal Resistance (kΩ)	Resolution (No. of Wiper Positions)	Power Supply Current (I_{DD}) (µA)	Packages	Comments
AD5201	1	±3, 5.5	3-Wire	10, 50	33	40	MSOP-10	Full AC Specs, Dual Supply, Power-On-Reset, Low Cost
AD5220	1	5.5	UP/DOWN	10, 50, 100	128	40	PDIP, SO-8, MSOP-8	No Rollover, Power-On-Reset
AD7376	1	±15, 28	3-Wire	10, 50, 100, 1000	128	100	PDIP-14, SOL-16, TSSOP-14	Single 28 V or Dual ±15 V Supply Operation
AD5200	1	±3, 5.5	3-Wire	10, 50	256	40	MSOP-10	Full AC Specs, Dual Supply, Power-On-Reset
AD8400	1	5.5	3-Wire	1, 10, 50, 100	256	5	SO-8	Full AC Specs
AD5260	1	±5, 15	3-Wire	20, 50, 200	256	60	TSSOP-14	5 V to 15 V or ±5 V Operation, TC < 50 ppm/°C
AD5241	1	±3, 5.5	2-Wire	10, 100, 1000	256	50	SO-14, TSSOP-14	I²C Compatible, TC < 50 ppm/°C
AD5231	1	±2.75, 5.5	3-Wire	10, 50, 100	1024	10	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5222	2	±3, 5.5	UP/DOWN	10, 50, 100, 1000	128	80	SO-14, TSSOP-14	No Rollover, Stereo, Power-On-Reset, TC < 50 ppm/°C
AD8402	2	5.5	3-Wire	1, 10, 50, 100	256	5	PDIP, SO-14, TSSOP-14	Full AC Specs, nA Shutdown Current
AD5207	2	±3, 5.5	3-Wire	10, 50, 100	256	40	TSSOP-14	Full AC Specs, Dual Supply, Power-On-Reset, SDO
AD5232	2	±2.75, 5.5	3-Wire	10, 50, 100	256	10	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5235	2	±2.75, 5.5	3-Wire	25, 250	1024	6	TSSOP-16	Nonvolatile Memory, Direct Program, TC < 50 ppm/°C
AD5242	2	±3, 5.5	2-Wire	10, 100, 1000	256	50	SO-16, TSSOP-16	I²C-Compatible, TC < 50 ppm/°C
AD5262	2	±5, 15	3-Wire	20, 50, 200	256	60	TSSOP-16	5 V to 15 V or ±5 V Operation, TC < 50 ppm/°C
AD5203	4	5.5	3-Wire	10, 100	64	5	PDIP, SOL-24, TSSOP-24	Full AC Specs, nA Shutdown Current
AD5233	4	±2.75, 5.5	3-Wire	10, 50, 100	64	10	TSSOP-24	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5204	4	±3, 5.5	3-Wire	10, 50, 100	256	60	PDIP, SOL-24, TSSOP-24	Full AC Specs, Dual Supply, Power-On-Reset
AD8403	4	5.5	3-Wire	1, 10, 50, 100	256	5	PDIP, SOL-24, TSSOP-24	Full AC Specs, nA Shutdown Current
AD5206	6	±3, 5.5	3-Wire	10, 50, 100	256	60	PDIP, SOL-24, TSSOP-24	Full AC Specs, Dual Supply, Power-On-Reset

*For the most current information on digital potentiometers, check the website at: www.analog.com/DigitalPotentiometers

AD5235

OUTLINE DIMENSIONS

16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters
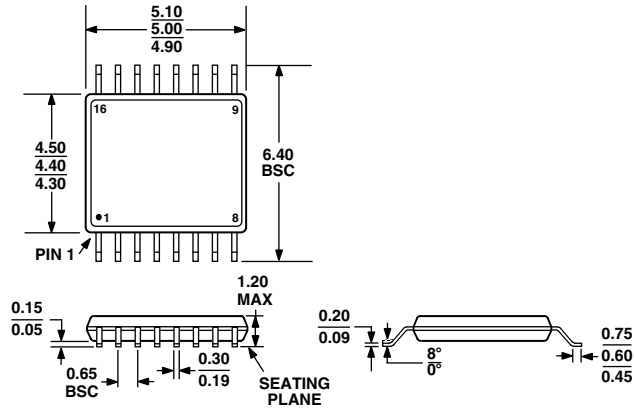
COMPLIANT TO JEDEC STANDARDS MO-153AB

Revision History

REV. A