

### FEATURES

- 2 V to +7 V Input Voltage Range
- Low  $V_{IN}$  Bias Current (<100 nA)
- Up to 5 V/ns Input Signal Tracking
- Low Dispersion of  $\pm 100$  ps
- 28-Lead PLCC Package

### APPLICATIONS

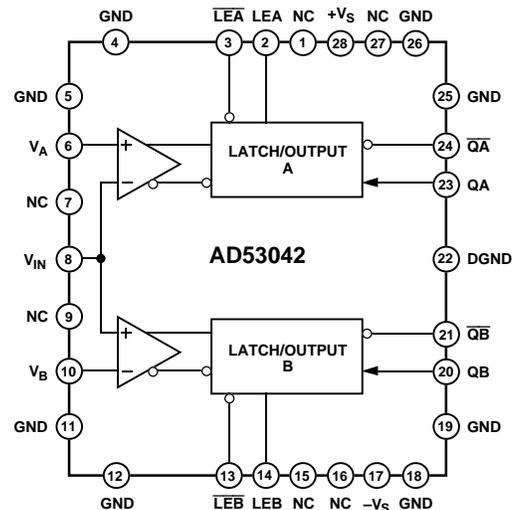
- Automatic Test Equipment
- Semiconductor Test Systems
- Board Test Systems

### PRODUCT DESCRIPTION

The AD53042 is an ultrahigh speed window comparator with latch. It uses a high speed monolithic process to provide high dc accuracy without sacrificing input voltage range. On-chip connection of the common input eliminates the contributions of a second bonding pad and package pin to the input capacitance, resulting in a maximum input capacitance of 2 pF.

The AD53042 employs a high precision differential input stage with a common mode range of 9 V. Its complementary digital outputs are fully ECL compatible. The output stage is capable of driving a 50  $\Omega$  line terminated to -2 V. The device also provides a latch function, allowing operation in track-hold mode and can also be used to generate hysteresis.

### FUNCTIONAL BLOCK DIAGRAM



NOTE:  
NOT THE ACTUAL PHYSICAL LAYOUT OF DEVICE.  
NC = NO CONNECTION INSIDE PACKAGE.

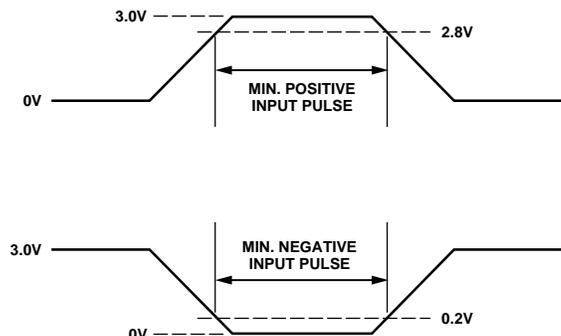


Figure 1. Typical Application Circuit

### REV. 0

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# AD53042–SPECIFICATIONS (All specifications apply with $T_C = 40^\circ\text{C}$ to $100^\circ\text{C}$ and $+V_S = +7.75\text{ V}$ to $+11.5\text{ V}$ ; $-V_S = -3.95\text{ V}$ to $-7.7\text{ V}$ unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions
<b>POWER SUPPLIES</b>					
I –Positive Supply Currents			65	mA	No Load
I –Negative Supply Current	-85			mA	No Load
P –Power Dissipation			1.19	W	No Load, $+V_S = +10\text{ V}$ , $-V_S = -5.2\text{ V}$
<b>DC INPUT CHARACTERISTICS</b>					
Offset Voltage ( $V_{OS}$ )	-10		10	mV	$CMV = 0\text{ V}$
$V_{IN}$ Bias Current	-0.5	<0.1>	0.5	$\mu\text{A}$	$V_{IN} = 0\text{ V}$
$V_A$ , $V_B$ Bias Current	-20		20	$\mu\text{A}$	$V_{IN} = 0\text{ V}$
Capacitance $V_{IN}$ , $V_A$ , $V_B$			2	pF	
Voltage Range ( $V_{CM}$ )	$-V_S + 2.7$		$+V_S - 2.5$	V	
Differential Voltage ( $V_{DIFF}$ )			9	V	
Nonlinearity	-5		5	mV	See Note 1
$V_A/V_B$ Interaction			0.1	mV/V	
<b>BIAS CURRENT</b>					
Change vs. Comparator State	-1		1	$\mu\text{A}$	
Nonlinearity	-2		2	$\mu\text{A}$	
Tempco		$\pm 0.1$		$\mu\text{A}/^\circ\text{C}$	
<b>LATCH ENABLE INPUTS</b>					
Common-Mode Range	-2		1	V	
Differential Voltage	0.4		3	V	
Logic “1” Current ( $I_{IH}$ )			200	$\mu\text{A}$	
Logic “0” Current ( $I_{IL}$ )	-10			$\mu\text{A}$	
<b>DIGITAL OUTPUTS</b>					
Logic “1” Voltage ( $V_{OH}$ )	-0.98			V	Q or $\bar{Q}$ , 50 $\Omega$ to -2 V
Logic “0” Voltage ( $V_{OL}$ )			-1.5	V	Q or $\bar{Q}$ , 50 $\Omega$ to -2 V
<b>SWITCHING PERFORMANCE</b>					
Propagation Delay					
Input to Output			2	ns	$V_{IN} = 2\text{ V p-p}$ , $t_{PDR}$ , $t_{PDF}$ , Figure 1, Note 2
Part-to-Part Skew			1	ns	
Change vs. Temperature		$\pm 1$		ps/ $^\circ\text{C}$	
<b>DISPERSION</b>					
5 V p-p Input (All Edges)		$\pm 100$		ps	10%, 90% 0.5 V/ns, 3 V/ns
5 V p-p Input (All Edges)		$\pm 175$		ps	10%, 90% 5 V/ns
V Slew = 1 V/ns (All Edges)		$\pm 50$		ps	10%, 90% 3 V, 5 V
V Slew = 1 V/ns (All Edges)		$\pm 50$		ps	20%, 80% 1 V
Minimum Pulsewidth		<1		ns	See Note 3
Edge Interaction		<200		ps	See Note 4
Duty Ratio		<100		ps	See Note 5
Comparator Interaction		<100		ps	

## NOTES

<sup>1</sup>Defined as change in  $V_{OS}$  from  $-V_S + 2.95\text{ V}$  to  $+V_S - 2.75\text{ V}$  (throughout the range) after  $V_A$  and  $V_B$  are corrected for gain and offset using 0 V and 5 V.

<sup>2</sup>Propagation delay is measured from the input threshold crossing at the 50% point of a 0 V to 5 V input to the output Q and  $\bar{Q}$  crossing.

<sup>3</sup>The minimum input pulsewidth that will maintain a 600 mV ECL swing on the output. The input is a 0 V to 3 V signal with a 3 V/ns rise and fall times. The input pulsewidth is measured between the 2.8 V point of a positive input pulse and the 0.2 V of a negative input pulse. See Figure 2.

<sup>4</sup>Maximum Change in propagation delay as the input pulse is reduced from 50 ns to a 2 ns pulsewidth. 0 V to 3 V swing with 3 V/ns rise/fall time and 25% duty cycle.

<sup>5</sup>Maximum Change in propagation delay as the input pulse is reduced from 99% to a 1% duty cycle. 0 V to 3 V swing with 3 V/ns rise/fall time and 50 ns to 4.95  $\mu\text{s}$  pulsewidth, period = 5  $\mu\text{s}$ .

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS\*

### Power Supply Voltage

+V <sub>S</sub> to GND	.....	+12 V
-V <sub>S</sub> to GND	.....	-8 V
+V <sub>S</sub> to -V <sub>S</sub>	.....	+17 V

### Inputs

V <sub>IN</sub> , V <sub>A</sub> , V <sub>B</sub>	.....	+V <sub>S</sub> - 13.5 V, -V <sub>S</sub> + 13.7 V
LEA, $\overline{LEA}$ , LEB, $\overline{LEB}$	.....	+V <sub>S</sub> - 14 V, -V <sub>S</sub> + 10 V

### Currents

I (+V <sub>S</sub> )	.....	95 mA
I (-V <sub>S</sub> )	.....	-75 mA
Q <sub>A</sub> , $\overline{Q_A}$ , Q <sub>B</sub> , $\overline{Q_B}$	.....	-40 mA to +2 mA

### Environmental

Operating Temperature (Ambient)	.....	0°C to +70°C
Storage Temperature	.....	-65°C to +125°C
Lead Temperature (Soldering, 20 sec)	.....	+300°C

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Absolute maximum limits apply individually, not in combination. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The device must suffer no reliability degradation if any supply pin is either shorted to ground or left floating for an indefinite periods of time during normal operation.

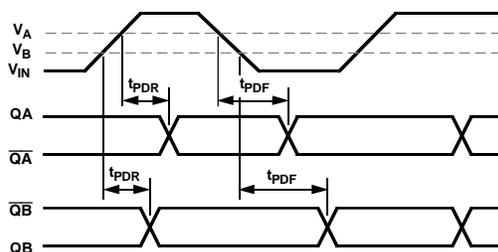
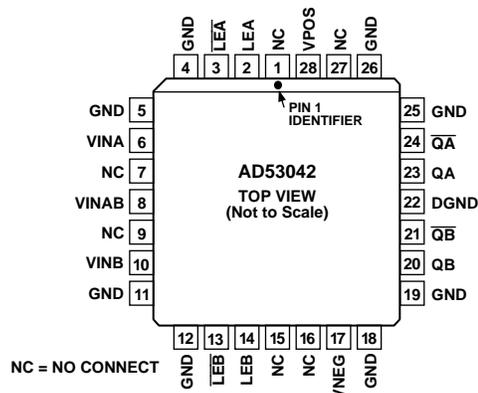


Figure 2. Timing Diagram

## ORDERING GUIDE

Model	Package Description	Shipment Method, Quantity Per Shipping Container	Package Option
AD53042KRP	28-Lead PLCC	Tube, 36 Pieces	P-28A

## PIN CONFIGURATION



## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD53042 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**28-Lead Plastic Leaded Chip Carrier  
(P-28A)**

