Twos Complement, Dual 12-Bit DACs with Internal REF and Fast Settling Time

AD5399

FEATURES

2-channel 12-bit DACs
Twos complement facilitates bipolar applications
Bipolar zero with 2 V dc offset
Built-in 2.000 V precision reference with 10 ppm/°C typ TC
Buffered voltage output, 0 V to 4 V
Single-supply operation, 4.5 V to 5.5 V
Fast 0.8 µs settling time typ
Ultra compact MSOP-10 package
Monotonic DNL < ±1 LSB
Optimized accuracy at zero scale
Power-on reset to V_{REF}
3-wire serial data input
Extended temperature range, –40°C to +105°C

APPLICATIONS

Single-supply bipolar converter operations
General-purpose DSP applications
Digital gain and offset controls
Instrumentation level settings
Disk drive control
Precision motor control

GENERAL DESCRIPTION

The AD5399 is the industry-first dual 12-bit digital-to-analog converter that accepts twos complement digital coding with 2 V dc offset for single-supply operation. Augmented with its built-in precision reference and solid buffer amplifier, the AD5399 is the smallest self-contained 12-bit precision DAC that fits many general-purpose as well as DSP specific applications. The twos complement programming facilitates the natural coding implementation commonly found in DSP applications and allows operation in single supply. The AD5399 provides a 2 V reference output, V_{REF}, for bipolar zero monitoring. It can also be used for other on-board components that require precision reference. The device is specified for operation from 5 V ±10% single supply with bipolar output swing from 0 V to 4 V centered at 2 V.

The AD5399 is available in the compact 1.1 mm low profile MSOP-10 package. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM

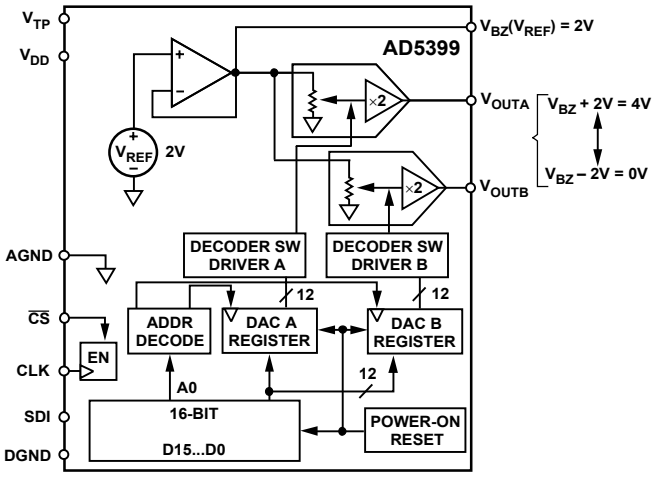

Figure 1.

V_{OUT} = ((D – 2048) / 4096 × 4 V) + 2 V for 0 ≤ D ≤ 4095 where D is the decimal code.

Table 1. Examples of Twos Complement Codes

Twos Complement	D	Scale	V_{OUT} (V)
2047	4095	+FS	4.000
2046	4094	+FS – 1 LSB	3.999
1	2049	BZS + 1 LSB	2.001
0	2048	BZS	2.000
4095	2047	BZS – 1 LSB	1.999
2049	1	–FS + 1 LSB	0.001
2048	0	–FS	0.000

FS = Full Scale, BZS = Bipolar Zero Scale

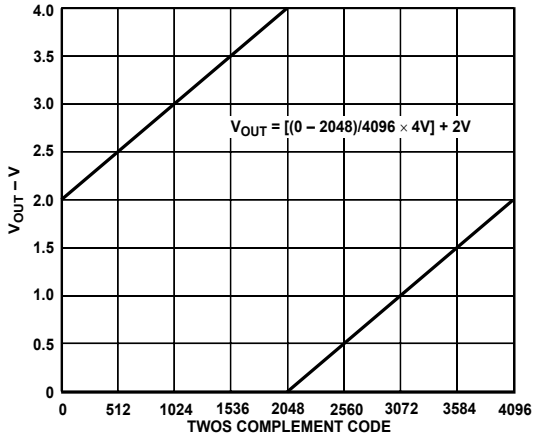

Figure 2. Output vs. Twos Complement Code

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

SPECIFICATIONS 3
ABSOLUTE MAXIMUM RATINGS 4
PIN CONFIGURATION AND FUNCTIONAL DESCRIPTION 5
TIMING CHARACTERISTICS 6
TYPICAL PERFORMANCE CHARACTERISTICS 7
OPERATION 10
OUTLINE DIMENSIONS 11

REVISION HISTORY

Revision A

Change to Table 1 1

Revision 0: Initial Version

SPECIFICATIONS

Table 2. ELECTRICAL CHARACTERISTICS (V_{DD} = +5 V ±10%, –40°C < T_A < +105°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS						
Resolution	N		12			Bits
Differential Nonlinearity Error	DNL		–1	±0.5	+1	LSB
Differential Nonlinearity Error	DNL	Codes 2048 to 2052, due to int. op amp offset	–1.2	±0.5	+1.2	LSB
Integral Nonlinearity Error	INL		–0.4	±0.02	+0.4	%FS
Positive Full-Scale Error	V_{+FSE}	Code = 0xF	–0.75	–0.15	+0.75	%FS
Bipolar Zero-Scale Error	V_{BZSE}	Code = 0x000	–0.75	–0.15	+0.75	%FS
Negative Full-Scale Error	$V_{–FSE}$	Code = 0x800	–0.75	–0.15	+0.75	%FS
ANALOG OUTPUTS						
Nominal Positive Full-Scale	$V_{OUTA/B}$	Code = 0x7FF		4		V
Positive Full-Scale Tempco[2]	$TCV_{OUTA/B}$	Code = 0x7FF, T_A = 0 to 70°C	–40	±10	+40	ppm/°C
Positive Full-Scale Tempco[2]	$TCV_{OUTA/B}$	Code = 0xFF, T_A = –40 to +105°C	–60	±10	+60	ppm/°C
Nominal V_{BZ} Output Voltage	V_{BZ}		1.995	2.000	2.004	V
Bipolar Zero Output Resistance[2]	R_{BZ}			1		Ω
V_{BZ} Output Voltage Tempco	TCV_{BZ}	T_A = 0°C to 70°C	–40	±10	+40	ppm/°C
V_{BZ} Output Voltage Tempco	TCV_{BZ}	T_A = –40 to +105°C	–60	±10	+60	ppm/°C
Nominal Peak-Peak Output Swing	$\|V_{+FS}\| + \|V_{–FS}\|$	Code 0x7FF to Code 0x800		4		V
DIGITAL INPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V, V_{DD} = 5 V			±1	µA
Input Capacitance[2]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ Range}$		4.5		5.5	V
Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = 0 V		1.8	2.6	mA
Supply Current in Shutdown	I_{DD_SHDN}	V_{IH} = V_{DD} or V_{IL} = 0 V, B14 = 0, T_A = 0°C to 105°C		10	100	µA
Supply Current in Shutdown	I_{DD_SHDN}	V_{IH} = V_{DD} or V_{IL} = 0 V, B14 = 0, T_A = –40 to 0°C		100	500	µA
Power Dissipation[3]	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = 0 V, V_{DD} = 5.5 V		9	13	mW
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = +5 V ±10%	–0.006	+0.003	+0.006	%/%
DYNAMIC CHARACTERISTICS[2]						
Settling Time	t_S	0.1% error band		0.8		µs
Digital Feedthrough	Q			10		nV.s
Bipolar Zero-Scale Glitch	G			10		nV.s
Capacitive Load Driving Capability	CL	No oscillation			1000	pF
INTERFACE TIMING CHARACTERISTICS[2, 4]						
SCLK Cycle Frequency	t_{CYC}				33	MHz
SCLK Clock Cycle Time	t_1		30			ns
Input Clock Pulsewidth	t_2, t_3	Clock level low or high	15			ns
Data Setup Time	t_4		5			ns
Data Hold Time	t_5		0			ns
FSYNC to SCLK Active Edge Setup Time	t_6		5			ns
SCLK to FSYNC Hold Time	t_7		0			ns
Minimum FSYNC High Time	t_8		30			ns

[1] Typicals represent average readings at 25°C and V_{DD} = 5 V.
[2] Guaranteed by design and not subject to production test.
[3] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.
[4] See Timing Diagram (Figure 4) for location of measured values. All input control voltages are specified with t_R = t_F = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using V_{DD} = 5 V. Input logic should have a 1 V/µs minimum slew rate.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Table 3. T_A = 25°C, unless otherwise noted.

Parameter	Rating
V_{DD} to GND	–0.3 V, +7.5 V
V_{OUTA}, V_{OUTB}, V_{BZ} to GND	0 V, V_{DD}
Digital Input Voltages to GND	0 V, V_{DD} + 0.3 V
Operating Temperature Range	–40°C to +105°C
Maximum Junction Temperature ($T_{J\ MAX}$)	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Package Power Dissipation	$(T_{J\ MAX} – T_A) / \theta_{JA}$
Thermal Resistance θ_{JA}, MSOP-10	206°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTION

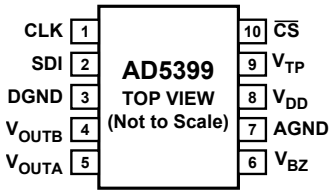

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Name	Description
1	CLK	Serial Clock Input. Positive edge triggered.
2	SDI	Serial Data Input. MSB first format.
3	DGND	Digital Ground.
4	V_{OUTB}	DAC B Voltage Output (A0 = Logic 1).
5	V_{OUTA}	DAC A Voltage Output (A0 = Logic 0).
6	V_{BZ}	2 V, Virtual Bipolar Zero (Active Output).
7	AGND	Analog Ground.
8	V_{DD}	Positive Power Supply. Specified for operation at 5 V.
9	V_{TP}	Connect to V_{DD}. Reserved for factory testing.
10	$\overline{CS}$	Chip Select (Frame Sync Input), Active Low. When $\overline{CS}$ returns high, data in the serial input register is transferred into the DAC register.

Table 5. Serial Data-Word Format

ADDR				DATA						
B15	B14	B13	B12	B11	B10	…	B3	B2	B1	B0
A0	X	SD	0	D11	D10	…	D3	D2	D1	D0
MSB										LSB

A0 Address Bit. Logic low selects Channel 1 and logic high selects Channel 2.

X Don't Care.

SD Shutdown Bit. Logic high puts both DAC outputs and V_{BZ} into high impedance.

D0–D11 Data Bits.

TIMING CHARACTERISTICS

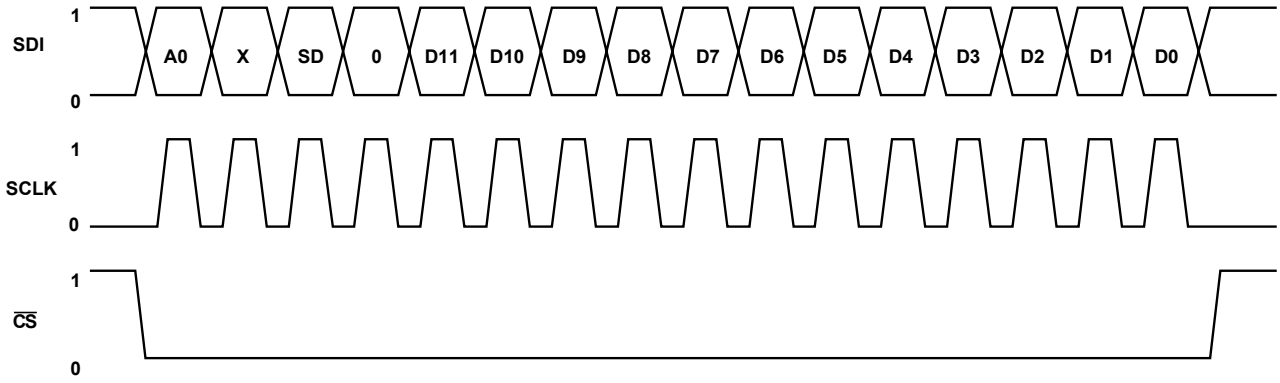

Figure 4. Timing Diagram

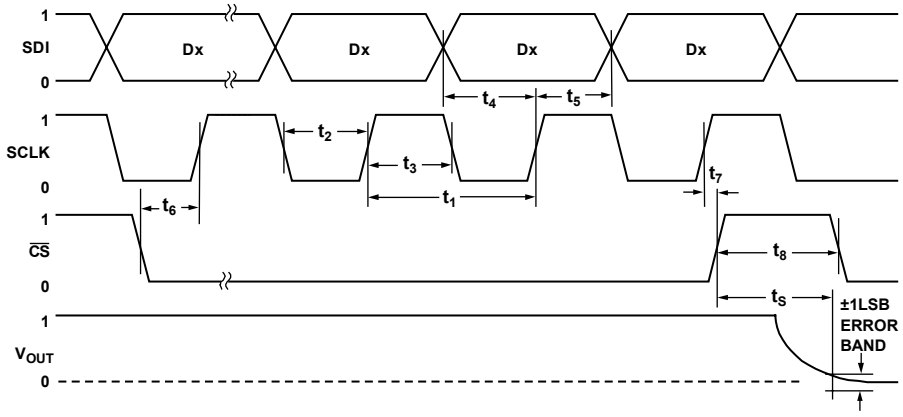

Figure 5. Detailed Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

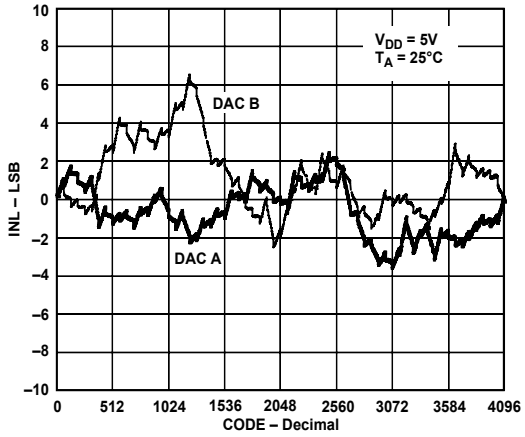

Figure 6. Integral Nonlinearity Errors

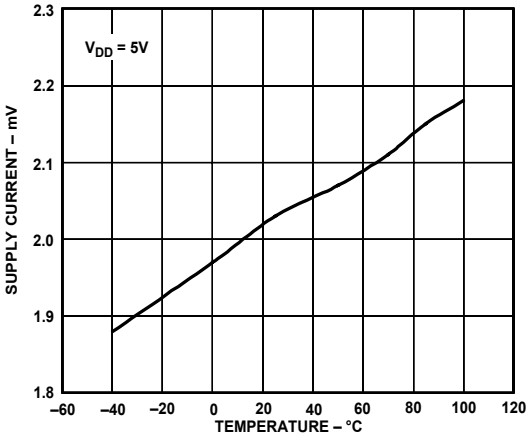

Figure 9. Supply Current vs. Temperature

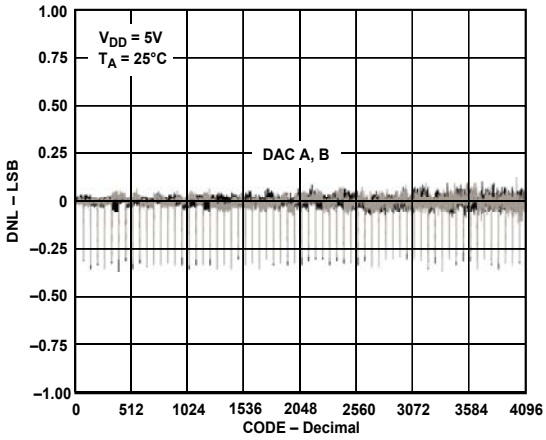

Figure 7. Differential Nonlinearity Errors

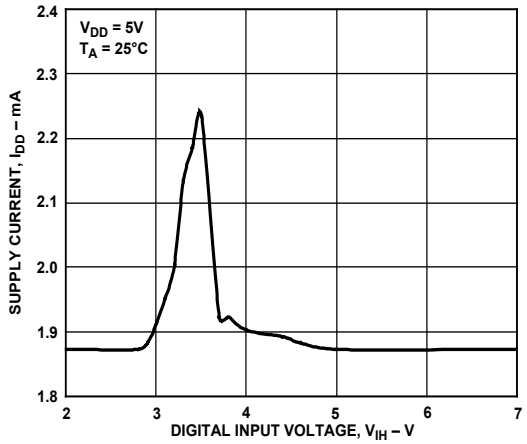

Figure 10. Supply Current vs. Digital Input Voltage

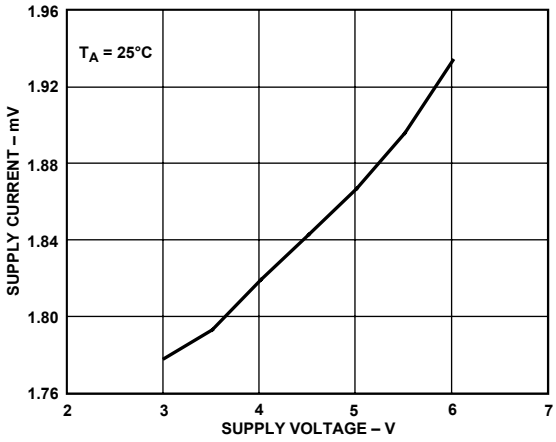

Figure 8. Supply Current vs. Supply Voltage

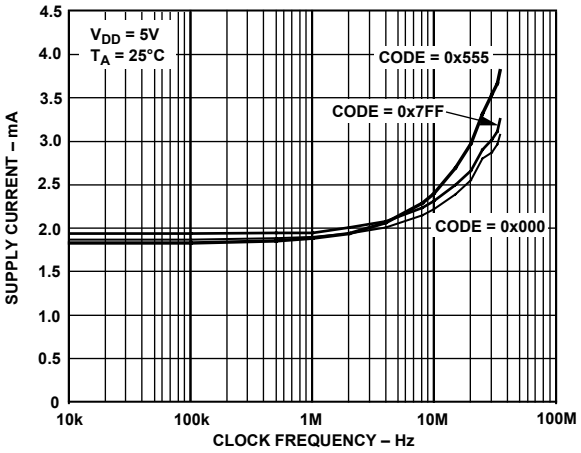

Figure 11. Supply Current vs. Clock Frequency

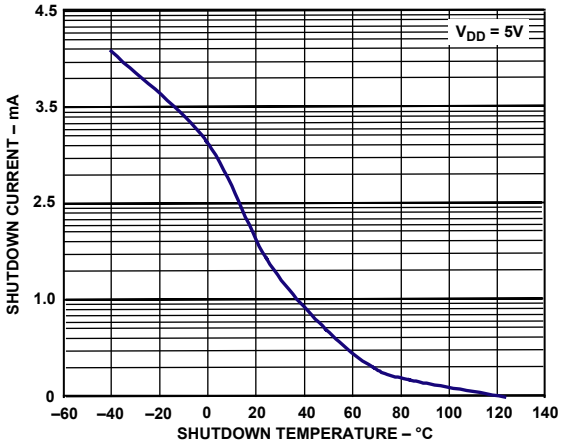

Figure 12. Shutdown Current vs. Temperature

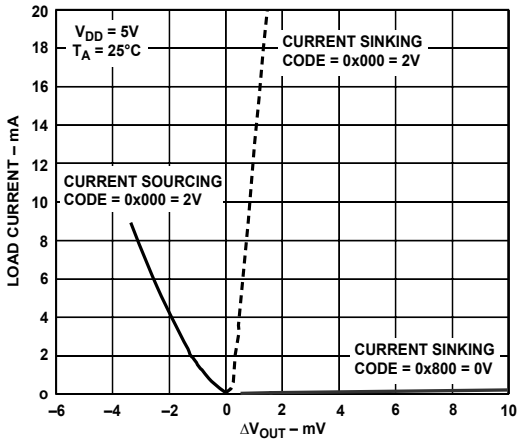

Figure 13. Load Current vs. Voltage Drop

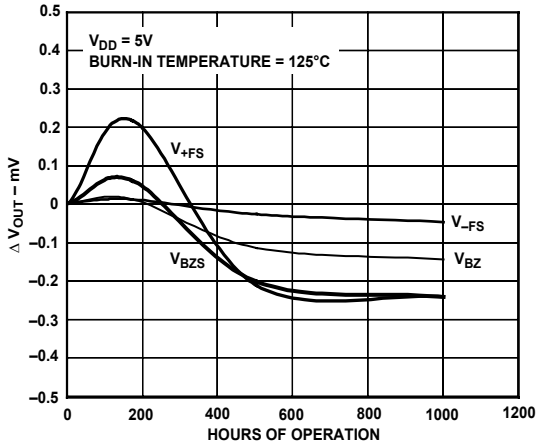

Figure 14. Long-Term Drift

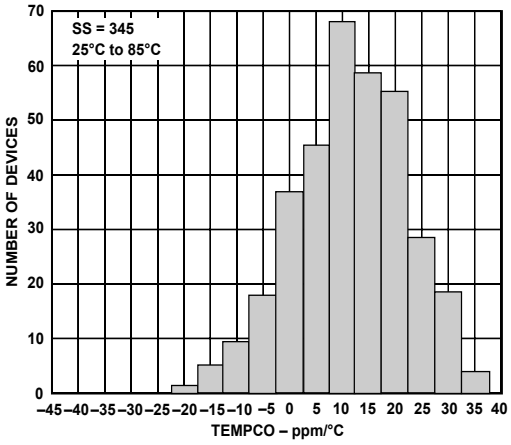

Figure 15. V_{BZ} Temperature Coefficient (T_A = 25°C to 85°C)

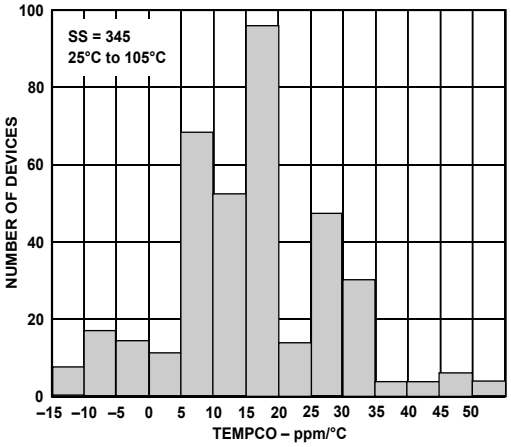

Figure 16. V_{BZ} Temperature Coefficient (T_A = 25°C to 105°C)

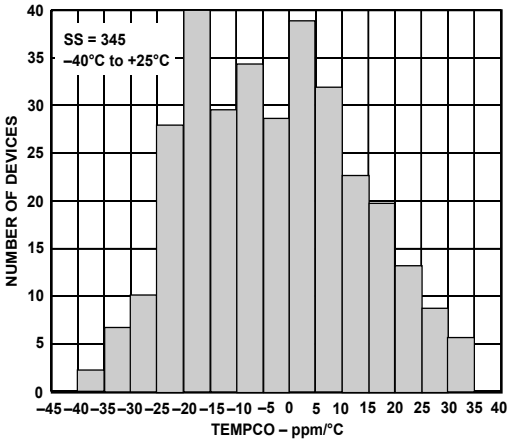

Figure 17. V_{BZ} Temperature Coefficient (T_A = –40°C to +25°C)

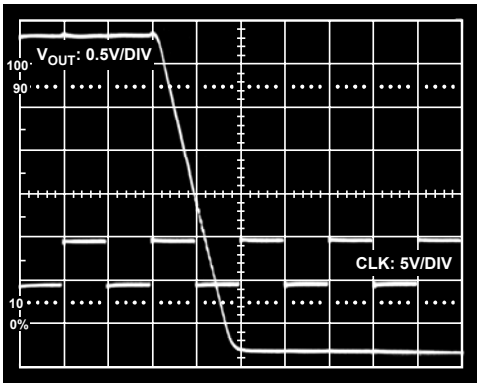

Figure 18. Large Signal Settling (0.5 µs/DIV)

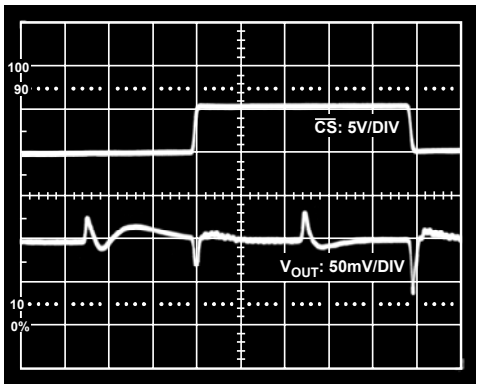

Figure 19. Midscale Glitch and Digital Feedthrough (2 µs/DIV)

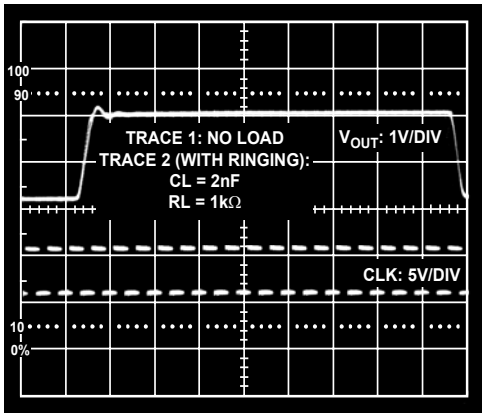

Figure 20. Capacitive Load Output Performance (2 µs/DIV)

OPERATION

The AD5399 provides a 12-bit, twos complement, dual voltage output, digital-to-analog converter (DAC). It has an internal reference with 2 V bipolar zero dc offset, where $0 \le V_{OUT} \le 4$ V.

The output transfer equation is:

$V_{OUT} = ((D - 2048) / 4096 \times 4\ V) + 2\ V$

where:

D is the 12-bit decimal data and not the twos complement code.

V_{OUT} is with respect to ground.

In data programming, the data is loaded MSB first on the positive clock edge (SCLK) when the chip select ($\overline{CS}$) input is active low. The digital word is 16 bits wide with the MSB, B15, as an address bit (DAC A: A0 = 0; DAC B: A0 = 1). B14 is don't care, B13 is a shutdown bit, B12 must be logic low, and the last 12 bits are data bits. All 16 bits clocked into the register will be transferred to the internal DAC register when $\overline{CS}$ returns to logic high.

Table 6. Input Logic Control Truth Table

CLK	$\overline{CS}$	Register Activity
L	H	No Shift Register Effect
P	L	Shift One Bit in from the SDI Pin
L	P	Transfer SR Data into DAC Register
X	L	No Operation

P = Positive Edge, X = Don't Care, SR = Shift Register

The data setup and data hold times in the Specifications table (Table 2) determine the timing requirements. The internal power-on reset circuit clears the serial input registers to all zeros, and sets the two DAC registers to a V_{BZ} (zero code) of 2 V.

Software shutdown B13 turns off the internal REF and amplifiers. The output will be close to zero potential, and the digital circuitry remains active such that new data can be written. Therefore, the DAC register will be refreshed with the new data once the shutdown bit is deactivated.

All digital inputs are ESD protected with a series input resistor and parallel Zener, as shown in Figure 21, that apply to digital input pins CLK, SDA, and $\overline{CS}$. The basic connection is shown in Figure 22.

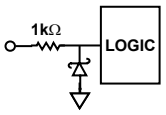

Figure 21. Equivalent ESD Protection Circuit

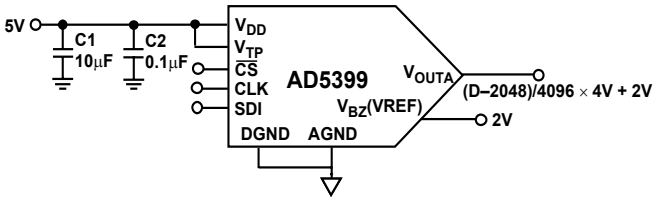

Figure 22. Basic Connection

OUTLINE DIMENSIONS

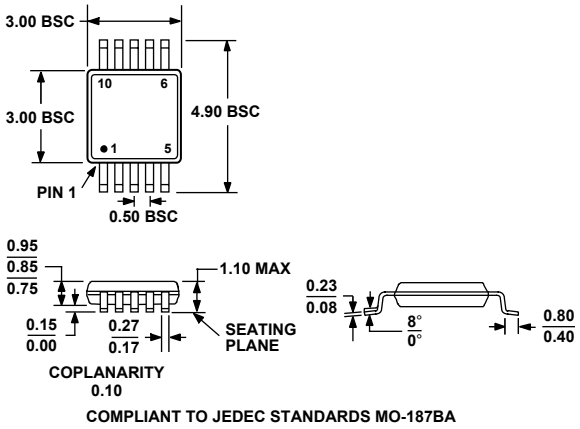

Figure 23. 10-Lead MSOP Package (RM-10)
Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Table 7.

Model	Temp Range	Package	Package Code	Top Brand	Ordering Quantity
AD5399YRM	–40°C to +105°C	MSOP-10	RM-10	DSB	50
AD5399YRM-REEL7	–40°C to +105°C	MSOP-10	RM-10	DSB	1500

C03469-0-3/03(A)