Low Power Mixer/Limiter/RSSI 3 V Receiver IF Subsystem

AD608

FEATURES

Mixer
- **–15 dBm 1 dB Compression Point**
- **–5 dBm IP3**
- **24 dB Conversion Gain**
- **>500 MHz Input Bandwidth**

Logarithmic/Limiting Amplifier
- **80 dB RSSI Range**
- **±3° Phase Stability over 80 dB Range**

Low Power
- **21 mW at 3 V Power Consumption**
- **CMOS-Compatible Power-Down to 300 μW typ**
- **200 ns Enable/Disable Time**

APPLICATIONS
- **PHS, GSM, TDMA, FM, or PM Receivers**
- **Battery-Powered Instrumentation**
- **Base Station RSSI Measurement**

GENERAL DESCRIPTION

The AD608 provides both a low power, low distortion, low noise mixer and a complete, monolithic logarithmic/limiting amplifier using a "successive-detection" technique. It provides both a high speed RSSI (Received Signal Strength Indicator) output with 80 dB dynamic range and a hard-limited output. The RSSI output is from a two-pole post-demodulation low-pass filter and provides a loadable output voltage of +0.2 V to +1.8 V. The AD608 operates from a single 2.7 V to 5.5 V supply at a typical power level of 21 mW at 3 V.

The RF and LO bandwidths both exceed 500 MHz. In a typical IF application, the AD608 will accept the output of a 240 MHz SAW filter and downconvert it to a nominal 10.7 MHz IF with a conversion gain of 24 dB (Z_{IF} = 165 Ω). The AD608's logarithmic/limiting amplifier section handles any IF from LF to as high as 30 MHz.

The mixer is a doubly-balanced "Gilbert-Cell" type and operates linearly for RF inputs spanning –95 dBm to –15 dBm. It has a nominal –5 dBm third-order intercept. An onboard LO preamplifier requires only –16 dBm of LO drive. The mixer's current output drives a reverse-terminated, industry-standard 10.7 MHz 330 Ω filter.

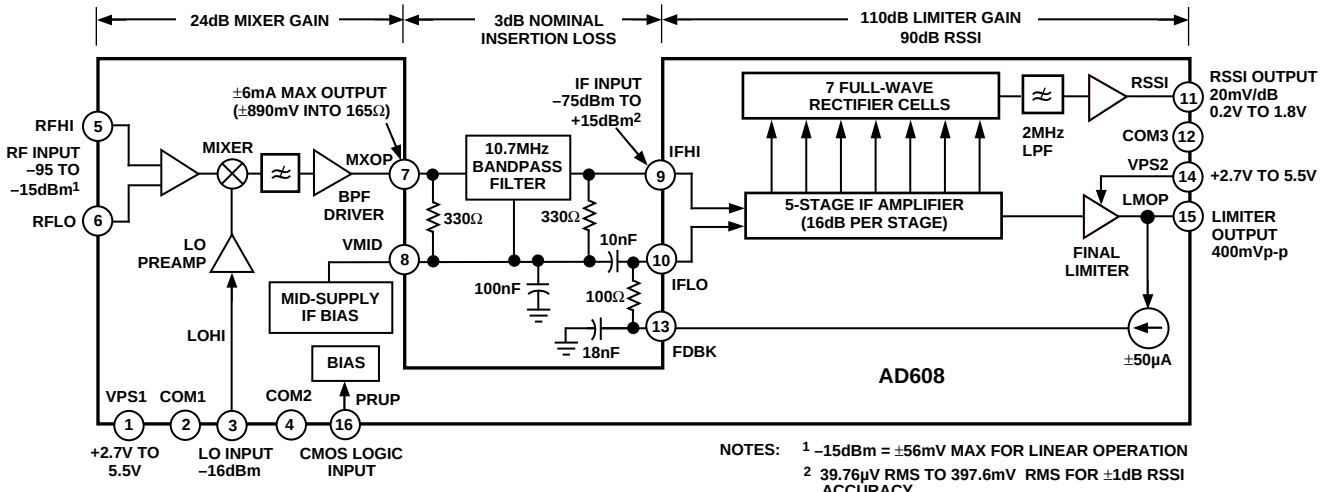
The nominal logarithmic scaling is such that the output is +0.2 V for a sinusoidal input to the IF amplifier of –75 dBm and +1.8 V at an input of +5 dBm; over this range the logarithmic conformance is typically ±1 dB. The logarithmic slope is proportional to the supply voltage. A feedback loop automatically nulls the input offset of the first stage down to the submicrovolt level.

The AD608's limiter output provides a hard-limited signal output at 400 mV p-p. The voltage gain of the limiting amplifier to this output is more than 100 dB. Transition times are 11 ns and the phase is stable to within ±3° at 10.7 MHz for signals from –75 dBm to +5 dBm.

The AD608 is enabled by a CMOS logic-level voltage input, with a response time of 200 ns. When disabled, the standby power is reduced to 300 μW within 400 ns.

The AD608 is specified for the industrial temperature range of –25°C to +85°C for 2.7 V to 5.5 V supplies and –40°C to +85°C for 4.5 V to 5.5 V supplies. It comes in a 16-pin plastic SOIC.

FUNCTIONAL BLOCK DIAGRAM



REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD608—SPECIFICATIONS (@ T_A = + 25°C, Supply = 3 V, dBm is referred to 50 Ω, unless otherwise noted)

Model	Conditions	AD608 Min	AD608 Typ	AD608 Max	Units
MIXER PERFORMANCE					
RF and LO Frequency Range			500		MHz
LO Power	Input Terminated in 50 Ω		–16		dBm
Conversion Gain	Driving Doubly-Terminated 330 Ω IF Filter, Z_{IF} = 165 Ω	19	24	28	dB
Noise Figure	Matched Input, f_{RF} = 100 MHz		11		dB
	Matched Input, f_{RF} = 240 MHz		16		dB
1 dB Compression Point	Input Terminated in 50 Ω		–15		dBm
Third-Order Intercept	f_{RF} = 240 MHz and 240.02 MHz, f_{LO} = 229.3 MHz		–5		dBm
Input Resistance	f_{RF} = 100 MHz (See Table I)		1.9		kΩ
Input Capacitance	f_{RF} = 100 MHz (See Table I)		3		pF
LIMITER PERFORMANCE					
Gain	Full Temperature and Supply Range		110		dB
Limiting Threshold	3° rms Phase Jitter at 10.7 MHz		–75		dBm
	280 kHz IF Bandwidth				
Input Resistance			10		kΩ
Input Capacitance			3		pF
Phase Variation	–75 dBm to +5 dBm IF Input Signal at 10.7 MHz		±3		Degree
DC Level	Center of Output Swing (VPOS-1)		2		V
Output Level	Limiter Output Driving 5 kΩ Load		400		mV p-p
Rise and Fall Times	Driving a 5 pF Load		11		ns
Output Impedance			200		Ω
RSSI PERFORMANCE	At 10.7 MHz				
Nominal Slope	At VPOS = 3 V; Proportional to VPOS	17.27	20	23.27	mV/dB
Nominal Intercept			–85		dBm
Minimum RSSI Voltage	–75 dBm Input Signal		0.2		V
Maximum RSSI Voltage	+5 dBm Input Signal		1.8		V
RSSI Voltage Intercept	0 dBm Input Signal	1.57		1.82	V
Logarithmic Linearity Error	–75 dBm to +5 dBm Input Signal at IFHI		±1		dB
RSSI Response Time	90% RF to 50% RSSI		200		ns
Output Impedance	At Midscale		250		Ω
POWER-DOWN INTERFACE					
Logical Threshold	System Active on Logical High		1.5		V
Input Current	For Logical High		75		μA
Power-Up Response Time	Active Limiter Output		200		ns
Power-Down Response Time	To 200 μA Supply Current		400		ns
Power-Down Current			100		μA
POWER SUPPLY					
Operating Range	–25°C to +85°C	2.7		5.5	V
	–40°C to +85°C	4.5		5.5	V
Powered Up Current	VPOS = 3 V		7.3		mA
OPERATING TEMPERATURE					
T_{MIN} to T_{MAX}	VPOS = 2.7 V to 5.5 V	–25		+85	°C
T_{MIN} to T_{MAX}	VPOS = 4.5 V to 5.5 V	–40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage VPS1, VPS2 . . . . . +6 V
Internal Power Dissipation[2] . . . . . 600 mW
Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering 60 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics:
16-Pin SOIC Package: θ_{JA} = 110°C/W.

ORDERING GUIDE

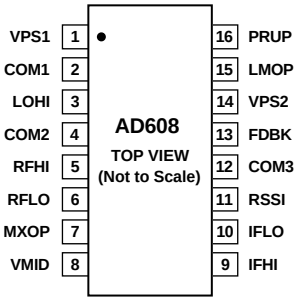
Model	Temperature Range	Package Option
AD608AR	–25°C to +85°C, 2.7 V to 5.5 V Supplies; –40°C to +85°C, 4.5 V to 5.5 V Supplies	R-16A*

*R = Small Outline IC (SOIC).

PIN DESCRIPTIONS

Pin	Mnemonic	Description
1	VPS1	Positive Supply Input
2	COM1	Common
3	LOHI	Local Oscillator Input Connection
4	COM2	Common
5	RFHI	RF Input, Noninverting
6	RFLO	RF Input, Inverting
7	MXOP	Mixer Output
8	VMID	Midpoint Supply Bias Output
9	IFHI	IF Input, Noninverting
10	IFLO	IF Input, Inverting
11	RSSI	Received Signal Strength Indicator Output
12	COM3	Output Common
13	FDBK	Offset-Null Feedback Loop Output
14	VPS2	Limiter Positive Supply Input
15	LMOP	Limiter Output
16	PRUP	Power-Up

TERMINAL DIAGRAM



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD608 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

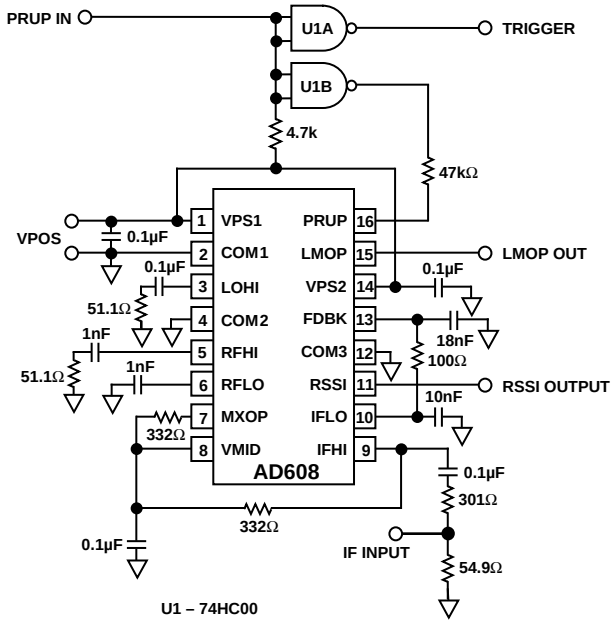


Figure 1. IF Test Board Schematic

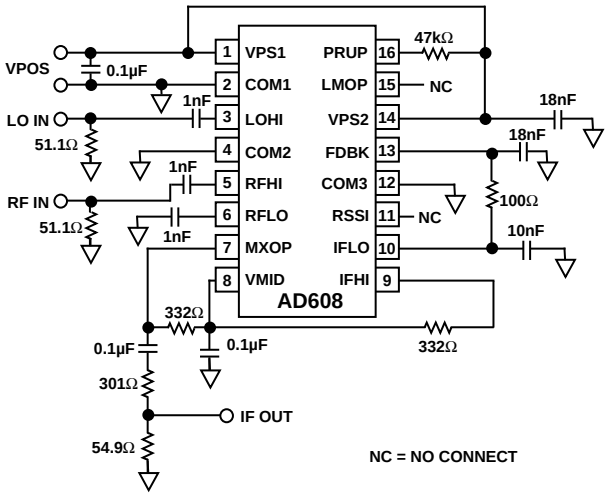


Figure 2. Mixer Test Board Schematic

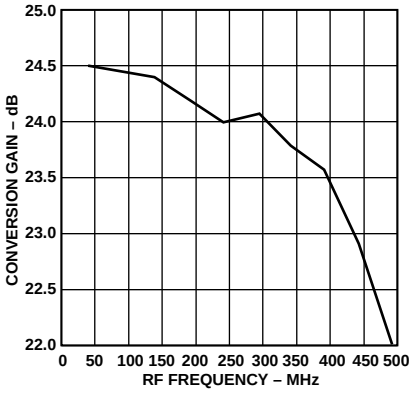


Figure 3. Mixer Conversion Gain vs. Frequency

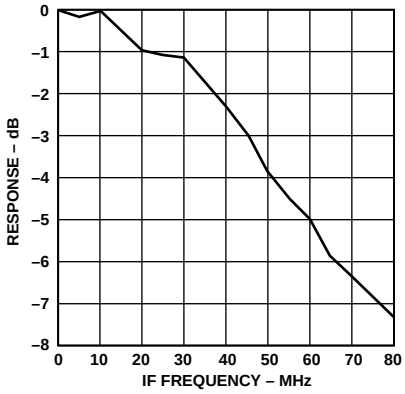


Figure 4. Mixer IF Port Bandwidth

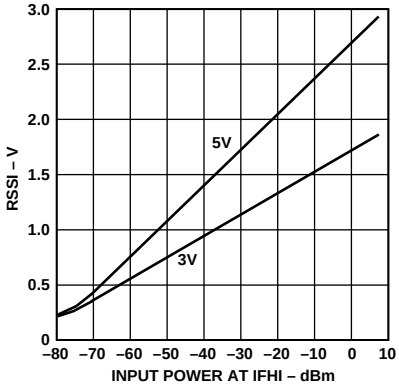


Figure 5. IF RSSI Output vs. Supply Voltage (Ambient Temperature)

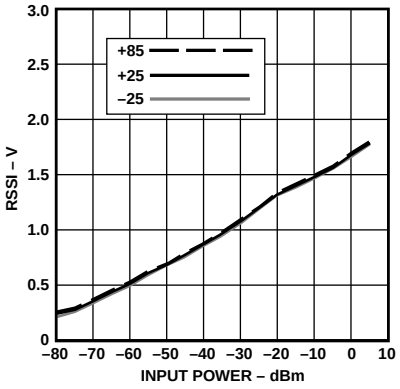


Figure 6. IF RSSI Output vs. Temperature (3 V Supply)

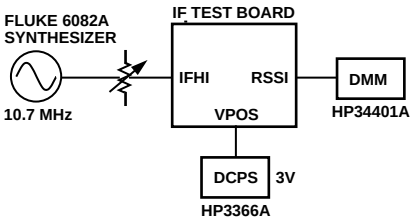


Figure 7. Test Circuit for IF RSSI Output vs. Supply Voltage (Ambient Temperature) (Figure 5) and IF RSSI Output vs. Temperature (3 V Supply) (Figure 6) and RSSI Error vs. Input Power (Figure 8)

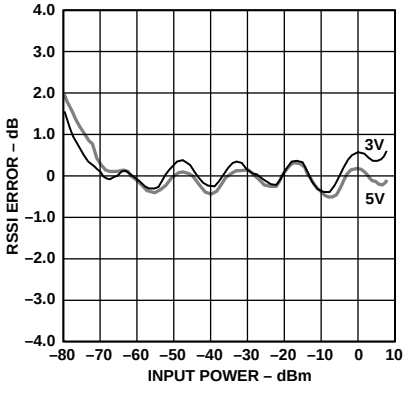


Figure 8. RSSI Error vs. Input Power

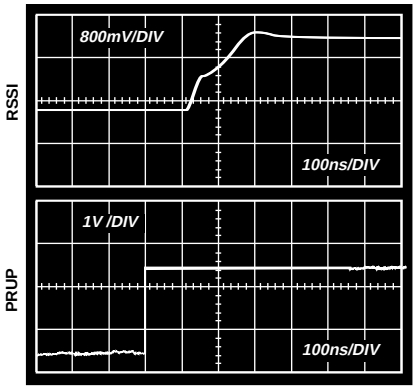


Figure 9. RSSI Power-Up Response

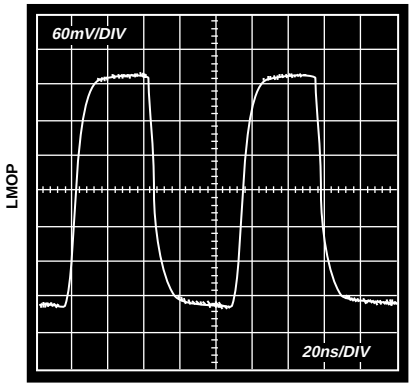


Figure 13. Limiter Rise and Fall Times

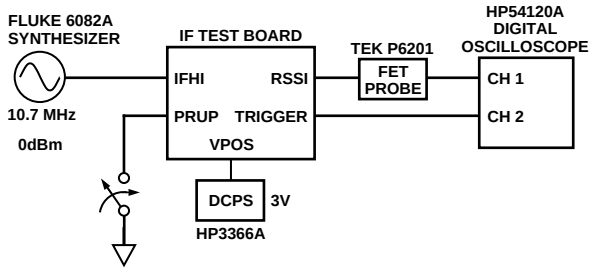


Figure 10. Test Circuit for RSSI Power-Up Response (Figure 9)

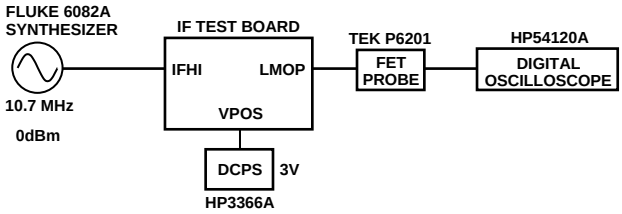


Figure 14. Test Circuit for Limiter Rise and Fall Times (Figure 13)

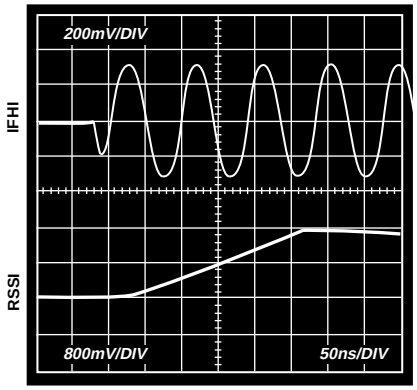


Figure 11. RSSI Pulse Response/RSSI Rise Time

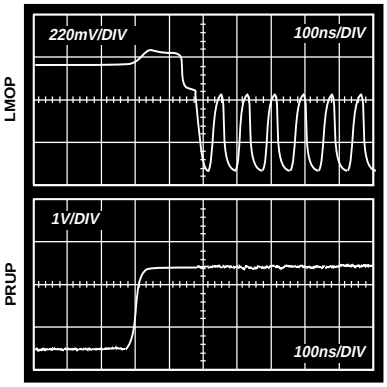


Figure 15. Limiter Power-Up Response Time

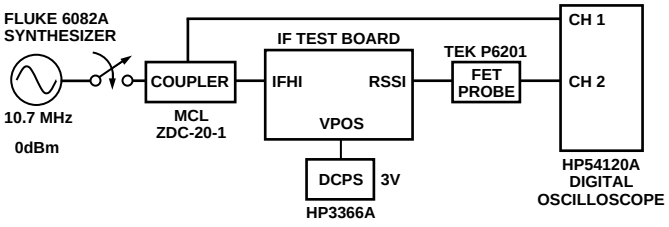


Figure 12. Test Circuit for RSSI Pulse Response/RSSI Rise Time (Figure 11)

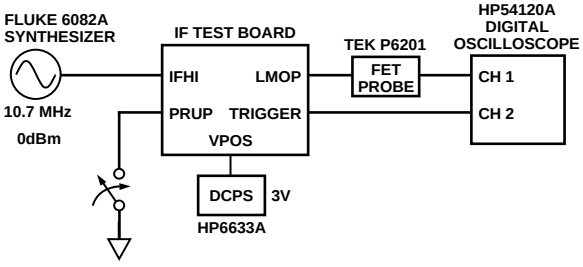


Figure 16. Test Circuit for Limiter Power-Up Response Time (Figure 15)

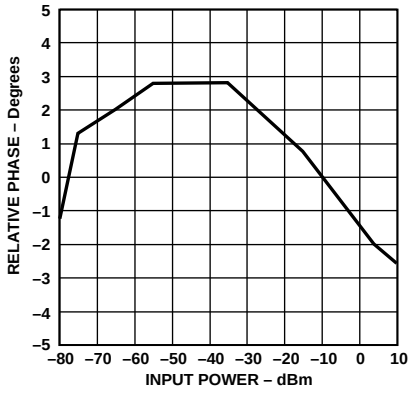


Figure 17. Limiter Phase Performance vs. Input Power at IFHI

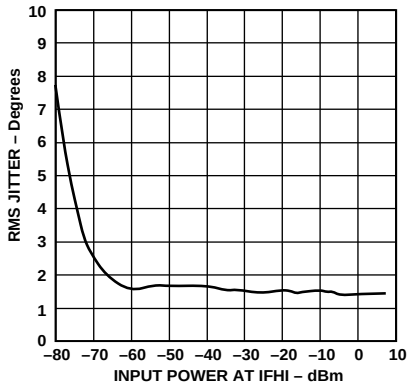


Figure 19. Limiter Jitter Performance vs. Input Power at IFHI

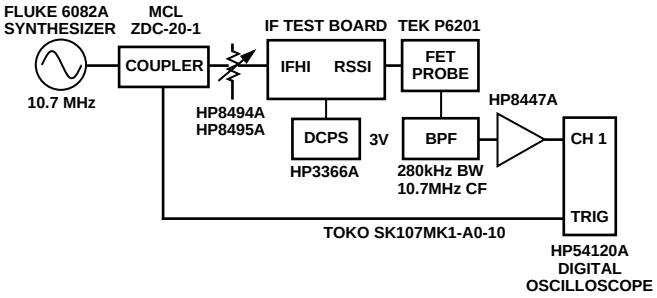


Figure 18. Test Circuit for Limiter Phase Performance vs. Input Power at IFHI (Figure 17) and Limiter Jitter Performance vs. Input Power at IFHI (Figure 19)

THEORY OF OPERATION

The AD608 (Figure 20) consists of a mixer followed by a logarithmic IF strip with RSSI and hard limited outputs. Each section will be described below.

Mixer

The mixer is a doubly-balanced modified Gilbert cell mixer. Its maximum input level for linear operation is ±56.2 mV regardless of the impedance across the mixer's inputs, or –15 dBm for a 50 Ω input termination. The input impedance of the mixer can be modeled as a simple parallel RC network; the values versus frequency are listed in Table I. The bandwidth from the RF input to the IF output at MXOP pin is –1 dB at 30 MHz and then falls off rapidly (Figure 4).

Mixer Gain

The mixer's conversion gain is the product of its transconductance and the impedance seen at pin MXOP. For a 330 Ω parallel-terminated filter at 10.7 MHz, the load impedance is 165 Ω, the gain is 24 dB, and the output is 15.85 × 56.2 mV, or ±891 mV, centered on the midpoint of the supply voltage. For other load impedances, the expression for the gain in dB is

$$G_{dB} = 20\ log_{10}\left(0.0961\ R_L\right)$$

The mixer's gain can be increased or decreased by changing R_L, the load impedance at pin MXOP. The limitations on the mixer's gain are the ±6 mA maximum output current at MXOP and the maximum allowable voltage swing at pin MXOP, which is ±1.0 V for a 3 V supply or 5 V supply.

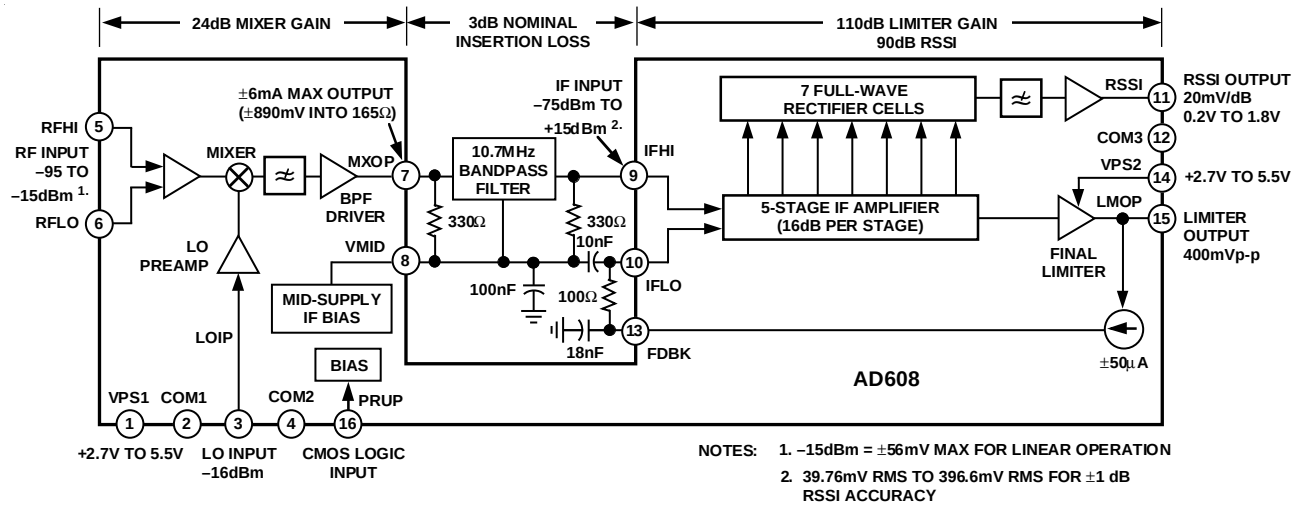


Figure 20. Functional Block Diagram

Table I. Mixer Input Impedance vs. Frequency

Frequency (MHz)	Resistance (Ohms)	Capacitance (pF)
45	2800	3.1
70	2600	3.1
100	1800	3.1
200	1200	3.1
300	760	3.2
400	520	3.4
500	330	3.6

IF Filter Terminations

The AD608 was designed to drive a parallel-terminated 10.7 MHz bandpass filter with a 330 Ω impedance. With a 330 Ω parallel-terminated filter, pin MXOP sees a 165 Ω termination and the gain is nominally 24 dB. Other filter impedances and gains can be accommodated by either accepting an increase or decrease in gain in proportion to the filter impedance or by keeping the impedance seen by MXOP a nominal 165 Ω (by using resistive dividers or matching networks). Figure 21 shows a simple resistive voltage divider for matching an assortment of filter impedances, and Table II lists component values.

The Logarithmic IF Amplifier

The logarithmic IF amplifier consists of five amplifier stages of 16 dB gain each, plus a final limiter. The IF bandwidth is 30 MHz (–1 dB) and the limiting gain is 110 dB. The phase skew is ±3° from –75 dBm to +5 dBm (approximately 111 μV p-p to 1.1 V p-p). The limiter output impedance is 200 Ω and the limiter's output drive is ±200 mV (400 mV p-p) into a 5 kΩ load. In the absence of an input signal, the limiter's output will limit on noise fluctuations, which produces an output that continues to swing 400 mV p-p but with random zero crossings.

Offset Feedback Loop

Because the logarithmic amplifier is dc coupled and has more than 110 dB of gain from the input to the limiter output, a dc offset at its input of even a few μV would cause the output to saturate. Thus, the AD608 uses a low frequency feedback loop to null out the input offset. Referring to Figure 21, the loop consists of a current source driven by the limiter, which sends 50 μA current pulses to pin FDBK. The pulses are low pass filtered by a π-network consisting of C1, R4, and C5. The smoothed dc voltage that results is subtracted from the input to the IF amplifier at pin IFLO. Because this is a high gain amplifier with a feedback loop, care should be taken in layout and component values to prevent oscillation. Recommended values for the common IFs of 450 kHz, 455 kHz, 6.5 MHz, and 10.7 MHz are listed in Table II.

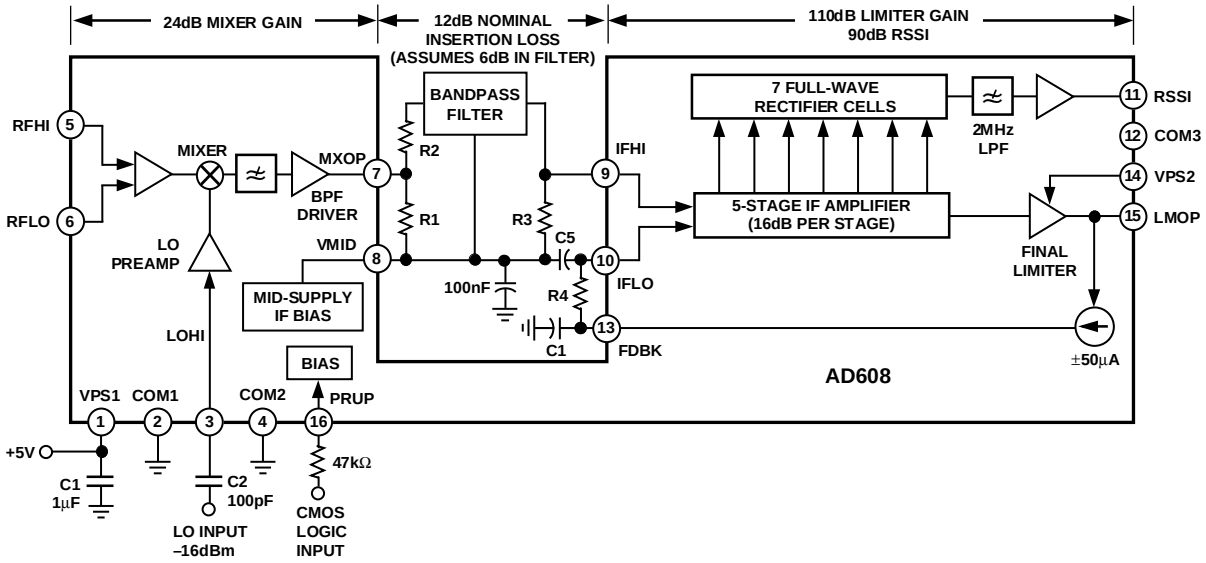


Figure 21. Applications Diagram for Common IFs and Filter Impedances

Table II. AD608 Filter Termination and Offset-Null Feedback Loop Resistor and Capacitor Values for Common IFs

IF	Filter Impedance	Filter Termination Resistor Values[1] for 24 dB of Mixer Gain			Offset Null Feedback Loop Values		
		R1	R2	R3	R4	C1	C5
450 kHz[2]	1500 Ω	174 Ω	1330 Ω	1500 Ω	1000 Ω	200 nF	100 nF
455 kHz	1500 Ω	174 Ω	1330 Ω	1500 Ω	1000 Ω	200 nF	100 nF
6.5 MHz	1000 Ω	178 Ω	825 Ω	1000 Ω	100 Ω	18 nF	10 nF
10.7 MHz	330 Ω	330 Ω	0 Ω	330 Ω	100 Ω	18 nF	10 nF

NOTES

[1]Resistor values were calculated so that R1 + R2 = Z_{FILTER} and R1‖(R2+Z_{FILTER}) = 165 Ω.

[2]Operation at IFs of 450 kHz and 455 kHz requires an external low pass filter with at least one pole at a cutoff frequency of 90 kHz (a decade below the ripple at 900 kHz).

RSSI Output

The logarithmic amplifier uses a successive detection architecture. Each of the five stages has a full-wave detector; two additional high level detectors are driven through attenuators at the input to the limiting amplifiers, for a total of seven detector stages. Because each detector is a full-wave rectifier, the ripple component in the resulting dc is at twice the IF. The AD608's low-pass filter has a 2 MHz cutoff frequency, which is one decade below the 21.4 MHz ripple that results from a 10.7 MHz IF.

For operation at lower IFs such as 450 kHz or 455 kHz, the AD608 requires an external low-pass filter with a single pole located at 90 kHz, a decade below the 900 kHz ripple frequency for these IFs. The RSSI range is from the noise level at approximately –80 dBm to overload at +15 dBm and is specified for ±1 dB accuracy from –75 dBm to +5 dBm. The +15 dBm maximum IF input is provided to accommodate bandpass filters of lower insertion loss than the nominal 4 dB for 10.7 MHz ceramic filters.

Digitizing the RSSI

In typical cellular radio applications, the RSSI output of the AD608 will be digitized by an A/D converter. The AD608's RSSI output is proportional to the power-supply voltage, which not only allows the A/D converter to use the supply as a reference but also causes the RSSI output and the A/D converter's output to track over power supply variations, reducing system errors and component costs.

Power Consumption

The total power-supply current of the AD608 is a nominal 7.3 mA. The power is signal-dependent, partly as the RSSI output increases (the current is increased by 200 μA at an RSSI output of +1.8 V) but mostly due to the IF BPF consumption when being driven to ±891 mV assuming a 4 dB loss in this filter and a peak input of +5 dBm to the log-IF amp, and temperature dependent, as the biasing system used in the AD608 is proportional to absolute temperature (PTAT).

Troubleshooting

The most common causes of problems with the AD608 are incorrect component values for the offset feedback loop, poor board layout, and pickup of RFI, which all cause the AD608 to "lose" the low end (typically below –65 dBm) of its RSSI output and cause the limiter to swing randomly. Both poor board layout and incorrect component values in the offset feedback loop can cause low level oscillations. Pickup of RFI can be caused by improper layout and shielding of the circuit.

Applications

Figure 22 shows the AD608 configured for operation in a digital system at a 10.7 MHz IF. The filter's input and output impedance are parallel terminated using 330 Ω resistors and the conversion gain is 24 dB. The RF port is terminated in 50 Ω; in a typical application the input would be matched to a SAW filter using the impedance data shown previously in Table I.

Figure 23 shows the AD608 configured for narrowband FM operation at a 450 kHz or 455 kHz with an external discriminator. The IF filter has 1500 Ω input and output impedances— the input is matched via a resistive divider and the output is terminated in 1500 Ω. The discriminator requires 1 V p-p drive from a 1 kΩ source impedance, here provided by a gain-of-2.5 Class A amplifier.

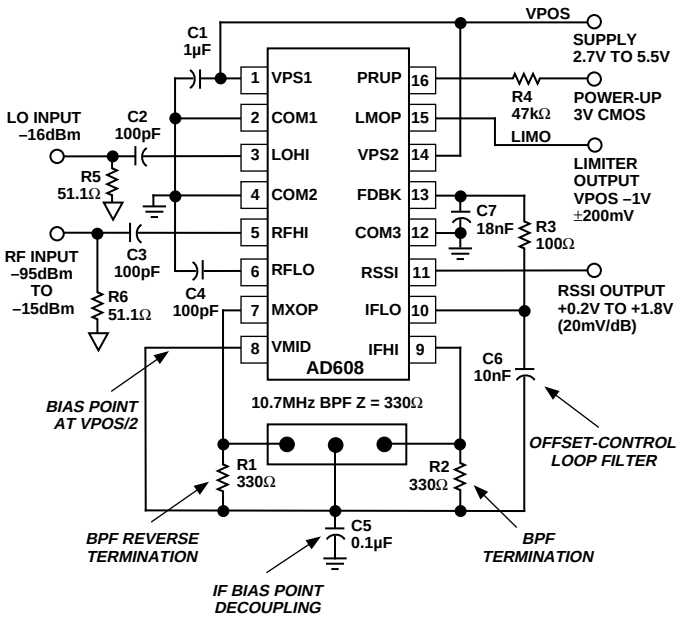


Figure 22. Application at 10.7 MHz. The Bandpass Filter Can Be a Toko Type SK107 or Murata Type SFE10.7

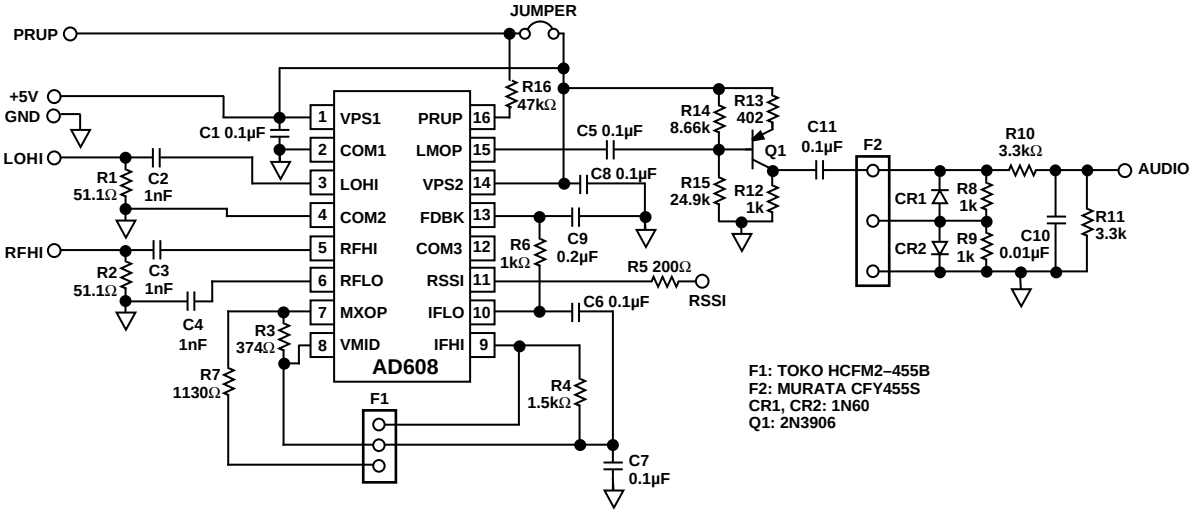
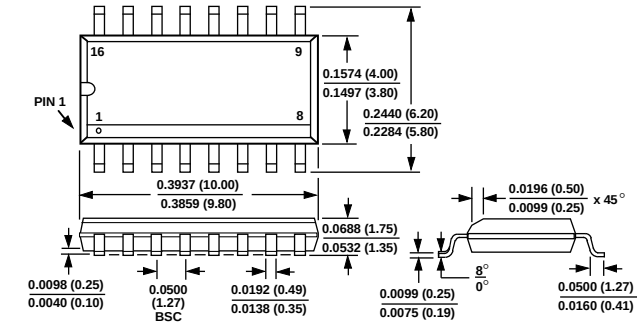


Figure 23. Narrowband FM Application at 450 kHz or 455 kHz

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead SOIC
(R-16A)



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C1990b–2–7/96