GSM/GPRS Digital Baseband Processor For Smartphone and Wireless Handheld Devices

Preliminary Technical Data AD6528

FEATURES

Complete Single Chip Programmable Digital Baseband Processor divided into three main subsystems:
- **Control Processor Subsystem including:**
  - **32-bit MCU ARM7TDMI® Control Processor**
  - **On-chip System SRAM Memory**
- **DSP Subsystem including**
  - **16-bit Fixed Point DSP Processor**
  - **Expanded Data and Program SRAM**
  - **Program Instruction Cache**
  - **Full Rate, Enhanced Full Rate and Half Rate Speech Encoding/Decoding**
- **DMA Subsystem including**
  - **16/32 channel chaining DMA**

Peripheral Functions
- **Parallel and Serial Display Interface**
- **Fast USB slave interface/ Fast IrDA**
- **SPI slave/master**
- **MMC/SD-Card support**
- **Keypad Interface**
- **FLASH Memory Interface**
- **Pseudo SRAM support**
- **13/26 MHz clock detection**
- **1.8V and 3.0V, 64 kbps SIM Interface**
- **Universal System Connector Interface**
- **Baseband Converter Interface**
- **Data Services Interface**

Control of Radio Subsystem
Three independent programmable backlight outputs
Real Time Clock with Alarm
Programmable Power and Clock Management
Slow Clocking Scheme for Low Idle Mode Current
Power Down modes
On-chip support for GSM Data Services up to 14.4kbits/sec, Class 12 GPRS, HSCSD
JTAG Interface for Test and In-Circuit Emulation
1.8V Typical Operating Voltage
Operating Voltage Range 1.7V - 1.9V
Independent I/O and Memory Voltages
160-Ball LFBGA (mini-BGA) package

APPLICATIONS

GSM850/900/DCS1800/PCS1900 Smartphone and Wireless PDA/Handheld Computers
GSM Phase 2 & GPRS Compliant
Full support for Java™, M-Services, and Multimedia Messaging Services (MMS)

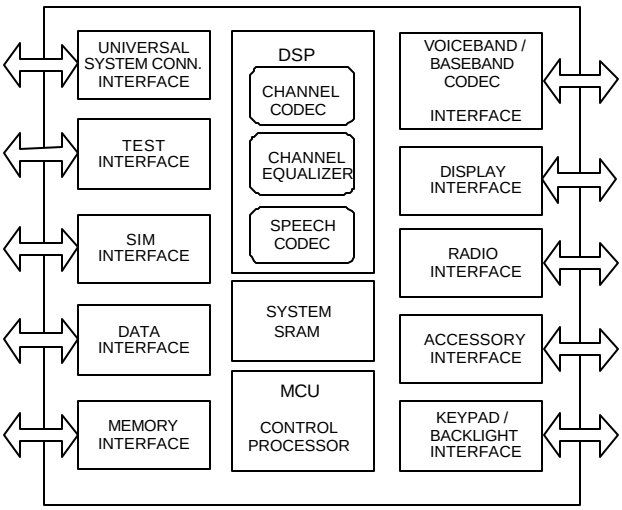

FIGURE 1. AD6528 FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD6528 is the third device in the Analog Devices AD20msp430 series of SoftFone® GSM Baseband Processors. The AD6528 is intended for use in feature-rich Smartphone and Wireless PDA/handheld computer applications with GSM/GPRS connectivity. It is designed to interface easily to an application processor in such systems.

The AD6528 integrates full rate, enhanced full rate and half rate speech codecs as well as a full range of data services including circuit-switched 14.4kb/s, GPRS to Class 12, and HSCSD. In addition, it supports A5/1 and A5/2 encryption algorithms as well as operation in non-encrypted mode.

The highly programmable architecture and sophisticated internal communication channels of the AD6528 offer maximum flexibility to system designers. It can adapt to tighter requirements led by changes in standards and multi-standard handset implementation.

A complete data sheet is available under Non-Disclosure Agreement to pre-qualified developers of GSM/GPRS terminal equipment. Contact your local Analog Devices Sales Office.

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