a

12-Bit, 65 MSPS IF to Base Band Diversity Receiver

Preliminary Technical Data AD6652

FEATURES

Integrated Dual Channel ADC
- Sample rates up to 65 MSPS
- IF sampling frequencies to 200 MHz
- SNR=70 dB (to Nyquist), SFDR 90 dB (to Nyquist)
- Power-Down to <2mW
- Internal Voltage Reference
- Internal Sample & Hold Analog Input
- Flexible Analog Input (1 to 2 V p-p)
- Differential or Single-Ended Analog Input
- Clock Duty Cycle Stabilizer
- -70 dB Channel-to-Channel Crosstalk

Quad-Channel Receive Signal Processor (RSP)
- Crossbar Switched Receive Processor Inputs
- Digital Re-sampling for non-Integer Decimation rates
- Programmable Decimating FIR Filters
- Flexible Control for Multi-Carrier and Phased Array
- Individual Channel Power-Down Functions to <1mW
- User Configurable Built in Self Test (BIST) capability
- JTAG Boundary Scan
- +3.0V Analog, +3.3V I/O, +2.5 V CMOS Digital Core

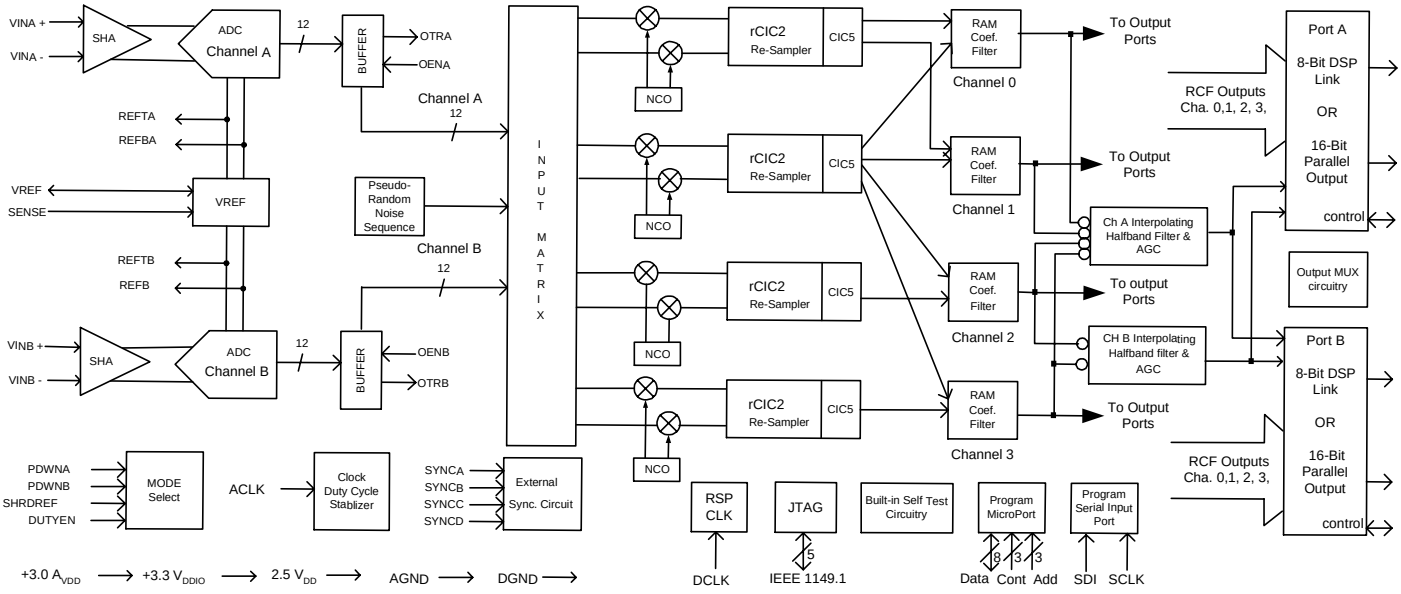
APPLICATIONS

Communications
- Diversity Radios Systems
- Multi-mode Digital Receivers:
- GSM, PHS, AMPS, UMTS, WCDMA, CDMA-ONE,
- IS95, IS136, CDMA2000, EDGE, IMT-2000
- Smart Antenna Systems
- General Purpose Software Radios

Broadband Data Applications

Instrumentation and Test Equipment

Dual-Channel 12-bit A/D Front End **4-Channel Receive Signal Processor**



FUNCTIONAL BLOCK DIAGRAM

REV. PrA

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PRODUCT DESCRIPTION

The AD6652 is a mixed-signal IF to base band receiver consisting of dual 12-bit 65 MSPS ADCs and a quad channel multi-mode digital Receive Signal Processor (RSP). The AD6652 is designed to support communications applications where low cost, small size, and versatility are desired. The AD6652 is also suitable for other applications in imaging, medical ultrasound, instrumentation, and test equipment.

The multi-stage differential pipelined architecture ADCs feature high performance sample-and-hold amplifiers with an integrated voltage reference. ADC data outputs are directly tied to the receiver input matrix. Over-range bits are available to alert the user to ADC clipping.

The digital receiver has four reconfigurable channels and provides extraordinary processing flexibility. The receiver input matrix feeds the ADC outputs to any or all of the four receive processing channels. Each receive-channel has five cascaded signal processing stages: a 32-bit frequency translator (numerically controlled oscillator (NCO)), two fixed-coefficient decimating filters (CIC), a programmable RAM coefficient decimating FIR filter (RCF) and an interpolating Halfband filter/AGC stage. Following the CIC filters, a channel or all channels may be configured to use any or all of the RCF filters. This permits the processing power of four 160-tap RCF FIR filters to be combined or used individually.

After FIR filtering the four channels are routed to two 16-bit output ports, and to two half-band interpolation stages where up to four channels may be combined (interleaved), interpolated and AGC (automatic gain control) applied. The outputs from the two AGC stages are also routed to both output ports. Each output port has a 16-bit parallel output and an 8-bit Link port to permit seamless data interface with DSP devices (such as the TigerSHARC™). A multiplexer for each port selects one of six data sources to appear on the device outputs pins.

The AD6652 is part of Analog Devices' SoftCell™ multi-mode and multi-carrier transceiver chipset. The SoftCell™ receiver digitizes a wide spectrum of IF frequencies and then down-converts the desired signals to base band using individual channel NCOs. AD6652 user-configurable digital filters remove any undesired base band components and the data are then passed on to an external DSP where demodulation and other signal processing is performed to complete the information retrieval task. Each receive channel is independently configured and provides simultaneous reception of the carrier it is tuned to. This IF sampling architecture greatly reduces component cost and complexity compared with analog techniques or less integrated digital methods.

High dynamic range decimation filters offer a wide range of decimation rates. The RAM-based architecture allows easy reconfiguration for multi-mode applications. The decimating filters remove unwanted signals and noise from the channel of interest. When the channel occupies less bandwidth than the input signal, this rejection of out-of-band noise is called "processing gain". By using large decimation factors, this "processing gain" can improve the SNR of the ADC by 30 dB or more. In addition, the programmable RAM Coefficient filter allows anti-aliasing, matched filtering, and static equalization functions to be combined in a single, cost-effective filter.

Flexible power-down options allow significant power savings when desired. The ADC stage can be powered-down to dissipate approximately 2mW while any of the receive processing channels can be individually or collectively powered-down. Total chip power-down results in less than 3mW power dissipation.

PRODUCT HIGHLIGHTS

1. Integrated Dual 12-bit 65 MSPS ADC.
2. Four Independent Digital Filtering Channels.
3. AD6652 operates from a 3V analog supply, 2.5V digital core supply, and a 3.3V I/O supply
4. Proprietary SHA input maintains excellent performance for input frequencies up to 200MHz, and can be configured for single-ended or differential operation.
5. Crossbar-Switched Receive Processor Input Ports
6. Fractional Digital Re-sampling permits non-integer relationships between the ADC clock and the digital output data rate.
7. Power-down to less than 3mW.
8. ADC over-range output bits.
9. 32-bit NCOs with selectable amplitude and phase dithering for better than -100dBc spurious performance.
10. CIC filters with user programmable decimation and interpolation factors
11. 160-tap programmable RAM coefficient filter.
12. Dual 16-bit Parallel output ports and dual 8-bit Link ports.
13. 8-bit Microport and 2-wire serial port for register programming, register read-back and coefficient memory programming.

CONTENTS

RECOMMENDED OPERATING CONDITIONS

Parameter	Temp	Test Level	AD6652AS MIN	Typ	Max	Units
AVDD			TBD	3.0	TBD	V
VDD		IV	2.375	2.5	2.675	V
VDDIO		IV	3.0	3.3	3.6	V
$T_{AMBIENT}$		IV	-40	+25	+70	°C

ADC DC SPECIFICATIONS (AVDD = 3.0, VDD = +2.5V, VDDIO = +3.3V, 65 MSPS, 2V p-p Differential Input, 1.0V internal reference, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	Min	AD6652 Typ	Max	Units
RESOLUTION	Full	VI	12			Bits
INTERNAL VOLTAGE REFERENCE						
Output Voltage Error (1V Mode)	Full	VI		±5	±35	mV
Load Regulation @ 1.0 mA	Full	V		.8		mV
Output Voltage Error (0.5V Mode)	Full	V		±2.5		mV
Load Regulation @ 0.5 mA	Full	V		0.1		mV
INPUT REFERRED NOISE						
VREF= 0.5V	25°C	V		0.54		LSBrms
VREF= 1.0V	25°C	V		0.27		LSBrms
ANALOG INPUT						
Input Span, VREF = 0.5V	Full	IV		1		Vp-p
Input Span, VREF = 1.0V	Full	IV		2		Vp-p
Input Capacitance	Full	V		7		pF
REFERENCE INPUT RESISTANCE	Full	V		7		kΩ

NOTES
Specifications subject to change without notice

ADC SWITCHING SPECIFICATIONS (AVDD = 3.0, VDD = +2.5V, VDDIO = +3.3V, 65 MSPS, 2V p-p Differential Input, 1.0V internal reference, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	Min	AD6652 Typ	Max	Units
SWITCHING PERFORMANCE						
Max Conversion Rate	Full	VI	65			MSPS
Min Conversion Rate	Full	V			1	MSPS
ACLK Period	Full	V	15.4			ns
ACLK Pulse width High[1]	Full	V	6.2			ns
ACLK Pulse width Low[1]	Full	V	6.2			ns
DATA OUTPUT PARAMETERS						
Wake-Up Time[2]	Full	V		2.5		ms
OUT-OF-RANGE RECOVERY TIME	Full	V		2		Cycles

Notes
[1]Duty Cycle Stabilizer enabled.
[2]Wake-Up Time is dependent on value of decoupling capacitors, typical values shown with 0.1µF and 10µF capacitors on REFT and REFB.
Specifications subject to change without notice

ADC AC SPECIFICATIONS (AVDD = 3.0, VDD = +2.5V, VDDIO = +3.3V, 65 MSPS, 2Vp-p Differential Input, 1.0V internal reference, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD6652 Min	Typ	Max	Units
TBD						
TBD						
TBD						

NOTES

1

2

Specifications subject to change without notice

ELECTRICAL CHARACTERISTICS (AVDD = 3.0, VDD = +2.5V, VDDIO = +3.3V, 65 MSPS, 2Vp-p Differential Input, 1.0V internal reference, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD6652 Min	AD6652 Typ	AD6652 Max	Units
LOGIC INPUTS (5V TOLERANT)						
Logic Compatibility	Full	IV		3.3V CMOS		
Logic "1" Voltage	Full	IV	2.0		5.0	V
Logic "0" Voltage	Full	IV	-0.3		0.8	V
Logic "1" Current	Full	IV		1	10	µA
Logic "0" Current	Full	IV		1	10	µA
Logic "1" Current (inputs with pull-down)	Full	IV				
Logic "0" Current (inputs with pull-up)	Full	IV				
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS						
Logic Compatibility	Full	IV		3.3V CMOS/TTL		
Logic "1" Voltage (I_{OH}=0.25mA)	Full	IV	2.4	VDD-0.2		V
Logic "0" Voltage (I_{OL}=0.25mA)	Full	IV		0.2	0.4	V
SUPPLY CURRENTS						
CDMA (61.44 MHz) example[1]						
I_{AVDD}	+25°C	V		TBD		mA
I_{VDD}	+25°C	V		TBD		mA
I_{VDDIO}	+25°C	V		TBD		mA
WCDMA (61.44 MHz) example[1]	+25°C	V				
I_{AVDD}	+25°C	V		TBD		mA
I_{VDD}	+25°C	V		TBD		mA
I_{VDDIO}	+25°C	V		TBD		mA
WCDMA (61.44 MHz) example[2]						
I_{AVDD}	+25°C	V		TBD		mA
I_{VDD}	+25°C	V		TBD		mA
I_{VDDIO}	+25°C	V		TBD		mA
GSM (64 MHz) example, 4 individual channels						
I_{AVDD}	+25°C	V		TBD		mA
I_{VDD}	+25°C	V		TBD		mA
I_{VDDIO}	+25°C	V		TBD		mA
TOTAL POWER DISSIPATION						
CDMA (61.44 MHz)[1]				TBD		mW
WCDMA (61.44 MHz)[1]				TBD		mW
WCDMA (61.44 MHz)[2]				TBD		mW
GSM, 64 MHz, four individual channels				TBD		mW
ADC Powered-down and RSP in Sleep Mode				3		mW

NOTES

[1]All signal processing stages and all RSP channels active

[2]Same as note [1] except two of four RSP channels are in Sleep Mode

Specifications subject to change without notice

GENERAL TIMING CHARACTERISTICS[1, 2] (AVDD = 3.0, VDD = +2.5V, VDDIO = +3.3V, 65 MSPS,2Vp-p Differential Input, 1.0V internal reference, unless otherwise noted)

Parameter (Conditions)		Temp	Test Level	AD6652 Min	Typ	Max	Units
DCLK TIMING REQUIREMENTS:							
t_{DCLK}	DCLK Period	Full	I	12.5			ns
t_{DCLKL}	DCLK Width Low	Full	IV	5.6	0.5 x t_{CLK}		ns
t_{DCLKH}	DCLK Width High	Full	IV	5.6	0.5 x t_{CLK}		ns
/RESET TIMING REQUIREMENTS:							
t_{RESL}	/RESET Width Low	Full	I	30.0			ns
Input Wideband Data Timing Requirements:							
t_{SI}	Input to ↑DCLK Setup Time	Full	IV	2.0			ns
t_{HI}	Input to ↑DCLK Hold Time	Full	IV	1.0			ns
SYNC TIMING REQUIREMENTS:							
t_{SS}	SYNC(A,B,C,D) to ↑DCLK Setup Time	Full	IV	2.0			ns
t_{HS}	SYNC(A,B,C,D) to ↑DCLK Hold Time	Full	IV	1.0			ns
SERIAL PORT CONTROL TIMING REQUIREMENTS: SWITCHING CHARACTERISTICS[2]							
t_{SCLK}	SCLK Period	Full	IV	16			ns
t_{SCLKL}	SCLK low time	Full	IV	3.0			ns
t_{SCLKH}	SCLK high time	Full	IV	3.0			ns
INPUT CHARACTERISTICS:							
t_{SSI}	SDIN to ↓SCLK Setup Time	Full	IV	1.0			ns
t_{HSI}	SDIN to ↓SCLK Hold Time	Full	IV	1.0			ns
PARALLEL PORT TIMING REQUIREMENTS (MASTER MODE): SWITCHING CHARACTERISTICS:[3]							
$t_{DPOCLKL}$	↓DCLK to ↑PCLK Delay (Divide by 1)	Full	IV	6.5		10.5	ns
$t_{DPOCLKLL}$	↓DCLK to ↑PCLK Delay (Divide by 2, 4, or 8)	Full	IV	8.3		14.6	ns
t_{DPREQ}	↑DCLK to ↑PxREQ Delay					1.0	
t_{DPP}	↑DCLK to Px[15:0] Delay					0.0	
INPUT CHARACTERISTICS:							
t_{SPA}	PxACK to ↓PCLK Setup Time			7.0			
t_{HPA}	PxACK to ↓PCLK Hold Time			-3.0			
PARALLEL PORT TIMING REQUIREMENTS (SLAVE MODE) SWITCHING CHARACTERISTICS: [3]							
t_{POCLK}	PCLK Period	Full	I	12.5			ns
t_{POCLKL}	PCLK Low Period (when PCLK divisor = 1)	Full	IV	2.0	0.5* t_{POCLK}		ns
t_{POCLKH}	PCLK High Period (when PCLK divisor = 1)	Full	IV	2.0	0.5* t_{POCLK}		ns
t_{DPREQ}	↑DCLK to ↑PxREQ Delay					10.0	
t_{DPP}	↑DCLK to Px[15:0] Delay					11.0	
INPUT CHARACTERISTICS:							
t_{SPA}	PxACK to ↓PCLK Setup Time			1.0			
t_{HPA}	PxACK to ↓PCLK Hold Time			1.0			
LINK PORT TIMING REQUIREMENTS SWITCHING CHARACTERISTICS: [3]		Temp	Test Level	AD6652 Min	Typ	Max	Units
t_{RDLCLK}	↑PCLK to ↑LxCLKOUT Delay	Full	IV			2.5	ns
t_{FDLCLK}	↓PCLK to ↓LxCLKOUT Delay	Full	IV			0	ns
$t_{RLCLKDAT}$	↑LCLKOUT to Lx[7:0] Delay	Full	IV	0		2.9	ns
$t_{FLCLKDAT}$	↓LCLKOUT to Lx[7:0] Delay	Full	IV	0		2.2	ns

NOTES

[1]All Timing Specifications valid over VDD range of 2.25V to 2.75V and VDDIO range of 3.0V to 3.6V.
[2](C_{LOAD}=40pF on all outputs unless otherwise specified)
[3]The timing parameters for Px[15:0], PxREQ, PxACK, LxCLKOUT, Lx[7:0] apply for port A and B. (x stands for A or B)
Specifications subject to change without notice

MICROPROCESSOR PORT TIMING CHARACTERISTICS[1, 2]

AVDD = 3.0, VDD = +2.5V, VDDIO = +3.3V, 65 MSPS, 2Vp-p Differential Input, 1.0V internal reference, unless otherwise noted)

MICROPROCESSOR PORT, MODE INM (MODE=0)		Temp	Test Level	AD6652 Min	AD6652 Typ	AD6652 Max	Units
MODE INM WRITE TIMING:							
t_{SC}	Control[3] to ↑DCLK Setup Time	Full	IV	2.0			ns
t_{HC}	Control[3] to ↑DCLK Hold Time	Full	IV	2.5			ns
t_{HWR}	/WR(RW) to RDY(/DTACK) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data to /WR(RW) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RDY(/DTACK) Hold Time	Full	IV	5.0			ns
t_{DRDY}	/WR(RW) to RDY(/DTACK) Delay	Full	IV	8.0			ns
t_{ACC}	/WR(RW) to RDY(/DTACK) High Delay	Full	IV	$4*t_{CLK}$	$5*t_{CLK}$	$9*t_{CLK}$	ns
MODE INM READ TIMING:							
t_{SC}	Control[3] to ↑DCLK Setup Time	Full	IV	5.0			ns
t_{HC}	Control[3] to ↑DCLK Hold Time	Full	IV	2.0			ns
t_{SAM}	Address to /RD(/DS) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DRDY}	/RD(/DS) to RDY(/DTACK) Delay	Full	IV	8.0			ns
t_{ACC}	/RD(/DS) to RDY(/DTACK) High Delay	Full	IV	$8*t_{CLK}$	$10*t_{CLK}$	$13*t_{CLK}$	ns
MICROPROCESSOR PORT, MODE MNM (MODE=1)		**Temp**	**Test Level**	**AD6652 Min**	**AD6652 Typ**	**AD6652 Max**	**Units**
MODE MNM WRITE TIMING:							
t_{SC}	Control[3] to ↑DCLK Setup Time	Full	IV	2.0			ns
t_{HC}	Control[3] to ↑DCLK Hold Time	Full	IV	2.5			ns
t_{HDS}	/DS(/RD) to /DTACK(RDY) Hold Time	Full	IV	8.0			ns
t_{HRW}	RW(/WR) to /DTACK(RDY) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data To RW(/WR) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RW(/WR) Hold Time	Full	IV	5.0			ns
t_{DDTACK}	/DS(/RD) to /DTACK(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	RW(/WR) to /DTACK(RDY) Low Delay	Full	IV	$4*t_{CLK}$	$5*t_{CLK}$	$9*t_{CLK}$	ns
MODE MNM READ TIMING:							
t_{SC}	Control[3] to ↑DCLK Setup Time	Full	IV	5.0			ns
t_{HC}	Control[3] to ↑DCLK Hold Time	Full	IV	2.0			ns
t_{HDS}	/DS(/RD) to /DTACK(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address to /DS(/RD) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DDTACK}	/DS(/RD) to /DTACK(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	/DS(/RD) to /DTACK(RDY) Low Delay	Full	IV	$8*t_{CLK}$	$10*t_{CLK}$	$13*t_{CLK}$	ns

[1]All Timing Specifications valid over VDD range of 2.25V to 2.75V and VDDIO range of 3.0V to 3.6V.
[2](C_{LOAD}=40pF on all outputs unless otherwise specified)
[3]Specification pertains to control signals: R/W, (/WR), /DS, (/RD), /CS

Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS

AVDD…….……..…….. –0.3 to +3.9V
VDD…….…… –0.3 to +2.75V
VDDIO……..…….….–0.3 to +3.6V
VINA, VINB…….-0.3 to AVDD +0.3V
Digital Input Voltage…….-0.3 to AVDD +0.3V
Output Voltage Swing…….…..-0.3V to VDDIO +0.3V
Load Capacitance…….……..…….200pF
Operating Temperature Range…….-40°C to +70°C
Junction Temperature Under Bias…..…..……+125°C
Storage Temperature Range…….....-65°C to +150°C
Lead Temperature (5 sec)……..…….…..+280°C

Notes

[1]Stresses greater than those listed above may cause permanent damage to the device These are stress ratings only; functional operation of the devices at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

256 BGA:
θ_{JA}==xx°C /Watt, no airflow
θ_{JA}==xx°C /Watt, 200-lfpm airflow
θ_{JA}==xx°C /Watt, 400-lfpm airflow
Thermal measurements made in the horizontal position on a 4-layer board.

EXPLANATION OF TEST LEVELS

I 100% Production Tested.
II 100% Production Tested at 25°C, and Sampled Tested at Specified Temperatures.
III Sample Tested Only
IV Parameter Guaranteed by Design and Analysis
V Parameter is Typical Value Only
VI 100% Production Tested at 25°C, and Sampled Tested at Temperature Extremes

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6652XBC[1]	-40°C to +70°C (Ambient)	256-Lead BGA (Ball Grid Array)	256 BGA
AD6652BBC	-40°C to +70°C (Ambient)	256-Lead BGA (Ball Grid Array)	256BGA
AD6652BC/PCB		Evaluation Board with AD6652 and Software	

ESD SENSITIVITY

The AD6652 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6652 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Figure 1: PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	DGND	PA7_ LA7	A2	PA6_ LA6	D1	D3	/CS	/RESET	MODE	SYNCD	OTRB	PDWN B	AVDD	AVDD	AGND	AGND
B	TDO	PA4_ LA4	PACH0_ LACLK OUT	A0	/TRST	R/W (/WR)	D4	D6	SYNCC	SYNCA	/OENB	DUTYEN	AVDD	AVDD	AGND	AGND
C	PA9	PA3_ LA3	A1	/DS (RD)	D0	D2	D5	D7	/DTACK (RDY)	SYNCB	n.c.	n.c.	AVDD	AVDD	AGND	VIN+B
D	PA1_ LA1	PA2_ LA2	PACH1_ LACLK IN	VDD	VDD	VDD	VDD	VDDIO	VDDIO	VDDIO	VDDIO	VDDIO	AVDD	AVDD	AGND	VIN-B
E	PA8	PA5_ LA5	n.c.	VDD	VDD	VDD	VDD	VDDIO	VDDIO	VDDIO	VDDIO	VDDIO	AVDD	AVDD	AGND	AGND
F	PA0_ LA0	TCLK	PA10	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	AGND
G	PA12	PA11	PA13	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	REFB B	REFTB
H	PAREQ	PA15	PA14	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	SENSE
J	CHIP_ ID1	TDI	TMS	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	VREF
K	CHIP_ ID3	PAACK	CHIP_ ID0	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	REFB A	REFTA
L	PB6_ LB6	PB7_ LB7	SCLK	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	AGND
M	CHIP_ ID2	PB3_ LB3	PB4_ LB4	VDDIO	VDDIO	VDDIO	VDDIO	VDD	VDD	VDD	VDD	VDDIO	AVDD	AVDD	AGND	AGND
N	PAIQ	PBCH1_ LBCLK IN	PB2_ LB2	VDDIO	VDDIO	VDDIO	VDDIO	VDD	VDD	VDD	VDD	VDDIO	AVDD	AVDD	AGND	VIN-A
P	SDIN	PB0_ LB0	PB8	PB10	PB14	reserved VDDIO	PBACK	n.c.	n.c.	n.c.	OTRA	n.c.	AVDD	AVDD	AGND	VIN+A
R	PBIQ	PBCH0_ LBCLK OUT	PB1_ LB1	PB9	PB12	PB15	n.c.	n.c.	n.c.	n.c.	/OENA	PDWN A	AVDD	AVDD	AGND	AGND
T	DGND	PCLK	PB5_ LB5	PB11	PB13	PBREQ	n.c.	n.c.	n.c.	n.c.	DCLK	SHRD REF	AVDD	ACLK	AGND	AGND

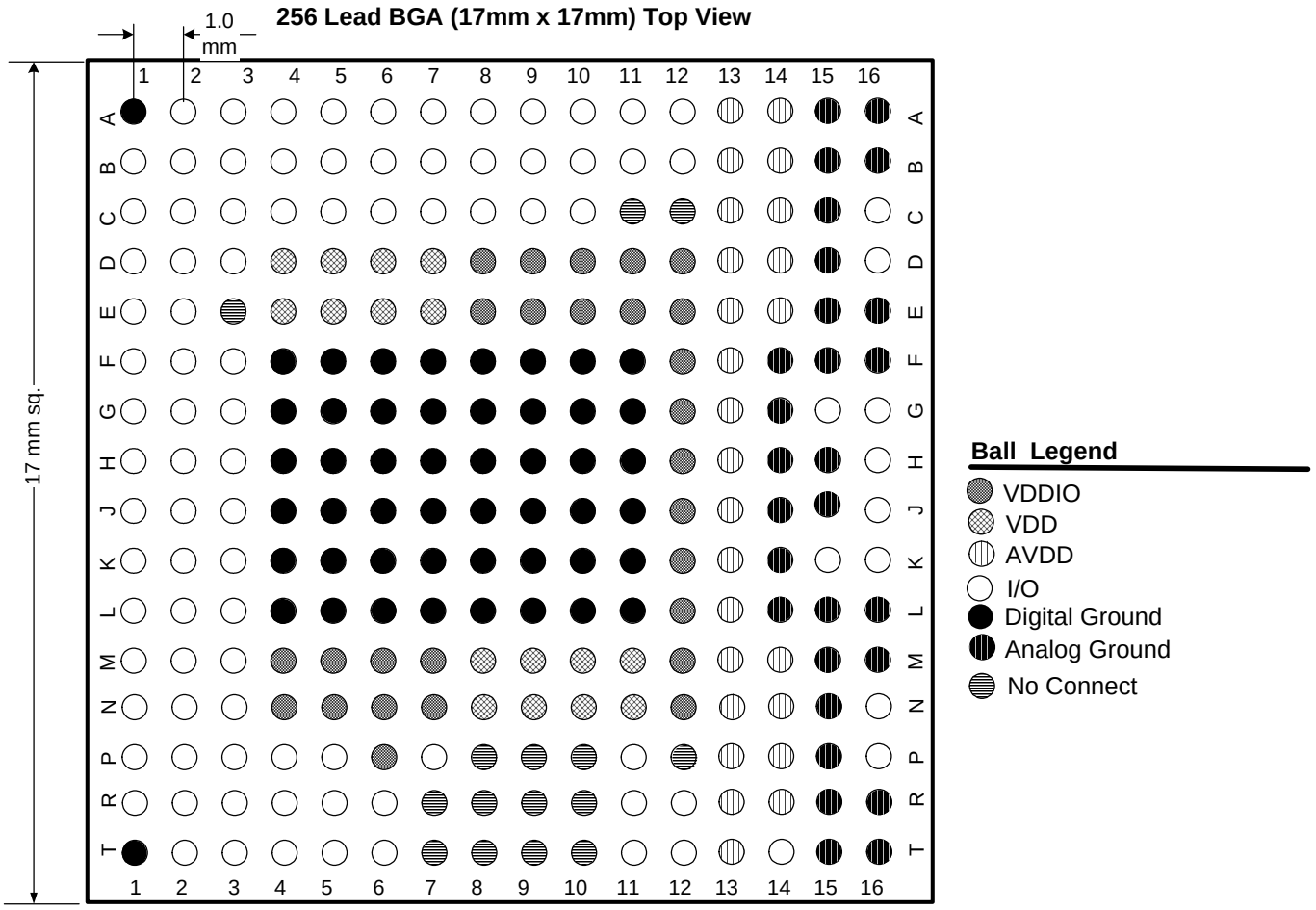


Figure 2. 17 x 17 Mini-BGA package showing power and signal ball assignments

TABLE 1: PIN NAME and FUNCTIONS

Name	Type	Function
POWER SUPPLY		
AVDD	P	3.0V Analog Supply, 25 pins
VDD	P	2.5V Digital Core Supply, 16 pins
VDDIO	P	3.3V Digital I/O Supply, 27 pins
DGND	G	Digital Ground, 50 pins
AGND	G	Analog Ground, 28 pins
n.c.	---	No Connect, 15 pins
ADC INPUTS		
VIN+A	I	Differential Analog Input Pin (+) for Channel A
VIN-A	I	Differential Analog Input Pin (-) for Channel A
VIN+B	I	Differential Analog Input Pin (+) for Channel B
VIN-B	I	Differential Analog Input Pin (-) for Channel B
VREF	I/O	Voltage Reference Input/Output
SENSE	I	Voltage Reference Mode Selection
ACLK	I	ADC Master Clock
DUTYEN	I	Duty Cycle Stabilizer (DCS) mode
PDWNA[1]	I	Power-Down Function (Active High)
PDWNB[1]	I	Power-Down Function (Active High)
/OENA	I	Output Enable for channel A (Active Low)
/OENB	I	Output Enable for channel A (Active Low)
SHRDREF	I	Shared Reference Control Bit (Low = Independent Mode, High = Shared Mode
ADC OUTPUTS		
OTRA	O	Out of Range Indicator for Channel A
OTRB	O	Out of Range Indicator for Channel B
REFTA	O	TOP Reference Voltage for Channel A
REFTB	O	TOP Reference Voltage for Channel B
REFBA	O	BOTTOM Reference Voltage for Channel A
REFBB	O	BOTTOM Reference Voltage for Channel B
RECEIVER INPUTS		
/RESET	I	Active Low Reset Pin
DCLK	I	Receive Signal Processor Master Clock
PCLK	I/O	Link/Parallel Port Clock
PACH1_LACLKIN[2]	I/O	Parallel Port A Channel Identification MSB output or Link Port A Data Ready. Function depends on value of bit 7 at 0x1B, output port control register.
PBCH1_LBCLKIN[2]	I/O	Parallel Port B Channel Identification MSB output or Link Port B Data Ready input. Function depends on value of bit 7 at 0x1D. output port control register.
SYNCA[3]	I	Hardware sync, connects to all four RSP channels
SYNCB[3]	I	Hardware sync, connects to all four RSP channels
SYNCC[3]	I	Hardware sync, connects to all four RSP channels
SYNCD[3]	I	Hardware sync, connects to all four RSP channels
/CS[3]	I	Chip Select (low active)
CHIP_ID[3:0][3]	I	Chip ID Selector, 4 pins

CONTROL		
PAACK	I	Parallel Port A Acknowledge
PAREQ	O	Parallel Port A Request
PBACK	I	Parallel Port B Acknowledge
PBREQ	O	Parallel Port B Request

MICROPORT CONTROL		
D[7:0]	I/O/T	Bi-directional Microport Data, eight pins
A[2:0]	I	MicroPort Address Bus, three pins
/DS(/RD)[4]	I	Active Low Data Strobe (Active Low Read) (pin function depends upon MODE. ( ) =Mode 0
/DTACK(RDY)[4,5]	O/T	Active Low Data Acknowledge (Microport Status Bit) (pin function depends upon MODE. ( ) =Mode 0
R/W (/WR)[4]	I	Read Write (Active Low Write) (pin function depends upon MODE. ( ) =Mode 0
MODE[4]	I	Mode select, Intel (logic 0) or Motorola (logic 1)
SERIAL PORT CONTROL		
SDIN[3]	I	Serial Port Control Data Input
SCLK[3]	I	Serial Port Control Clock
RECEIVER OUTPUTS		
PACH0_LACLKOUT[2]	O	Parallel Port A Channel Identification LSB output or Link Port A Clock output. Function depends on value of bit 7 at 0x1B, output port register.
PBCH0_LBCLKOUT[2]	O	Parallel Port B Channel Identification LSB output or Link Port B Clock output. Function depends on value of bit 7 at 0x1D, output port register.
PA [7:0]_LA[7:0]	O	Link Port A Output Data or Parallel Data Port A LSBs (depends on value of bit 7 at 0x1B, output port register), eight pins
PB [7:0]_LB[7:0]	O	Link Port B Output Data or Parallel Data Port B LSBs (depends on value of bit 7 at 0x1D, output port register), eight pins
PA[15:8]	O	Parallel Data Port A, bits 15:8, eight pins
PB[15:8]	O	Parallel Data Port B, bits 15:8, eight pins
PAIQ	O	Parallel Port A I/Q Data Indicator
PBIQ	O	Parallel Port B I/Q Data Indicator
JTAG & BIST		
/TRST[5]	I	Test Reset Pin
TCLK[3]	I	Test Clock Input
TMS[5]	I	Test Mode Select Input
TDO	O/T	Test Data Output
TDI[5]	I	Test Data input

[1]PDWNA and PDWNB must be the same logic level, both logic high or both logic low
[2]PACH0 and PACH1 form a 2-bit output word in the parallel output mode that identifies the processing channel (0,1,2 or 3) whose data appears on Port A parallel outputs. Likewise, PBCH0 and PBCH1 identify the channel for Port B.
[3]Pins with a Pull-Down resistor of nominal 70K ohms
[4]Mode 0 = Intel Non-Multiplexed (IMN) and Mode 1= Motorola Non-Multiplexed (MNM)

[5] Pins with a Pull-Up resistor of nominal 70K ohms

DEFINITIONS OF A/D SPECIFICATIONS

Integral Nonlinearity (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, no missing codes)
An ideal A/D converter exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

Zero Error
The major carry transition, 011111111111 to 100000000000, should occur when analog input voltage is ½ LSB below VIN- = VIN+. Zero error is defined as the voltage deviation of the actual transition from the ideal transition.

Gain Error
The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Temperature Drift
The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at TMIN or TMAX.

Power Supply Rejection Ratio (PSRR)
The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Aperture Jitter
Aperture jitter is the variation in aperture delay for successive samples and can be manifested as noise on the input to the A/D converter.

Aperture Delay
Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

Signal-To-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise and Distortion (S/N+D, SINAD) Ratio
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Effective Number Of Bits (ENOB)
For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,
N = (SINAD - 1.76)/6.02 it is possible to obtain a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Spurious Free Dynamic Range (SFDR)
SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

Clock Pulse Width And Duty Cycle
Pulse width high is the minimum amount of time that the clock pulse should be left in the logic 1 state to achieve rated performance: pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Minimum Conversion Rate
The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The clock rate at which parametric testing is performed.

Output Propagation Delay
The delay between the clock logic threshold and the time when all bits are within valid logic levels.

Out-Of-Range Recovery Time
Out-of-range recovery time is the time it takes for the A/D converter to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Crosstalk
Coupling onto one channel being driver by a low level (-40dBFS) signal when the adjacent interfering channel is driven by a full-scale signal.

Nyquist Sampling (oversampling)
Occurs when the frequency components of the analog input signal are confined between dc and the Sample Rate/2. Requires the analog input frequency to be sampled at least 2 samples per cycle.

IF Sampling (undersampling)
Due to the effects of aliasing, an ADC is not necessarily limited to Nyquist sampling. Frequencies above Nyquist will be aliased and appear in the first Nyquist zone (dc to Sample Rate/2). Care must be taken to limit the bandwidth of the sampled signal so that it does not overlap Nyquist zones and alias onto itself. *IF Sampling* performance is limited by the bandwidth of the input SHA (sample and hold amplifier) and clock "jitter". The sample rate of the analog input frequency will be less than 2 samples per cycle.

TIMING DIAGRAMS

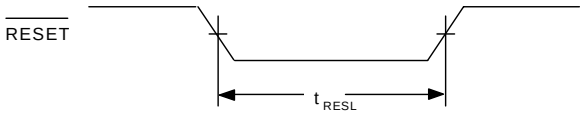


Figure 3. Reset Timing Requirements

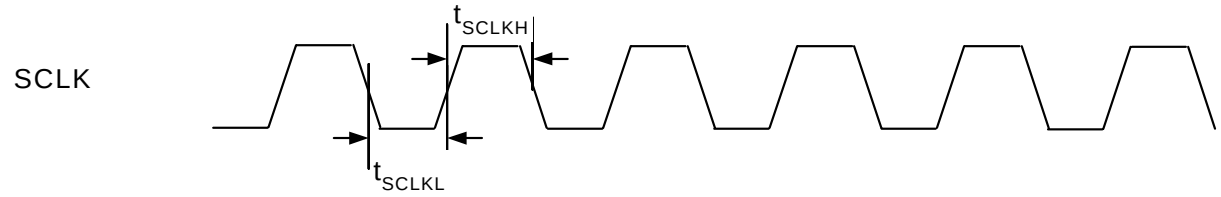


Figure 4. SCLK Switching Characteristics

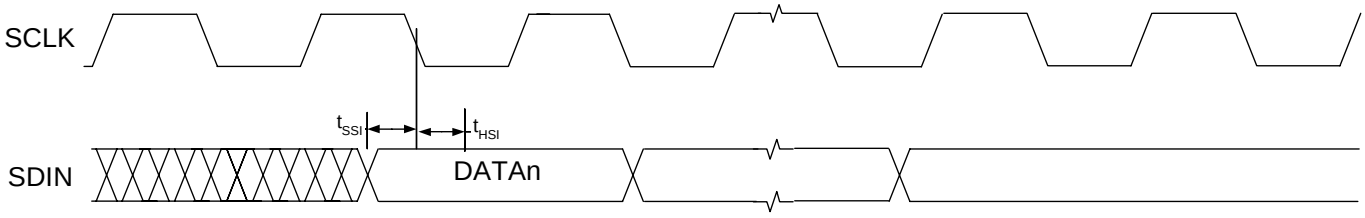


Figure 5. Serial Port Input Timing Characteristics

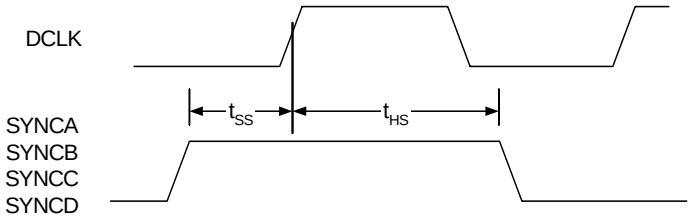


Figure 6. SYNC Timing Inputs

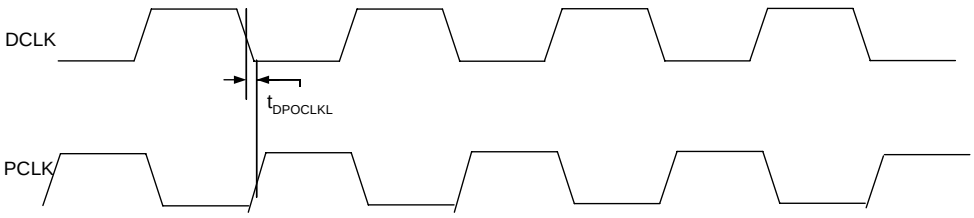


Figure 7. PCLK to DCLK Switching Characteristics Divide by 1

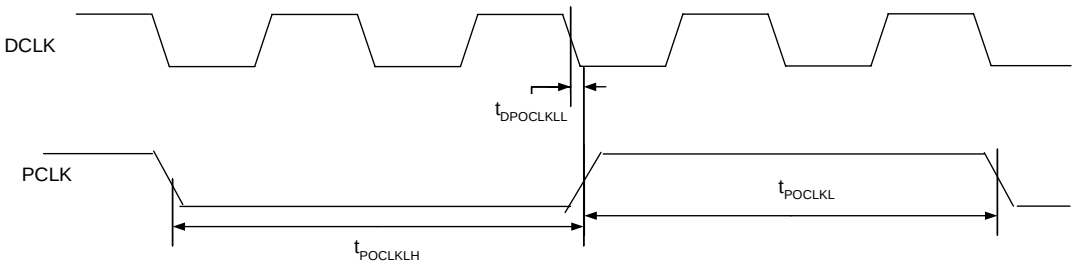


Figure 8. PCLK to DCLK Switching Characteristics Divide by 2,4, or 8

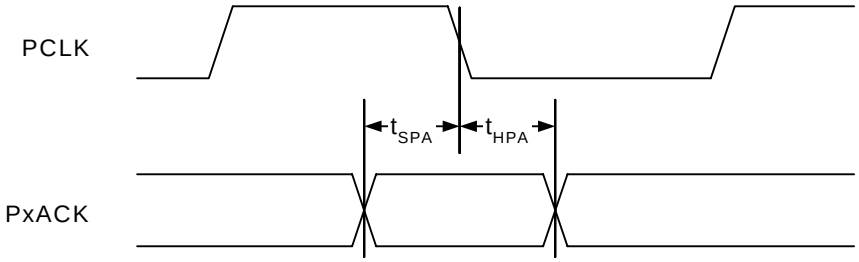


Figure 9. Master Mode PxACK to PCLK Setup and Hold Characteristics

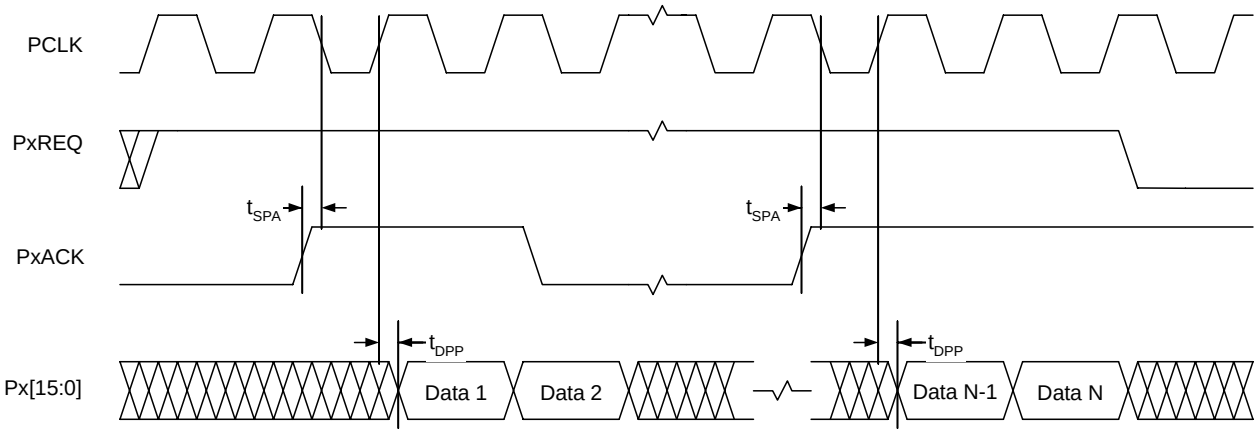


Figure 10. Master Mode PxACK to PCLK Switching Characteristics

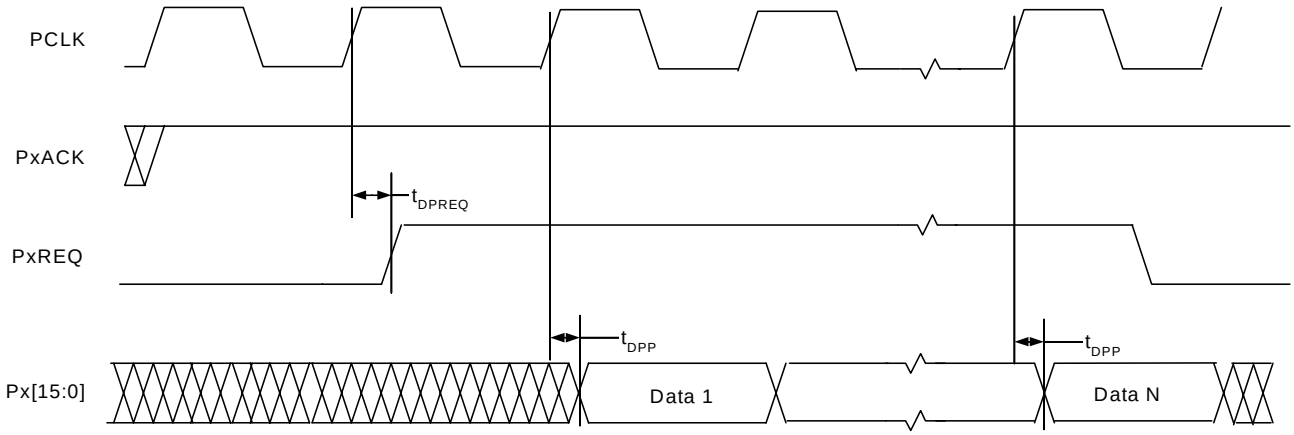


Figure 11. Master Mode PxREQ to PCLK Switching Characteristics

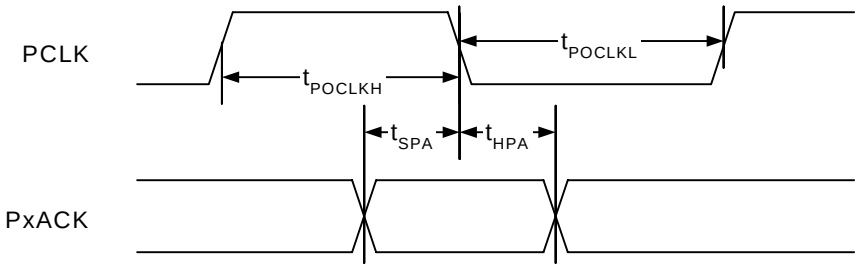


Figure 12. Slave Mode PxACK to PCLK Setup and Hold Characteristics

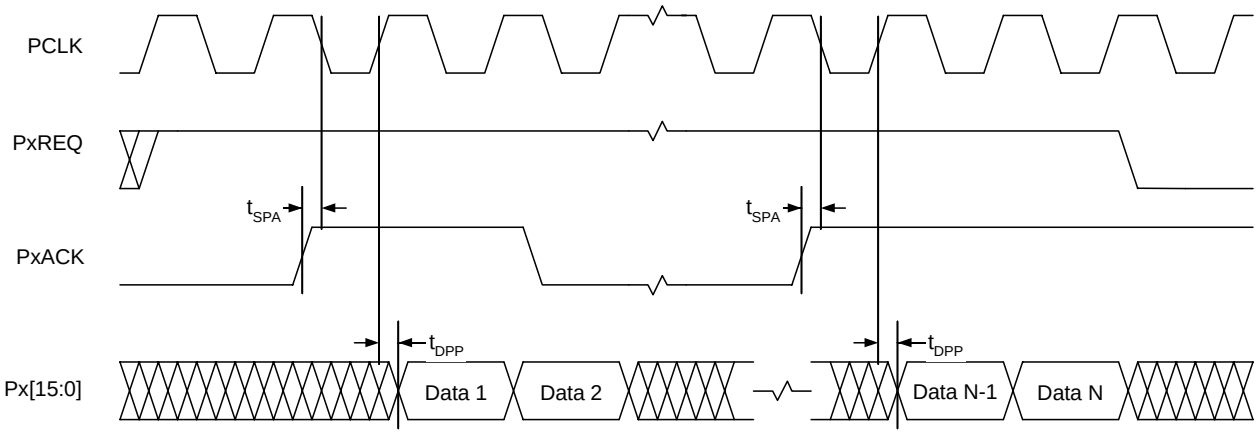


Figure 13. Slave Mode PxACK to PCLK Switching Characteristics

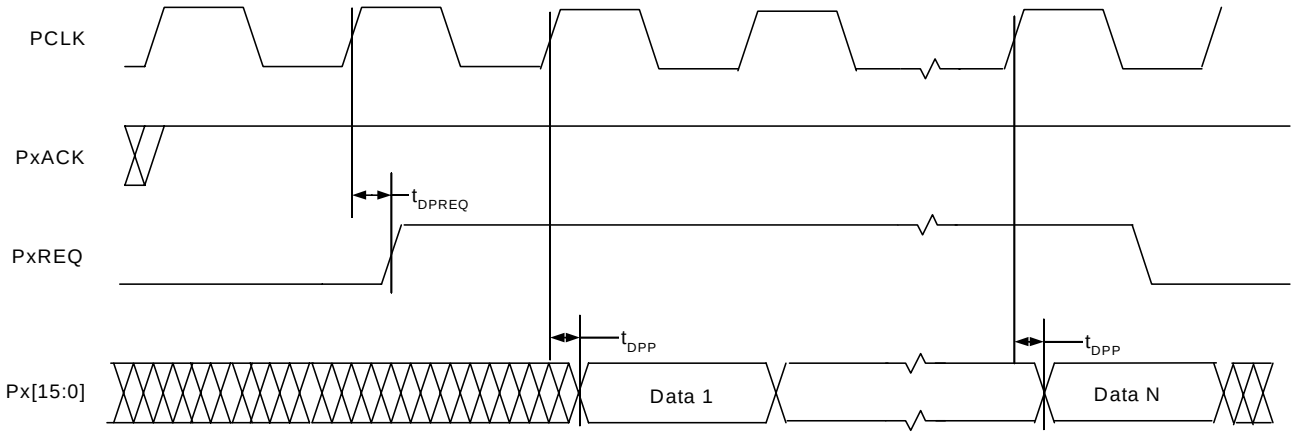


Figure 14. Slave Mode PxREQ to PCLK Switching Characteristics

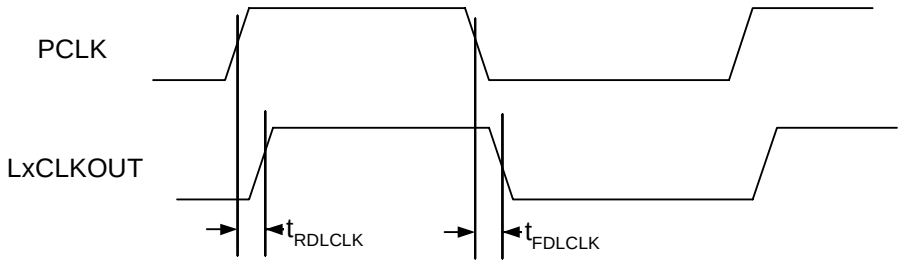


Figure 15. LxCLKOUT to PCLK Switching Characteristics

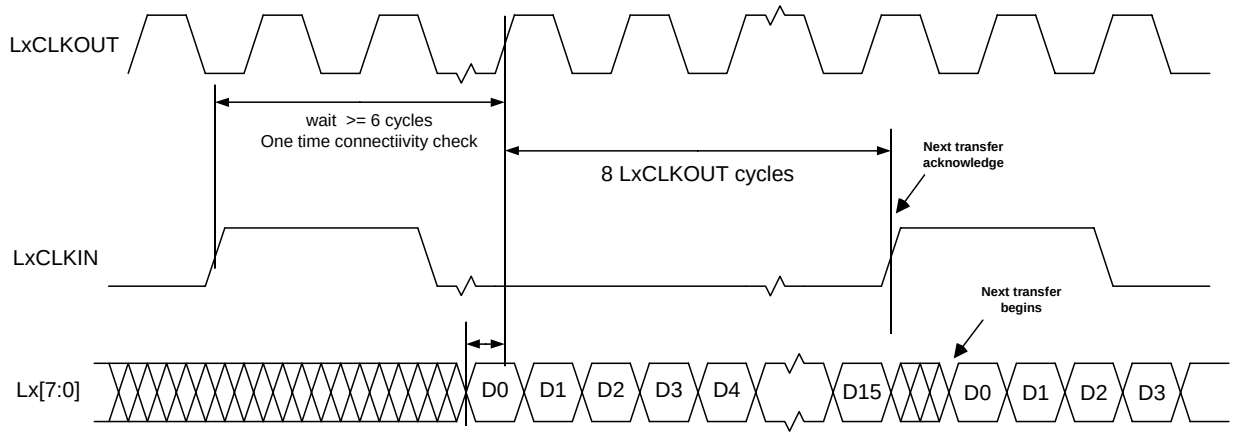


Figure 16. LxCLKIN to LxCLKOUT Data Switching Characteristics

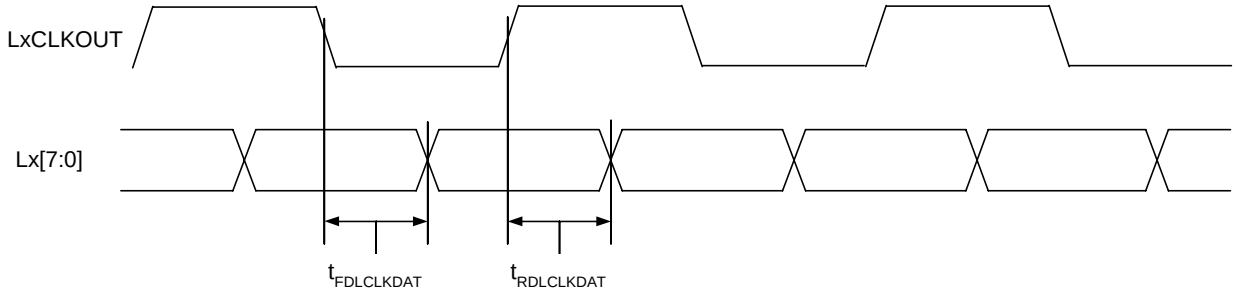
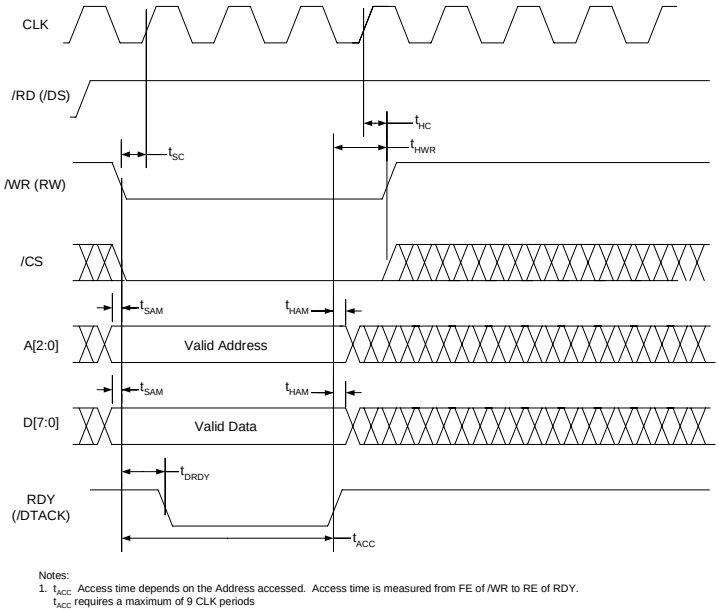


Figure 17. LxCLKOUT to Lx[7:0]Data Switching Characteristics

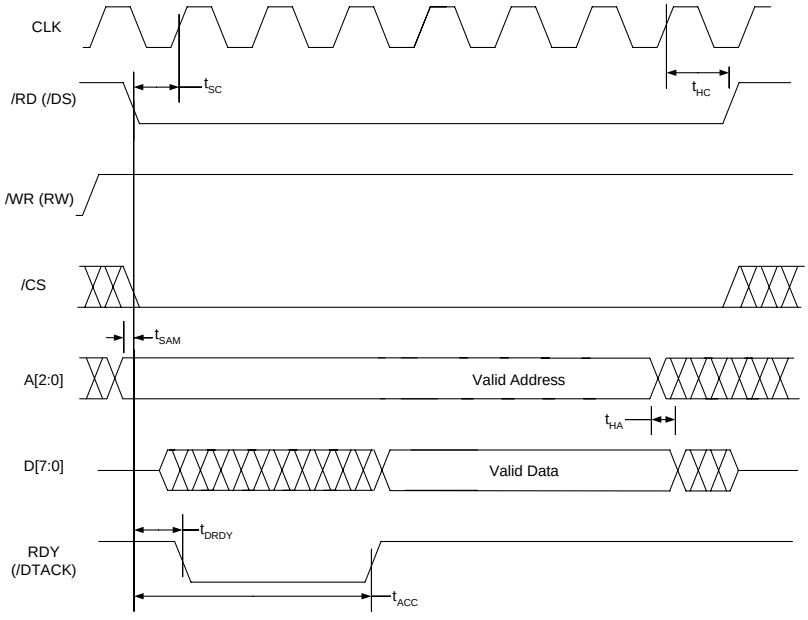
AD6652

TIMING DIAGRAMS – INM Microport Mode



Notes:
1. t_{ACC} Access time depends on the Address accessed. Access time is measured from FE of /WR to RE of RDY.
   t_{ACC} requires a maximum of 9 CLK periods

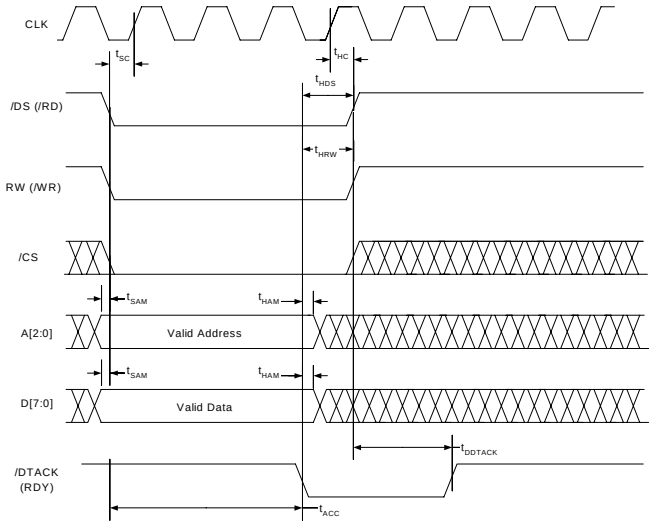
Figure 18. INM Microport Write Timing Requirements.



Notes:
1. t_{ACC} Access time depends on the Address accessed. Access time is measured from FE of /WR to RE of RDY.
   t_{ACC} Requires a maximum of 13 CLK periods

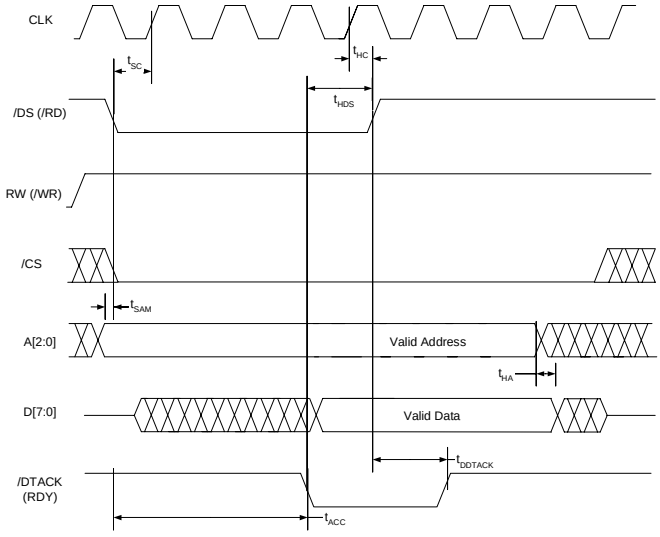
Figure 19. INM Microport Read Timing Requirements.

TIMING DIAGRAMS – MNM Microport Mode



Notes:
1. t_{ACC} Access time depends on the Address accessed. Access time is measured from the FE of /DS to the FE of /DTACK. t_{ACC} requires a maximum of 9 CLK periods

Figure 20. MNM Microport Write Timing Requirements.



Notes:
1. t_{ACC} Access time depends on the Address accessed. Access time is measured from the FE of /DS to the FE of /DTACK. t_{ACC} requires a maximum of 13 CLK periods

Figure 21. MNM Microport Read Timing Requirements.

AD6652 THEORY OF OPERATION

INTRODUCTION

The AD6652 has two analog input channels, four digital filtering channels and two digital output channels. The signal at each output channel may experience up to seven signal-processing operations:

1. 12-Bit A/D Conversion
2. Frequency Translation (from IF to Baseband)
3. Second Order Re-Sampling Cascaded Integrator Comb FIR Filtering (rCIC2)
4. Fifth Order Cascaded integrator Comb FIR Filtering (CIC5)
5. RAM Coefficient FIR Filtering (RCF)
6. Automatic Gain Control (AGC)
7. 2x Interpolation

The digitally filtered channels allow up to four signals to be concurrently processed from the ADC stage. Flexible channel multiplexing allows one to four channels to be interleaved onto one output port. Four synchronization input pins allow AD6652 start-up and frequency hop functions to be precisely orchestrated with other devices. The NCOs phase can be programmed to produce carriers with known phase offset. Programming and control is accomplished using either 2-wire serial or 8-bit parallel microport interfaces.

ADC ARCHITECTURE

The AD6652 front-end consists of two 12-bit A/D converters, preceded by high performance sample-and-hold amplifiers (SHA) capable of excellent performance up to 200 MHz. A flexible, integrated voltage reference allows analog inputs up to 2V p-p. An over-range bit for each channel is provided to signal when an out-of-range condition exists. Both ADC channels are internally routed to the input matrix of the Receive Signal Processor (RSP) stage for channel routing, frequency translation, baseband filtering and data output configuration.

Each Sample and Hold Amplifier (SHA) is followed by a pipelined switched capacitor A/D converter. The pipelined A/D converter is divided into three sections, consisting of a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and inter-stage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

ANALOG INPUT

The analog inputs to the AD6652 are differential switched capacitor SHAs that have been designed for optimum performance while processing differential ac or dc input signals. The SHA input can support a wide common-mode range and maintain excellent performance. An input common-mode voltage of mid-supply will minimize signal-dependant errors and provide optimum performance.

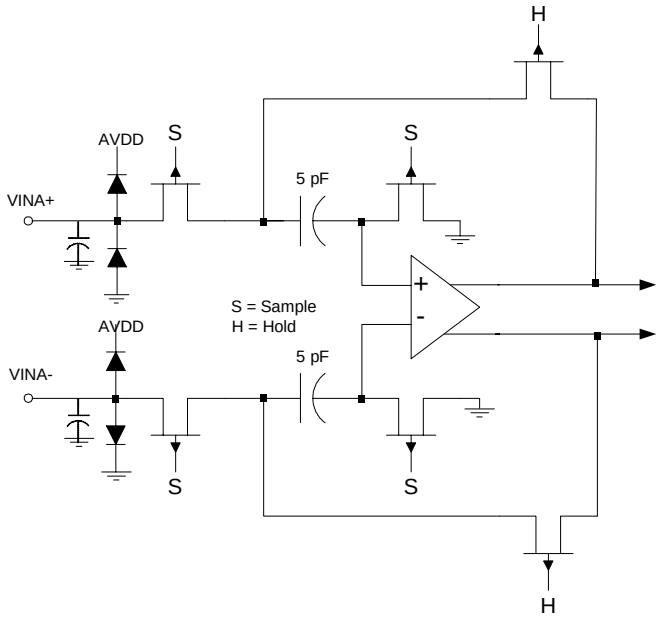


Figure 22. Switched-Capacitor SHA Input for one ADC channel

Referring to Figure 22, the clock signal alternatively switches the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network will create a low-pass filter at the

ADC's input; therefore, the precise values are dependant upon the application. In IF under-sampling applications, any shunt capacitors should be removed. In combination with the driving source impedance, they would limit the input bandwidth.

For best dynamic performance, the source impedances driving the differential analog inputs should be matched such that common-mode settling errors are symmetrical. These errors will be reduced by the common-mode rejection of the ADC.

The SHA may be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined as follows:

$$VCM_{MIN} = VREF/2,$$
$$VCM_{MAX} = (AVDD + VREF)/2$$

The minimum common-mode input level allows the AD6652 to accommodate ground-referenced inputs.

Although optimum performance is achieved with a differential input, a single-ended source may be driven into VINA or VINB. In this configuration, one input will accept the signal, while the opposite input should be set to mid-scale by connecting it to an appropriate reference. For example, a 2 V p-p signal may be applied to VINA while a 1 V reference is applied to VINB. The AD6652 will then accept a signal varying between 2 V and 0 V. In the single-ended configuration, distortion performance may degrade significantly as compared to the differential case. However, the effect will be less noticeable at lower input frequencies.

DIFFERENTIAL INPUT CONFIGURATIONS

As previously detailed, optimum performance will be achieved while driving the AD6652 inputs in a differential input configuration. For baseband (dc to 32.5 MHz) applications, the AD8138 Differential Driver provides excellent performance and a flexible interface to the A/D converter. The output common-mode voltage of the AD8138 is easily set to AVDD/2, and the driver can be configured in a Sallen Key filter topology to provide band limiting of the input signal. The schematic diagram in Figure 23 is a recommended example of a baseband differential driver for the AD6652 inputs.

At input frequencies above the Nyquist zone (>32.5 MHz), the performance of most amplifiers will not be adequate to achieve the true performance of the AD6652 ADC stage. This is especially true in IF under-sampling applications where frequencies in the 70 MHz to 200 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration as shown in Figure 24.

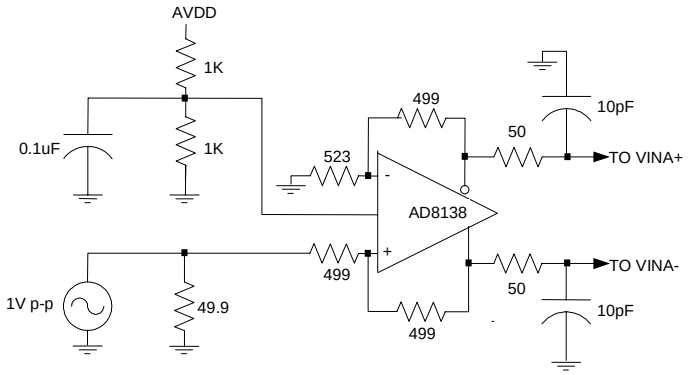


Figure 23. Differential Input for a single channel of the AD6652 using the AD8138 for Nyquist applications (dc to 32.5 MHz).

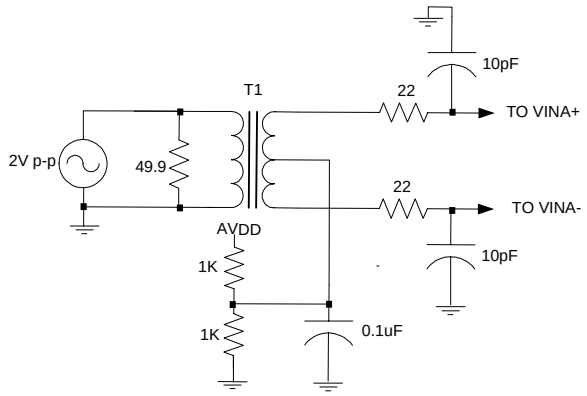


Figure 24. Differential Transformer-Coupled Input for a single channel of the AD6652.

The circuit in Figure 24 should be considered for input frequencies above the first Nyquist zone (32.5 to 200 MHz). T1 is a broadband center-tapped 1:1 RF transformer such as Mini Circuits T1-1T.The signal characteristics must be considered when selecting a transformer. Some RF transformers will saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

SINGLE-ENDED INPUT CONFIGURATION

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration there will be degradation in SFDR and distortion performance due to

the large input common-mode swing. However, if the source impedances on each input are matched, there should be little effect on SNR performance. Figure 25 details a typical single-ended input configuration.

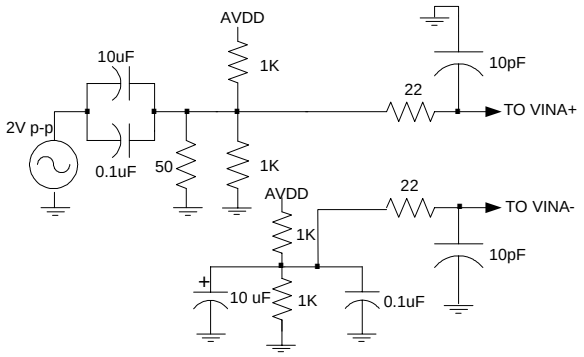


Figure 25. AC-Coupled Single-Ended Input for a single ADC Input Channel

ADC VOLTAGE REFERENCE

An internal differential reference buffer creates positive (top) and negative (bottom) reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common mode of the reference buffer is set to mid-supply, and the REFT and REFB voltages and span are defined as follows:

REFT = 1/2 (AVDD + VREF),
REFB = 1/2 (AVDD - VREF),
Span = 2 x (REFT-REFB) = 2 x VREF.

It can be seen from the equations above that the REFT and REFB voltages are symmetrical about the mid-supply voltage and, by definition, the input span is twice the value of the VREF voltage.

The internal voltage reference can be pin-strapped to fixed values of 0.5 V or 1.0 V, or adjusted within the same range as discussed in the Internal Reference Connection section. Maximum SNR performance will be achieved with the reference set to the largest input span of 2 Vp-p. The relative SNR degradation will be 3 dB when changing from 2 Vp-p mode to 1 Vp-p mode.

A stable and accurate 0.5 V voltage reference is built into the AD6652. The input range can be adjusted by varying the reference voltage applied to the AD6652, using either the internal reference or an externally applied reference voltage. The input span of each ADC tracks reference voltage changes linearly. If the ADC is being driven differentially through a transformer, the reference voltage can be used to bias the center tap (common-mode voltage).

INTERNAL REFERENCE CONNECTION

A comparator within the AD6652 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table II. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 27), setting VREF to 1 V. Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected as shown in Figure FFF, the switch will again be set to the SENSE pin. This will put the reference amplifier in a non-inverting mode with the VREF output defined as follows:

VREF = 0.5 x (1 + R2/R1)In all reference configurations, REFT and REFB drive the A/D conversion core and establish its input span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

Table II. Reference SENSE Operation

SENSE Voltage	Internal Switch Position	Selected Mode	Resulting VREF (V)	Resulting Differential Span (V p-p)
AVDD	N/A	External Reference	N/A	2 x External Reference
VREF	SENSE	Internal Fixed Reference	0.5	1.0
0.2 V to VREF	SENSE	Programmable Reference	0.5 x (1+R2/R1)	2 x VREF (See Fig. yyy)
AGND to 0.2V	Internal Divider	Internal Fixed Reference	1.0	2.0

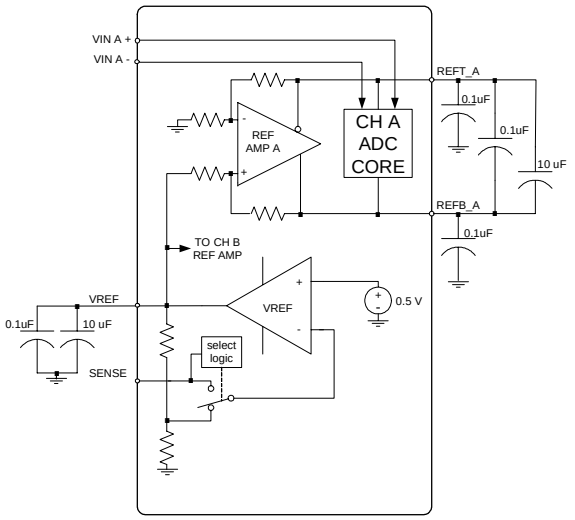


Figure 26. Fixed reference configuration showing the common VREF and Ch.A connections. Ch. B connections are identical to those of Ch. A.

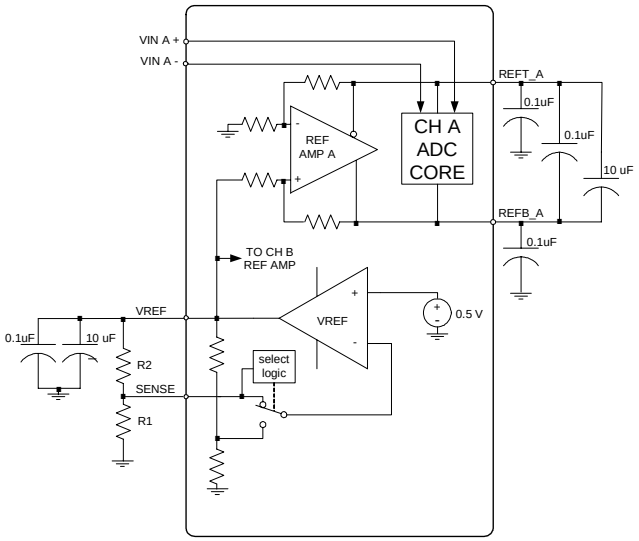


Figure 27. Programmable reference configuration showing the common VREF and Ch. A connections. Ch. B connections are identical to those of Ch. A.

EXTERNAL REFERENCE OPERATION

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. When multiple ADCs track one another, a single reference (internal or external) may be necessary to reduce gain-matching errors to an acceptable level. A high precision external reference may also be selected to provide lower gain and offset temperature drift.

When the SENSE pin is tied to AVDD, the internal reference will be disabled, allowing the use of an external reference. An internal reference buffer will load the external reference with an equivalent 7 kΩ load. The internal buffer will still generate the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span will always be twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1 V.

If the internal reference of the AD6652 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered.

CLOCK INPUT CONSIDERATIONS

Typical high-speed A/D converters use both clock edges to generate a variety of internal timing signals, and as a result may be sensitive to ACLK clock duty cycle. Commonly a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD6652 contains a clock duty cycle stabilizer that re-times the non-sampling edge, providing an internal clock signal with a nominal 50% duty cycle. Duty cycle stabilizing is engaged by setting DUTYEN, pin B12, to logic high. This allows a wide range of ACLK clock input duty cycles without affecting the performance of the AD6652 ADC stage. The duty cycle stabilizer uses a delay-locked loop (DLL) to create the non-sampling edge. As a result, any changes to the sampling frequency will require approximately 2 – 3 microseconds to allow the DLL to acquire and lock to the new rate.

High-speed, high-resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to aperture jitter (t_A) can be calculated with the following equation:

$$\text{SNR } \textit{degradation} = 20 \times \log10 \left[1/2 \times p \times f_{INPUT} \times t_A\right]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. Under-sampling or IF sampling applications are particularly sensitive to jitter.

The ACLK clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD6652 ADC stage. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the ACLK clock is generated from another type of source (by gating, dividing, or other methods), it should be re-timed by the original clock at the last step.

ADC POWER-DOWN MODE
The power dissipated by the AD6652 front end ADC is proportional to its sampling rate. Normal ADC operation requires that PDWNA and PDWNB be set to logic low. However, the ADC can be placed in a power-down mode by setting the PDWNA or PDWNB pins to logic high. In this mode, the ADC sampling rate is irrelevant. Low power dissipation in power-down mode is achieved by shutting-down the reference buffers and biasing networks of both channels. In this mode, power consumption of the ADC drops from a maximum of 600mW during normal operation to <2mW. Both power down pins must be either high or low for proper ADC operation.

ADC WAKE-UP TIME
The decoupling capacitors on REFT and REFB are discharged when entering standby mode, and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in standby mode, and shorter standby cycles will result in proportionally shorter wake-up times. With the recommended 0.1 µF and 10 µF decoupling capacitors on REFT and REFB, it takes approximately one second to fully discharge the reference buffer decoupling capacitors, and 5 ms to restore full operation.

RECEIVE SIGNAL PROCESSOR (RSP) ARCHITECTURE

Data Input Matrix
The RSPsection features dual high-speed 12-bit input ports that are capable of crossbar multiplexing of data to the four processing channels that follow the input matrix. In addition, a third input option to the matrix is available to facilitate BIST (built-in self test). This option is a PN (pseudo-random noise) sequence. The dual input ports allow unusual flexibility with a single tuner chip. These can be diversity inputs or truly independent inputs such as separate antenna segments. Either input port or the PN sequence can be routed to any or all of the four tuner channels. This flexibility allows for up to 4 different analog sources to be processed simultaneously.

Numerically Controlled Oscillator
Frequency translation is accomplished with a 32-bit complex Numerically Controlled Oscillator (NCO). Each of the four processing channels contains a separate NCO. Real data entering this stage is separated into in-phase (I) and quadrature (Q) components. This stage translates the input signal from a digital intermediate frequency (IF) to digital baseband. Phase and amplitude dither may be enabled on-chip to improve spurious performance of the NCO. A phase-offset word is available to create a known phase relationship between multiple AD6652s or between channels.

2nd ORDER rCIC FILTER
Following frequency translation is a re-sampling, fixed coefficient, high speed, second order, Re-Sampling Cascade Integrator Comb (rCIC2) filter that reduces the sample rate based on the ratio between the decimation and interpolation registers. The re-sampler allows for non-integer relationships between the master clock and the output data rate. This stage may be bypassed by setting the decimation/interpolation ratio to 1.

5th ORDER CIC FILTER
The next stage is a fifth order Cascaded Integrator Comb (CIC5) filter whose response is defined by the decimation rate. The purpose of these filters is to reduce the data rate to the final filter stage so that it can calculate more taps per output.

RAM COEFFICIENT FILTER
The RCF stage is a sum-of-products FIR filter with programmable 20-bit coefficients, and decimation rates programmable from 1 to 256 (1-32 in practice). Each RAM Coefficient FIR Filter (RCF in Figure 1) can handle a maximum of 160 taps. Two or more RCF stages may be combined using flexible channel configuration to increase the processing power beyond the 160 tap maximum.

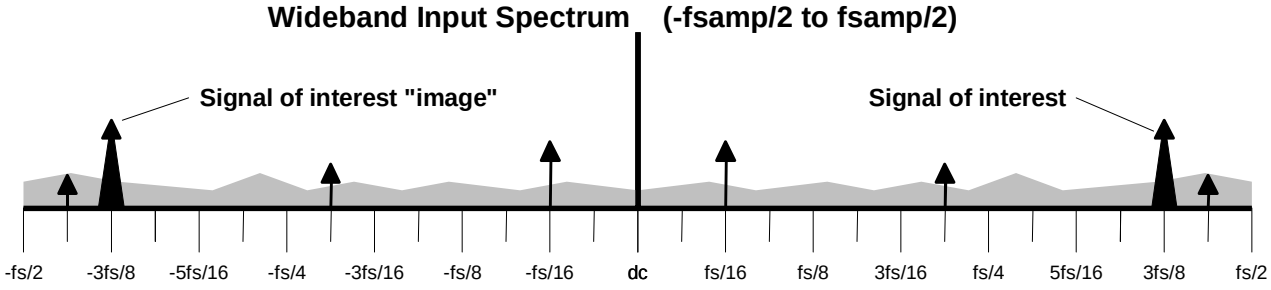
The RCF outputs of each channel are directly routed to both output port multiplexers. The output multiplexer can route any of the four channels to the Parallel outputs or Link outputs.

INTERPOLATING HALF-BAND FILTERS AND AGC

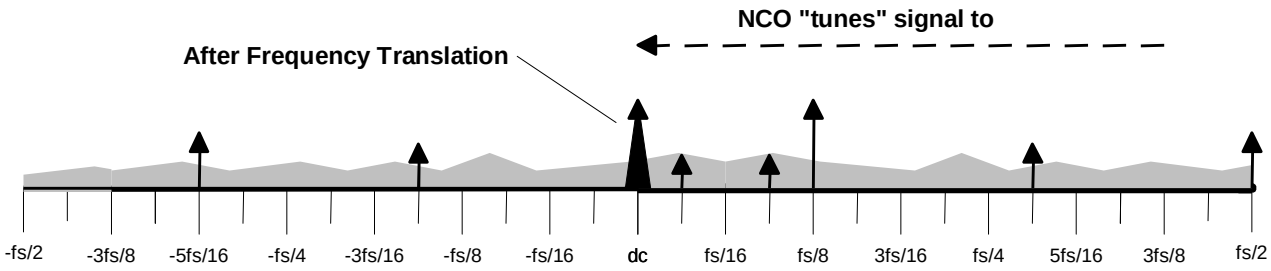
Processed RCF data may also be routed to two half-band interpolation stages where up to four channels may be combined (interleaved), interpolated by a factor of two and AGC (automatic gain control) applied. Each AGC stage has a dynamic range of 96.3 dB. These half-band filters and AGC stages can be bypassed independently of each other. The outputs from the two AGC stages are routed to both output port multiplexers. Each output has a "link" port to permit seamless data interface with DSP devices such as the TigerSHARC™. A multiplexer for each port selects one of the six data sources to appear at the device Parallel or Link output pins.

The overall filter response for the AD6652 is the composite of all decimating and interpolating stages. Each successive filter stage is capable of narrower transition bandwidths but requires a greater number of DCLK cycles to calculate the output. More decimation in the first filter stage will minimize overall power consumption.

Figure 28 illustrates the basic function of the AD6652: that is, to select and filter a single channel from a wide input spectrum. The frequency translator "tunes" the desired carrier to base band. Figure 29 shows the combined filter response of the rCIC2, CIC5, and RCF.



Wideband Input Spectrum (e.g. 30MHz from Highspeed ADC)



Frequency Translation (e.g. single 1MHz channel tuned to basband)

Figure 28. AD6652 Frequency Translation of Wideband Input Spectrum

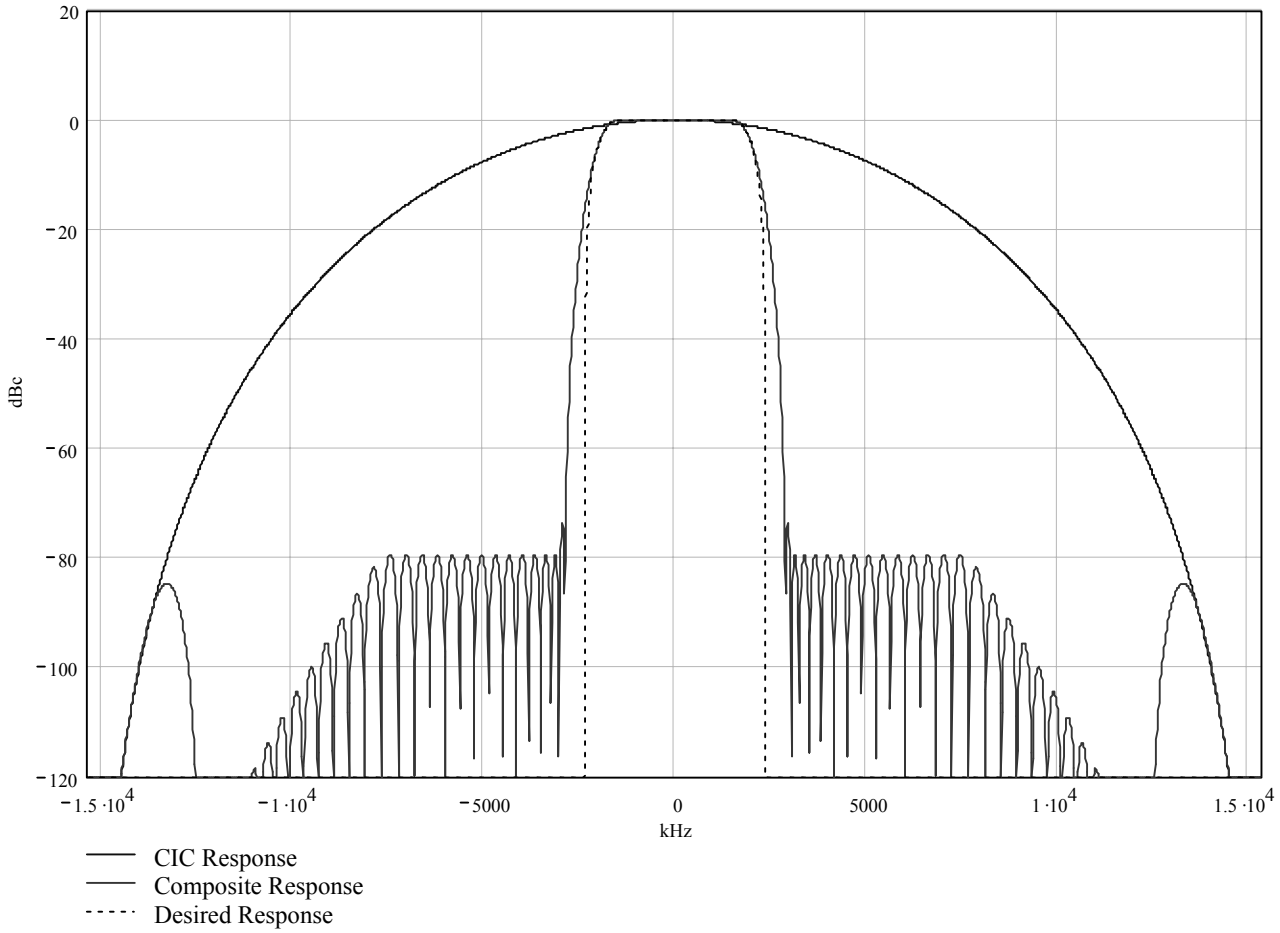


Figure 29. Composite Filter Response of rCIC2, CIC5, and RCF

MEMORY MAPPING AND ADDRESS NOTATION

For the remainder of this document, frequent text references will be made to programming registers and memory mapping. The reader is advised to become familiar with the "MICROPORT CONTROL" section, now, to gain an overview of the AD6652 register/memory mapping structure. All register addresses beginning with 0x indicate that the address characters that follow are in hexadecimal notation. A colon following an address indicates which bit(s), in decimal format, is/are involved.

RECEIVE INPUT MATRIX

The receive signal processor stages feature dual high-speed crossbar-switched input ports that allow the most flexibility in routing the two ADC data streams to the four receive processing channels. These can be diversity inputs or truly independent inputs such as separate antenna segments. Crossbar switching means that any of the four processing channels may receive data from either port A or port B for a total of 16 possible combinations as seen in Table III below. Input port routing is selected in each NCOs control register at 0x88:6.

CH 3	CH 2	CH 1	CH0
A	A	A	A
A	A	A	B
A	A	B	A
A	A	B	B
A	B	A	A
A	B	A	B
A	B	B	A
A	B	B	B
B	A	A	A
B	A	A	B

B	A	B	A
B	A	B	B
B	B	A	A
B	B	A	B
B	B	B	A
B	B	B	B

Table III. Crossbar-switched routing of the two 12-bit ADC data streams (A & B) using the RSP input matrix

RSP Data Latency
The overall signal path latency from RSP input to output can be expressed in high-speed clock cycles. The equation below can be used to calculate the latency.

$$T_{latency} = M_{rCIC2}\left(M_{CIC5} + 7\right) + N_{taps} + 26$$

M_{rCIC2} and M_{CIC5} are decimation values for the rCIC2 and CIC5 filters respectively, N_{taps} is the number RCF taps chosen.

Frequency Translation
This processing stage comprises a digital tuner consisting of two multipliers and a 32-bit complex NCO. Each channel of the AD6652 has an independent NCO. The NCO serves as a quadrature local oscillator capable of producing a NCO frequency between –DCLK/2 and +DCLK/2 with a resolution of DCLK/2^{32} in the complex mode. The worst-case spurious signal from the NCO is better than -100dBc for all output frequencies.

The NCO frequency programmed in registers 0x85 and 0x86 is interpreted as a 32-bit unsigned integer. The NCO frequency is calculated using the equation below.

$$NCO\_FREQ = 2^{32} * \mathrm{mod}(\frac{f_{channel}}{DCLK})$$

where:
NCO_FREQ is the decimal equivalent of the 32-bit binary value that should be programmed at registers 0x85 and 0x86.
$f_{channel}$ is the desired channel frequency in Hz and DCLK is the AD6652 RSPmaster clock rate (in Hz). The function "mod" indicates that the operation within the parenthesis must have any integer value removed such that only the "remainder" is utilized.

NCO Frequency Hold-Off Register
When the NCO Frequency registers are written, data is actually passed to a shadow register. Data may be moved to the main registers by one of two methods. When the channel comes out of sleep mode or when a SYNC Hop occurs. In either event a counter can be loaded with NCO Frequency Hold-Off register value. The 16-bit unsigned integer counter (0x84) starts counting down clocked by the Master clock and when it reaches zero the new Frequency value in the shadow register is written to the NCO Frequency register. The NCO could also be setup to SYNC immediately in which case the Frequency Hold-off counter is bypassed and new Frequency values are updated immediately.

Phase Offset
The phase offset register (0x87) adds an offset to the phase accumulator of the NCO. This is a 16-bit register and is interpreted as a 16-bit unsigned integer. A 0x0000 in this register corresponds to a 0 Radian offset and a 0xFFFF corresponds to an offset of 2π* (1-(1/2^{16})) radians. This register allows multiple NCOs to be synchronized to produce sine waves with a known and steady phase difference.

NCO Control Register
The NCO control register located at 0x88 is used to configure the features of the NCO. These are controlled on a per channel basis. These are described below.

By-Pass
The NCO of the AD6652 can be by-passed. By-Pass mode is enabled by setting bit 0 of 0x88 high. When the NCO is by-passed, down conversion is not performed and the AD6652 channel functions simply as a real filter on complex data. This is useful for base-band sampling applications where the A input is connected to the I signal path within the filter and the B input is connected to the Q signal path. This may be desired if the digitized signal has already been converted to baseband in prior analog stages or by other digital preprocessing.

Phase Dither
The AD6652 provides a phase dither option for improving the spurious performance of the NCO. Phase Dither is enabled by setting bit 1of register 0x88. When phase dither is enabled by setting this bit high, spurs due to phase truncation in the NCO are randomized. The energy from these spurs is spread into the noise floor and Spurious Free Dynamic Range is increased at the expense of very slight decreases in the SNR. The choice of whether Phase Dither is used in a system will ultimately be decided by the system goals. If lower spurs are desired at the expense of a slightly raised noise floor, it should be employed. If a low noise floor is desired and the higher spurs can be tolerated or filtered by subsequent stages, then Phase Dither is not needed.

Amplitude Dither
Amplitude Dither can also be used to improve spurious performance of the NCO. Amplitude Dither is enabled by setting bit 2 of 0x88. Amplitude Dither improves performance by randomizing the amplitude quantization errors within the angular to Cartesian conversion of the NCO. This option may reduce spurs at the expense of a slightly raised noise floor. Amplitude Dither and Phase Dither can be used together, separately or not at all.

Clear Phase Accumulator on HOP
When bit 3 is set, the NCO phase accumulator is cleared prior to a frequency hop. This ensures a consistent phase of the NCO on each hop. The NCO phase offset is unaffected by this setting. If phase continuous hopping is desired, this bit should be cleared and the last phase in the NCO phase register will be the beginning phase for the new frequency.

Reserved
Bits 4 and 5 are reserved and should written to logic 0.

Input Select
Bit 6 of NCO control register at address 0x88 controls input port selection. If this bit is set high, then input port B is connected to the selected filter channel. If this bit is cleared, then input port A is connected to the selected filter channel.

Sync Pin Select
Bits 7 and 8 of the NCO control register determine which external sync pin (if any) is assigned to the channel of interest. The AD6652 has four sync pins: SYNCA, SYNCB, SYNCC, and SYNCD. Any of these sync pins can be assigned to any or all of the four receiver channels of the AD6652; however, a channel may have only one sync pin assigned to it. The sync pin(s) must also be enabled in the PIN_SYNC Control Register at address 4 of the External Memory Map. Table IV shows bit values to select a specific external sync pin. A

Address/bit 0x88:8	Address/bit 0x88:7	SELECTED SYNC PIN
0	0	SYNCA
0	1	SYNCB
1	0	SYNCC
1	1	SYNCD

Table IV. Programming channel address register (CAR) bits to choose a sync pin for a selected NCO.

2nd ORDER rCIC FILTER

The rCIC2 filter is a second order Cascaded re-sampling Integrator Comb filter. The resampler is implemented using a unique technique, which does not require the use of a high-speed clock, thus simplifying the design and saving power. The re-sampler allows for non-integer relationships between the master clock and the output data rate. This allows easier implementation of systems that are either multi-mode or require a master clock that is not a multiple of the data rate to be used.

Interpolation up to 512 and decimation up to 4096 is allowed in the rCIC2. The re-sampling factor for the rCIC2 (L) is a 9-bit integer. When combined with the decimation factor M, a 12-bit number, the total rate-change can be any fraction in the form of:

$$R_{rCIC2} = \frac{L}{M}$$
$$R_{rCIC2} \le 1$$

The only constraint is that the ratio L/M must be less than or equal to one. This implies that the rCIC2 decimates by 1 or more.

Re-sampling is implemented by apparently increasing the input sample rate by the factor L, using zero stuffing for the new data samples. Following the re-sampler is a second order cascaded integrator comb filter. Filter characteristics are determined only by the fractional rate-change (L/M).

The filter can process signals at the full rate of the input port (65 MHz). The output rate of this stage is given by the equation below.

$$f_{SAMP\ 2} = \frac{L_{rCIC\ 2}\, f_{SAMP}}{M_{\ rCIC\ 2}}$$

Both L_{rCIC2} and M_{rCIC2} are unsigned integers. The interpolation rate (L_{rCIC2}) may be from 1 to 512 and the decimation (M_{rCIC2}) may be between 1 and 4096. The stage can be bypassed by setting the decimation to 1/1. The frequency response of the rCIC2 filter is given by the following equations.

$$H(z) = \frac{1}{2^{S_{rCIC2}} \cdot L_{rCIC2}} \cdot \left(\frac{1 - z^{-\frac{M_{rCIC2}}{L_{rCIC2}}}}{1 - z^{-1}} \right)^2$$

$$H(f) = \frac{1}{2^{S_{rCIC2}} \cdot L_{rCIC2}} \cdot \left(\frac{\sin\left(\pi \frac{M_{rCIC2} \cdot f}{L_{rCIC2} \cdot f_{SAMP}} \right)}{\sin\left(\pi \frac{f}{f_{SAMP}} \right)} \right)^2$$

The gain and passband droop of the rCIC2 should be calculated by the equations above, as well as the filter transfer equations that follow. Excessive passband droop can be compensated for in the RCF stage by peaking the passband by the inverse of the roll-off.

rCIC2 Scale Factor

The scale factor, S_{rCIC2} is a programmable unsigned 5 bit between 0 and 31. This serves as an attenuator that can reduce the gain of the rCIC2 in 6dB increments. For the best dynamic range, S_{rCIC2} should be set to the smallest value possible (i.e. lowest attenuation) without creating an overflow condition. This can be safely accomplished using the next equation that follows. The SrCIC2 scale factor is always used whether or not the rCIC2 is bypassed.

The S_{rCIC2} value must be less than 32 or the interpolation and decimation rates must be adjusted to validate this equation. The ceil function denotes the next whole integer and the floor function denotes the previous whole integer. For example, the ceil(4.5) is 5 while the floor(4.5) is 4.

When SrCIC2 has been determined for all channels, it must be programmed at 0x92 [9:5] of each channel address register. The same value should also be programmed at 0x92[4:0] to accommodate a redundant hardware feature.

The gain and pass-band droop of the rCIC2 should be calculated by the equations above, as well as the rCIC2 filter transfer equations. Excessive passband droop can be compensated for in the RCF stage by peaking the passband by the inverse of the roll-off.

$$S_{rCIC2} = ceil\left[\log_2 \left(\begin{array}{l} M_{rCIC2} + floor\left(\frac{M_{rCIC2}}{L_{rCIC2}} \right) * \\ \left(2 * M_{rCIC2} - L_{rCIC2} * floor\left(\frac{M_{rCIC2}}{L_{rCIC2}} + 1 \right) \right) \end{array} \right) \right]$$

rCIC2 Output Level

After the proper scaling factor has been determined, the output level from the rCIC2 stage can be determined using the following equation.

$$OL_{rCIC2} = \frac{\left(M_{rCIC2}{}^2 \right)}{L_{rCIC2} * 2^{S_{rCIC2}}} * input\_level$$

Where input_level is normally full-scale (or 1) from the ADC to the rCIC2 stage and OLrCIC2 is the output level from the rCIC2 stage expressed as a fraction of the input_level. OLrCIC2 will be used later in the CIC5 stage level calculations.

rCIC2 Rejection

Table V illustrates the amount of bandwidth in percent of the data rate into the rCIC2 stage. The data in this table may be scaled to any other allowable sample rate up to 65 MHz. The table can be used as a tool to decide how to distribute the decimation between rCIC2, CIC5 and the RCF.

Example Calculations

Goal: Implement a filter with an Input Sample Rate of 10MHz requiring 100dB of Alias Rejection for a +/- 7kHz passband.

Solution: First determine the percentage of the sample rate that is represented by the pass band.

$$BW_{fraction} = 100 * \frac{7kHz}{10MHz} = 0.07$$

Find the -100dB column on the right of the table and look down this column for a value greater than or equal to your passband percentage of the clock rate. Then look across to the extreme left column and find the corresponding rate change factor (M_{rCIC2}/L_{rCIC2}). Referring to the table, notice that for a M_{rCIC2}/L_{rCIC2} of 4, the frequency having -100dB of alias rejection is 0.071 percent, which is slightly greater than the 0.07 percent calculated. Therefore, for this example, the maximum bound on rCIC2 rate change is 4. A higher chosen M_{rCIC2}/L_{rCIC2} means less alias rejection than the 100dB required.

An M_{rCIC2}/L_{rCIC2} of less than 4 would still yield the required rejection, however, the power consumption can be minimized by decimating as much as possible in this rCIC2 stage. Decimation in rCIC2 lowers the data rate, and thus reduces power consumed in subsequent stages. It should also be noted that there is more than one way to get the decimation by 4. A decimation of 4 is the same as an L/M

ratio of 0.25. Thus any integer combination of L/M that yields 0.25 will work (1/4, 2/8 or 4/16). However, for the best dynamic range, the simplest ratio should be used. For example, ¼ gives better performance than 4/16.

M_{rCIC2}/ L_{rCIC2}	-50dB	-60dB	-70dB	-80dB	-90dB	-100dB
2	1.79	1.007	0.566	0.318	0.179	0.101
3	1.508	0.858	0.486	0.274	0.155	0.087
4	1.217	0.696	0.395	0.223	0.126	0.071
5	1.006	0.577	0.328	0.186	0.105	0.059
6	0.853	0.49	0.279	0.158	0.089	0.05
7	0.739	0.425	0.242	0.137	0.077	0.044
8	0.651	0.374	0.213	0.121	0.068	0.038
9	0.581	0.334	0.19	0.108	0.061	0.034
10	0.525	0.302	0.172	0.097	0.055	0.031
11	0.478	0.275	0.157	0.089	0.05	0.028
12	0.439	0.253	0.144	0.082	0.046	0.026
13	0.406	0.234	0.133	0.075	0.043	0.024
14	0.378	0.217	0.124	0.07	0.04	0.022
15	0.353	0.203	0.116	0.066	0.037	0.021
16	0.331	0.19	0.109	0.061	0.035	0.02

Table V SSB rCIC2 Alias Rejection Table (f_{SAMP} = 1) Bandwidth shown in percentage of f_{SAMP}.

Decimation and Interpolation Registers
rCIC2 decimation values are stored in register 0x90. This register is a 12-bit register and contains the decimation portion less 1. The interpolation portion is stored in register 0x91. This 9-bit value holds the interpolation less one.

rCIC2 Scale Register
Register 0x92 contains the scaling information for this section of the circuit. The primary function is to store the scale value computed in the sections above.

Bits 4-0 of this register should be written with the same values of those written to bits 9-5 to accommodate an redundant internal hardware feature.

Bits 9-5 (SrCIC2) contain the 5-bit scaling factor for rCIC2.

Bit 10 of this register is reserved and must be written low.

Bit 11 of this register is reserved and must be written low.

In applications that do not require the features of the rCIC2, it may be by-passed by setting the L/M ratio to 1/1. This effectively bypasses all circuitry of the rCIC2 except the scaling which is still effectual.

5th ORDER CIC FILTER

The fourth signal processing stage, CIC5, implements a sharper fixed-coefficient, decimating filter than rCIC2. The input rate to this filter is f_{SAMP2}. The maximum input rate is given by the equation below. N_{CH} equals two for Diversity Channel Real input mode; otherwise N_{CH} equals one. In order to satisfy this equation, M_{rCIC2} can be increased, N_{CH} can be reduced, or f_{CLK} can be increased (reference fractional rate input timing described in the "Input Timing" section).

$$f_{SAMP2} \le \frac{f_{CLK}}{N_{CH}}$$

The decimation ratio, M_{CIC5}, may be programmed from 2 to 32 (all integer values). The frequency response of the filter is given by the following equations. The gain and passband droop of CIC5 should be calculated by these equations. Both parameters may be compensated for in the RCF stage.

$$H(z) = \frac{1}{2^{S_{CIC5}+5}} \cdot \left(\frac{1 - z^{-M_{CIC5}}}{1 - z^{-1}} \right)^5$$

$$H(f) = \frac{1}{2^{S_{CIC5}+5}} \cdot \left(\frac{\sin\left(\pi \frac{M_{CIC5} \cdot f}{f_{SAMP2}} \right)}{\sin\left(\pi \frac{f}{f_{SAMP2}} \right)} \right)^5$$

The scale factor, S_{CIC5} is a programmable unsigned integer between 0 and 20. It serves to control the attenuation of the data into the CIC5 stage in 6dB increments. For the best dynamic range, S_{CIC5} should be set to the smallest value possible(lowest attenuation) without creating an overflow condition. This can be safely accomplished using the equation below, where OL_{rCIC2} is the largest fraction of full scale possible at the input to this filter stage. This value is output from the rCIC2 stage then pipe-lined into the CIC5.

$$S_{CIC5} = ceil\left(\log_2 \left({M_{CIC5}}^5 \cdot OL_{rCIC2} \right) \right) - 5$$

$$OL_{CIC5} = \frac{\left({M_{CIC5}}^5 \right)}{2^{S_{CIC5}+5}} \cdot OL_{rCIC2}$$

The output rate of this stage is given by the equation below.

$$f_{SAMP5} = \frac{f_{SAMP2}}{M_{CIC5}}$$

CIC5 Rejection

Table VI illustrates the amount of bandwidth in percentage of the clock rate that can be protected with various decimation rates and alias rejection specifications. The maximum input rate into the CIC5 is 65MHz when the rCIC2 decimates by 1. As in the previous table, these are the ½ bandwidth characteristics of the CIC5. Notice that the CIC5 stage can protect a much wider band to any given rejection.

M_{CIC5}	-50dB	-60dB	-70dB	-80dB	-90dB	-100dB
2	10.277	8.078	6.393	5.066	4.008	3.183
3	7.924	6.367	5.11	4.107	3.297	2.642
4	6.213	5.022	4.057	3.271	2.636	2.121
5	5.068	4.107	3.326	2.687	2.17	1.748
6	4.267	3.463	2.808	2.27	1.836	1.48
7	3.68	2.989	2.425	1.962	1.588	1.281
8	3.233	2.627	2.133	1.726	1.397	1.128
9	2.881	2.342	1.902	1.54	1.247	1.007
10	2.598	2.113	1.716	1.39	1.125	0.909
11	2.365	1.924	1.563	1.266	1.025	0.828
12	2.17	1.765	1.435	1.162	0.941	0.76
13	2.005	1.631	1.326	1.074	0.87	0.703
14	1.863	1.516	1.232	0.998	0.809	0.653
15	1.74	1.416	1.151	0.932	0.755	0.61
16	1.632	1.328	1.079	0.874	0.708	0.572
17	1.536	1.25	1.016	0.823	0.667	0.539
18	1.451	1.181	0.96	0.778	0.63	0.509
19	1.375	1.119	0.91	0.737	0.597	0.483
20	1.307	1.064	0.865	0.701	0.568	0.459
21	1.245	1.013	0.824	0.667	0.541	0.437
22	1.188	0.967	0.786	0.637	0.516	0.417
23	1.137	0.925	0.752	0.61	0.494	0.399
24	1.09	0.887	0.721	0.584	0.474	0.383
25	1.046	0.852	0.692	0.561	0.455	0.367
26	1.006	0.819	0.666	0.54	0.437	0.353
27	0.969	0.789	0.641	0.52	0.421	0.34
28	0.934	0.761	0.618	0.501	0.406	0.328
29	0.902	0.734	0.597	0.484	0.392	0.317
30	0.872	0.71	0.577	0.468	0.379	0.306
31	0.844	0.687	0.559	0.453	0.367	0.297
32	0.818	0.666	0.541	0.439	0.355	0.287

Table VII. SSB CIC5 Alias Rejection Table (f_{SAMP2} = 1)

This table helps to calculate an upper bound on decimation, M_{CIC5}, given the desired filter characteristics.

RAM COEFFICIENT FILTER

The final signal processing stage is a sum-of-products decimating filter with programmable coefficients. A simplified block diagram is shown below. The data memories I-RAM and Q-RAM store the 160 most recent complex samples from the previous filter stage with 20-bit resolution. The coefficient memory, CMEM, stores up to 256 coefficients with 20-bit resolution. On every DCLK cycle one tap for I and one tap for Q are calculated using the same coefficients. The RCF output consists of 24 bits I data and 24 bits Q data.

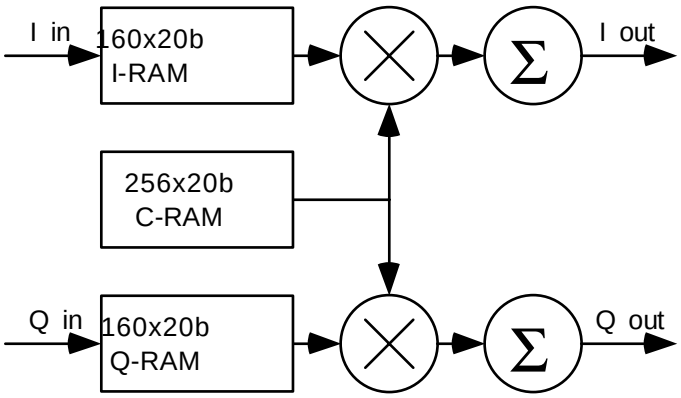


Figure 30. RAM Coefficient Filter Block Diagram

RCF Decimation Register

Each RCF channel can be used to decimate the data rate. The decimation register is an 8 bit register and can decimate from 1 to 256. The RCF decimation is stored in 0xA0 in the form of M_{RCF} -1. The input rate to the RCF is f_{SAMP5}.

RCF Decimation Phase

The RCF decimation phase can be used to synchronize multiple filters within a chip. This is useful when using multiple channels within the AD6652 to implement poly-phase filter allowing the resources of several filters to be paralleled. In such an application, two RCF filters would be processing the same data from the CIC5. However, each filter will be delayed by one half the decimation rate, thus creating a 180-degree phase difference between the two halves. The AD6652 filter channel uses the value stored in this register to pre-load the RCF counter. Therefore, instead of starting from 0, the counter is loaded with this value, thus creating an offset in the processing that should be equivalent to the required processing delay. This data is stored in 0xA1 as an 8-bit number.

RCF Filter Length

The maximum number of taps this filter can calculate, N_{taps}, is given by the equation below. The value N_{taps}-1 is written to the channel register within the AD6652 at address 0xA2.

$$N_{taps} \le \min\left(\frac{f_{CLK} \cdot M_{RCF}}{f_{SAMP5}}, 160 \right)$$

Where "min" indicates that N_{taps} is the lesser of the two values, separated by the comma, that appear within the brackets.

The RCF coefficients are located in addresses 0x00 to 0x7F and are interpreted as 20-bit 2's complement numbers. When writing the coefficient RAM, the lower addresses will be multiplied by relatively older data from the CIC5 and the higher coefficient addresses will be multiplied by relatively newer data from the CIC5. The coefficients need not be symmetric and the coefficient length, N_{taps}, may be even or odd. If the coefficients are symmetric, then both sides of the impulse response must be written into the coefficient RAM.

Although the base memory for coefficients is only 128 words long, the actual length is 256 words long. There are two pages, each of 128 words long. The page is selected by bit 8 of 0xA4. Although this data must be written in pages, the internal core handles filters that exceed the length of 128 taps. Therefore, the full length of the data RAM may be used as the filter length (160 taps).

The RCF stores the data from the CIC5 into a 160x40 RAM. 160x20 is assigned to I data and 160x20 is assigned to Q data. The RCF uses the RAM as a circular buffer, so that it is difficult to know in which address a particular data element is stored.

When the RCF is triggered to calculate a filter output, it starts by multiplying the oldest value in the data RAM by the first coefficient, which is pointed to by the RCF Coefficient Offset Register (0xA3). This value is accumulated with the products of newer data words multiplied by the subsequent locations in the coefficient RAM until the coefficient address RCF_{OFF} +N_{taps}-1 is reached.

Table VII. Three-tap Filter

Coefficient Address	Impulse Response	Data
0	h(0)	N(0) oldest
1	h(1)	N(1)
2 =(N_{taps} - 1)	h(2)	N(2) newest

The RCF Coefficient Offset register can be used for two purposes. The main purpose of this register is allow for multiple filters to loaded into memory and selected simply by changing the offset as a pointer for rapid filter changes. The other use of this register is to form part of symbol timing adjustment. If the desired filter length is padded with zeros on the ends, then the starting point can be adjusted to form slight delays in when the filter is computed with reference to the high-speed clock. This allows for vernier adjustment of the symbol timing. Course adjustments can be made with the RCF Decimation Phase.

The output rate of this filter is determined by the output rate of the CIC5 stage and M_{RCF}.

$$f_{SAMPR} = \frac{f_{SAMP5}}{M_{RCF}}$$

RCF Output Scale Factor and Control Register

Register 0xA4 is a compound register and is used to configure several aspects of the RCF register. Bits 3-0 are used to set the scale of the fixed-point output mode. This scale value may also be used to set the floating-point outputs in conjunction with bit 6 of this register.

Bits 4 and 5 determine the output mode. Mode 00 sets the chip up in fixed-point mode. The number of bits is determined by the serial port configuration. See serial port configuration below.

Mode 01 selects floating-point mode 8+4. In this mode, an 8-bit mantissa is followed by a 4-bit exponent. In mode 1x (x is don't care), the mode is 12+4, or 12 bit mantissa and 4-bit exponent.

TableVIII. Output Mode Formats

Floating Point 12 + 4	1x
Floating Point 8 + 4	01
Fixed Point	00

Normally, the AD6652 will determine the exponent value that optimizes numerical accuracy. However, if bit 6 is set, the value stored in bits 3-0 is used to scale the output. This ensures that consistent scaling and accuracy during conditions that may warrant predictable output ranges. If bits 3-0 are represented by RCF Scale, the scaling factor in dB is given by:

$$Scaling\ Factor = (RCF\ Scale - 3) * 20\log_{10}(2)\ dB$$

For RCF Scale of 0, Scaling Factor is equal to –18.06 db and for maximum RCF Scale of 15, Scaling Factor is equal to +72.25 dB.

If bit 7 is set, the same exponent will be used for both the real and imaginary (I and Q) outputs. The exponent used will be the one that prevents numeric overflow at the expense of small signal accuracy. However, this is seldom a problem as small numbers would represent 0 regardless of the exponent used.

Bit 8 is the RCF bank select bit used to program the register. When this bit is 0, the lowest block of 128 is selected (taps 0 through 127). When high, the highest block is selected (taps 128 through 255). It should be noted that while the chip is computing filters, tap 127 is adjacent to 128 and there are no paging issues.

Bit 9 Selects where the input to each RCF originates. If bit 9 is clear, then the RCF input comes from the CIC5 normally associated with the RCF. If however, the bit is set, then the input comes from CIC5 channel 1. The only exception is channel 1, which uses the output of CIC5 channel 0 as its alternate. Using this feature, each RCF can either operate on its own channel data or be paired with the RCF of channel 1. The RCF of channel 1 can also be pared with channel 0. This control bit is used with poly-phase distributed filtering.

If bit 10 is clear, the AD6652 channel operates in normal mode. However, if bit 10 is set, then the RCF is bypassed to Channel BIST. See BIST (Built In Self Test) section for more details.

INTERPOLATING HALF BAND FILTERS

The AD6652 has two interpolating half band finite impulse response filters that immediately precede the two digital AGCs and after the four RCF channel outputs. Each interpolating half band takes 16-bit I and 16-bit Q data from the preceding RCF and outputs 16-bit I and 16-bit Q to the AGC. The half band and AGC operate independently of each other, so the AGC can be bypassed, in which case the output of the half band is sent directly to the output data port. The half bands also operate independent of each other -- either one can be enabled or disabled. The control register for half band A is at address 0x08 and for half band B is at address 0x09.

Halfband filters also perform the function of interleaving data from various RCF channel outputs prior to the actual function of interpolation. This interleaving of data is allowed even when the actual function of Halfband Filter is bypassed. This feature allows for the usage of multiple channels (implementing a polyphase filter) on the AD6652 to process a single carrier. Either RCF phase decimation of the Start Hold-Off Counter for the channels are used to process one CDMA2000 carrier, RCF filters for both the channels should be 180° out of phase. This can be done using RCF phase decimation or an appropriate Start Hold-Off Counter followed by appropriate NCO phase offsets.

Half band A can listen to all 4 channels: channels 0, 1, 2, and 3; channel 0 and 1; or only channel 0. Half band B can listen to channels 2 and 3,or only channel 2. Each half band interleaves the channels specified in its control register and interpolates by two on the combined data from those channels. For one channel running at twice the chip rate, the halfband can be used to output channel data at 4x the chip rate.The frequency response of the interpolating halfband FIR is shown in Figure 31.

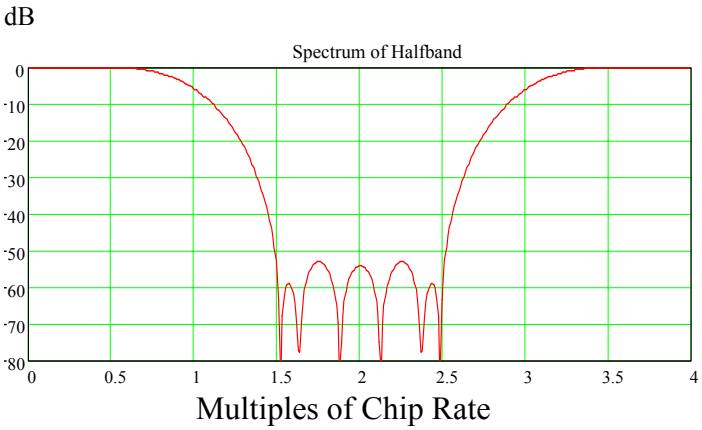


Figure 31. Interpolating Halfband Frequency Response

The SNR of the interpolating halfband is around –149.6 dB. The highest error spurs due to fixed-point arithmetic are around –172.9 dB. The coefficients of the 13-tap interpolating halfband FIR are given in the table IX.

0
14
0
-66
0
309
512
309
0
-66
0
14
0

TableIX. Halfband Coefficients

AUTOMATIC GAIN CONTROL

The AD6652 is equipped with two independent automatic gain control (AGC) loops for direct interface with a RAKE receiver. Each AGC circuit has 96dB of range. It is important that the decimating filters of the AD6652 preceding the AGC reject undesired signals, so that each AGC loop is only operating on the carrier of interest and carriers at other frequencies do not affect the ranging of the loop.

The AGC compresses the 23-bit complex output from the interpolating half band filter into a programmable word size of 4-8, 10, 12 or 16 bits. Since the small signals from the lower bits are pushed in to higher bits by adding gain, the clipping of the lower bits does not compromise the SNR of the signal of interest. The AGC maintains a constant mean power on the output despite the level of the signal of interest, allowing operation in environments where the dynamic range of the signal exceeds the dynamic range of the output resolution.

The AGC and the interpolation filters are not tied together and any one or both of them can be selected without the other. The AGC section can be bypassed if desired, by setting bit 0 of the AGC control word. When bypassed the I/Q data is still clipped to a desired number of bits and a constant gain can be provided through the AGC Gain multiplier.

There are three sources of error introduced by the AGC function: underflow, overflow, and modulation. Underflow is caused by truncation of bits below the output range. Overflow is caused by clipping errors when the output signal exceeds the output range. Modulation error occurs when the output gain varies during the reception of a data.

The desired signal level should be set based on the probability density function of the signal so that the errors due to underflow and overflow are balanced. The gain and damping values of the loop filter should be set so that the AGC is fast enough to track long term amplitude variations of the signal that might cause excessive underflow or overflow, but slow enough to avoid excessive loss of amplitude information due to the modulation of the signal.

The AGC Loop

The AGC loop is implemented using a log-linear architecture. It contains four basic operations: power calculation, error calculation, loop filtering and gain multiplication.

The AGC can be configured to operate in one of the two modes: desired signal level mode or desired clipping level mode as set by bit 4 of AGC control word (0x0A, 0x12). The AGC adjusts the gain of the incoming data according to how far it is from a given desired signal level or desired clipping level, depending on the mode of operation selected. Two data paths to the AGC loop are provided: one, before the clipping circuitry and one after the clipping circuitry as shown in figure 34. For Desired Signal level mode, only the I/Q path from before the clipping is used. For Desired Clipping level mode, the difference of the I/Q signals from before and after the clipping circuitry is used.

Desired Signal Level Mode

In this mode of operation, the AGC strives to maintain the output signal at a programmable set level. This mode of operation is selected by putting a value of zero in bit 4 of AGC control word (0x0A, 0x12). First, the loop finds the square (or power) of the incoming complex data signal by squaring I and Q and adding them. This operation is implemented in exponential domain using 2^x (power of 2).

The AGC loop has an average and decimate block. This average and decimate operation takes place on power samples and before the square root operation. This block can be programmed to average 1-16384 power samples and the decimate section can be programmed to update the AGC once every 1-4096 samples. The limitation on the averaging operation is that the number of averaged power samples should be a multiple of the decimation value (1x, 2x, 3x or 4x times).

The averaging and decimation effectively means the AGC can operate over averaged power of 1-16384 output samples. The choice of updating the AGC once every 1-4096 samples and operating on average power facilitates the implementation of loop filter with slow time constants, where the AGC error converges slowly and makes infrequent gain adjustments. It would also be useful in scenarios where the user wants to keep the gain scaling constant over a frame of data (or a stream of symbols).

Due to the limitation on the number of average samples to be a multiple of decimation value, only the multiple number 1, 2, 3 or 4 is programmed. This number is programmed in bits 1,0 of 0x10 and 0x18 registers. These averaged samples are then decimated with decimation ratios programmable from 1 to 4096. This decimation ratio is defined in 12-bit registers 0x11 and 0x19.

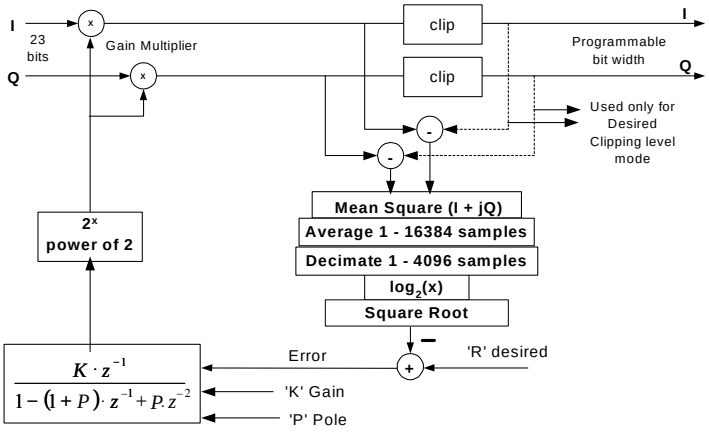


Figure 32: Block Diagram of the AGC

The average and decimate operations are tied together and implemented using a first-order CIC filter and some FIFO registers. There is a gain and bit growth associated with CIC filters and these depend on the decimation ratio. To compensate for the gain associated with these operations attenuation scaling is provided before the CIC filter.

This scaling operation accounts for the division associated with averaging operation as well as the traditional bit growth in CIC filters. Since this scaling is implemented as a bit shift operation only coarse scaling is possible. Fine scale is implemented as an offset in the Request level explained later. The attenuation scaling S_{CIC} is programmable from 0 to 14 using 4-bits of 0x10 and 0x18 registers and is given by:

$$S_{CIC} = ceil[\log_2(M_{CIC} * N_{avg})]$$

where, M_{cic} is the decimation ratio (1-4096) and N_{avg} is the number of averaged samples programmed as a multiple of decimation ratio (1, 2, 3 or 4).

For example if a decimation ratio M_{cic} is 1000 and N_{avg} is selected to be 3 (decimation of 1000 and averaging of 3000 samples), then the actual gain due to averaging and decimation is 3000 or 69.54dB ($=\log_2(3000)$). Since attenuation is implemented as a bit shift operation, only multiples of 6.02dB attenuations are possible. S_{CIC} in this case is 12 corresponding to 72.24dB. This way S_{CIC} scaling always attenuates more than sufficient to compensate for the gain changes in average and decimate sections and hence prevent overflows in the AGC loop. But it is also evident that the CIC scaling is inducing a gain error (difference between gain due to CIC and attenuation provided) of up to 6.02dB. This error should be compensated for in the Request signal level as explained below.

Logarithm to the base 2 is applied to the output from the average and decimate section. These decimated power samples (in logarithmic domain) are converted to RMS signal samples by applying a square root. This square root is implemented using a simple shift operation. The RMS samples so obtained are subtracted from the Request signal level 'R' specified in registers (0x0B, 0x14) leaving an error term to be processed by the loop filter, G(z).

The user sets this programmable Request signal level 'R' according to the output signal level that he desires. The Request signal level 'R' is programmable from –0 to –23.99dB in steps of 0.094dB.The Request signal level should also compensate for error, if any, due to the CIC scaling as explained previously. Hence the Request signal level is offset by the amount of error induced in CIC, given by,

$$Offset = 20 * \log_{10}(M_{CIC} * N_{avg}) - S_{CIC} * 6.02$$

where, the offset is in dB. Continuing with the previous example this offset is given by, Offset = 72.24 – 69.54 = 2.7dB. So the Request Signal level is given by:

$$R = ceil\left[\frac{(DSL - Offset)}{0.094}\right] * 0.094$$

where, R is the Request signal level and DSL (Desired Signal Level) is the output signal level that the user desires. So in the previous example if the desired signal level is –13.8dB, the Request level 'R' is programmed to be –16.54dB.

The AGC provides a programmable second order loop filter. The programmable parameters gain 'K' and pole 'P' completely define the loop filter characteristics. The error term after subtracting the Request signal level is processed by the loop filter, G(z). The open loop poles of the second order loop filter are '1' and 'P' respectively. The loop filter parameters pole 'P' and gain 'K', allow adjustment of the filter time constant that determines the window for calculating the peak-to-average ratio.

The open loop transfer function for the filter including the gain parameter is given below.

$$G(z) = \frac{Kz^{-1}}{1-(1+P)z^{-1}+Pz^{-2}}$$

If the AGC is properly configured (in terms of offset in Request level) then there are no gains except the filter gain K. Under these circumstances a closed loop expression for the AGC loop is possible and is given by

$$G_{closed}(z) = \frac{G(z)}{1+G(z)} = \frac{Kz^{-1}}{1+(K-1-P)z^{-1}+Pz^{-2}}$$

The gain parameter 'K' and pole 'P' are programmable through registers (0x0E and 0x0F respectively, for AGC channel A and B) from 0 to 0.996 in steps of 0.0039 using 8-bit representation. Though the user defines the open loop pole 'P' and gain 'K', they will directly impact the placement of the closed loop poles and filter characteristics. These closed loop poles P_1, P_2 are the roots of the denominator of the above closed loop transfer function and are given by.

$$P_1, P_2 = \frac{(1+P-K)+\sqrt{(1+P-K)^2-4P}}{2}$$

Typically the AGC loop performance is defined in terms of its time constant or settling time. In such a case the closed loop poles should be set to meet the time constants required by the AGC loop. The following relation between time constant and closed loop poles can be used for this purpose.

$$P_{1,2} = \exp\left[\frac{M_{CIC}}{SampleRate * \tau_{1,2}}\right]$$

where, $\tau_{1,2}$ are the time constants corresponding to the poles $P_{1,2}$, and exp denotes the inverse of the natural log. The time constants can also derived from settling times as given below,

$$\tau = \frac{2\%\ \text{settling time}}{4} \text{ or } \frac{5\%\ \text{settling time}}{3}$$

M_{CIC} (CIC decimation is from 1 to 4096), and either the settling time or time constant should be chosen by the user. The Sample rate is the combined sample rate of all the interleaved channels coming into the AGC / halfband interpolated filters. If 2 channels are being used to process one carrier of UMTS at 2x chip rate, then each channel works at 3.84MHz and the combined sample rate coming into the halfband interpolated filters is 7.68Msps. This rate should be used in the calculation of poles in the above equation.

The loop filter output corresponds to the Signal gain that is updated by the AGC. Since all computation in the loop filter is done in logarithmic domain (to the base 2) of the samples, the Signal Gain is generated using the exponent (power of 2) of the loop filter output.

The gain multiplier gives the product of the Signal Gain with both the I and Q data entering the AGC section. This Signal Gain is applied as a coarse 4-bit scaling and then a fine scale 8-bit multiplier. Hence the applied signal gain is between –48.16dB to 48.13dB in steps of 0.024dB. Initial value for Signal Gain is programmable using the registers 0x0D and 0x15 for AGC A and AGC B respectively.

The products of the gain multiplier are the AGC scaled outputs have 19-bit representation. These are in turn used as I and Q for calculating the power and AGC error and loop filtered to produce Signal Gain for next set of samples. These AGC scaled outputs can be programmed to have 4, 5, 6, 7, 8, 10, 12, or 16 bit widths using the AGC control word (0x0A, 0x12). The AGC scaled outputs are truncated to required bit widths using the clipping circuitry as shown in the block diagram.

Open Loop Gain Setting: If filter gain K occupies only one LSB or 0.0039, then during the multiplication with error term, errors of up to 6.02dB could be truncated. This truncation is due to the lower bit widths available in the AGC loop. If filter gain K were the maximum value, truncated errors would be a less than 0.094dB (equivalent to 1 LSB of Error term representation). Generally a small filter gain is used to achieve a large time constant loop (or slow loops), but in this case it would cause large errors to go undetected. Due this peculiarity, the designers recommend that if a user wants slow AGC loops they rather use fairly high values for filter gain K and then use CIC decimation to achieve a slow loop. In this way the AGC loop will make large infrequent gain changes compared to small and frequent gain changes as in the case of normal small gain loop filter. However though the AGC loop makes large infrequent gain changes a slow time constant is still achieved and there is lesser truncation of errors.

Average Samples Setting: Though it is complicated to express the exact effect of the number of averaging samples, thinking intuitively it has a smoothing effect on the way the AGC loop attacks a sudden increase or a spike in the signal level. If averaging of 4 samples is used, the AGC will attack a sudden increase in signal level more slowly compared to no averaging. The same would apply to the manner in which the AGC would attack a sudden decrease in the signal level.

Desired Clipping Level Mode

As noted previously, each AGC can be configured so that the loop locks on to a desired clipping level or a desired

signal level. The Desired Clipping Level mode can be selected by setting the bit 4of individual AGC control words (0x0A, 0x12). For signals that tend to exceed the bounds of the peak-to-average ratio, desired clipping level option allows a way to keep from truncating those signals and still provide an AGC that attacks quickly and settles to the desired output level. The signal path for this mode of operation is shown with broken arrows in the block diagram and the operation is similar to the desired signal level mode.

First, the data from the gain multiplier is truncated to a lower resolution (4, 5, 6, 7, 8, 10, 12, or 16 bits) as set by the AGC control word. An error term (both I and Q) is generated that is the difference between the signals before and after truncation. This term is passed to the complex squared magnitude block, for averaging and decimating the update samples and taking their square root to find RMS samples as in desired signal level mode. In place of the Request desired signal level, a desired clipping level is subtracted, leaving an error term to be processed by the second order loop filter. The rest of the loop operates the same way as the desired signal level mode. This way the truncation error is calculated and the AGC loop operates to maintain a constant truncation error level.

Apart from bit 4 of the AGC control words, the only register setting changes compared to the Desired Signal level mode is that the Desired Clipping level is stored in the AGC Desired Level registers (0x0C, 0x15) instead of the Request Signal level (as in Desired Signal Level mode).

Synchronization

In scenarios where AGC output is connected to a RAKE receiver, the RAKE receiver can synchronize the average and update section to update the average power for AGC error calculation and loop filtering. This external sync signal synchronizes the AGC changes to RAKE receiver and makes sure that the AGC gain word does not change over a symbol period and hence more accurate estimation. Such synchronization can be accomplished by setting the appropriate bits of the AGC control register.

When the channel comes out of sleep, it loads the AGC hold off counter value and starts counting down, clocked by the Master clock. When this counter reaches zero, the CIC filter of the AGC starts decimation and updates the AGC loop filter based on the CIC decimation value set.

Further whenever the user wants to synchronize the start of decimation for a new update sample an appropriate hold-off value can be set in AGC Hold-off counter (0x0B, 0x13) and the Sync now bit (bit 3) in the AGC control word is set. Upon setting this bit the hold-off counter value is counted down and a CIC decimated value is updated on the count of zero.

Along with updating a new value, the CIC filter accumulator can be reset if Init on Sync bit (bit 2) of the AGC control word is set. Each sync will initiate a new sync signal unless First sync only bit (bit 1) of the AGC control word is set. If this bit is not set, again the hold-off counter is loaded with the value in the Hold-off register to count down and repeat the same process. These additional features make the AGC synchronization more flexible and applicable to varied circumstances.

Addresses 0x0A – 0x11 have been reserved for configuring AGC A and addresses 0x12 – 0x19 have been reserved for configuring AGC B. The register specifications are detailed in the "Memory Map for Output Port Control Registers" section of this data sheet.

USER CONFIGURABLE BUILT IN SELF TEST (BIST)

The AD6652 includes two built in test features to test the integrity of each channel. The first is a RAM BIST (Built In Self Test) and is intended to test the integrity of the high-speed random access memory within the AD6652. The second is Channel BIST, which is designed to test the integrity of the main signal paths of the AD6652. Each BIST function is independent of the other meaning that each channel can be tested independently at the same time.

RAM BIST

The RAM BIST can be used to validate functionality of the on-chip RAM. This feature provides a simple pass/fail test, which will give confidence that the channel ram is operational. The following steps should be followed to perform this test.

- The Channels to be tested should be put into Sleep mode via the external address register 0x011.
- The RAM BIST Enable bit in the RCF register xA8 should be set high.
- Wait 1600 clock cycles.
- Register 0xA8 should be read back. If bit 0 is high, the test is not yet complete. If bit 0 is low, the test is complete and bits 1 and 2 indicate the condition of the internal ram. If bit 1 is high, then CMEM is bad. If bit 2 is high then DMEM is bad.

XA8	Coefficient MEM	Data MEM
XX1	Test incomplete	Test incomplete

000	PASS	PASS
010	FAIL	PASS
100	PASS	FAIL
110	FAIL	FAIL

Table X8. BIST Register 0xA8

CHANNEL BIST

The Channel BIST is a thorough test of the selected AD6652 signal path. With this test mode, it is possible to use externally supplied vectors or an internal pseudo-random generator. An error signature register in the RCF monitors the output data of the channel and is used to determine if the proper data exits the RCF. If errors are detected then each internal block may be bypassed and another test can be run to debug the fault. The I and Q paths are tested independently. The following steps should be followed to perform this test.

- The Channels to be tested should be configured as required for the application setting the decimation rates, scalars and RCF coefficients.
- The Channels should remain in the Sleep mode.
- The Start Hold-Off counter of the channels to be tested should be set to 1.
- Memory location 0xA5 and 0xA6 should be set to 0.
- The Channel BIST located at 0xA7 should be enabled by setting bits 19-0 to the number of RCF outputs to observe.
- Bit 4 of external address register 5 should be set high to start the soft sync.
- Set the SYNC bits high for the channels to be tested.
- Bit 6 must be set to 0 to allow the user to provide test vectors. The internal pseudo-random number generator may also be used to generate an input sequence by setting bit 7 high.
- An internal Full Scale sine wave can be inserted when bit 6 is set to 1 and bit 7 is cleared.
- When the SOFT_SYNC is addressed, the selected channels will come out of the sleep mode and processing will occur.
- If the user is providing external vectors, then the chip may be brought out of Sleep mode by one of the other methods.
- After a sufficient amount of time the Channel BIST Signature registers 0xA5 and 0xA6 will contain a numeric value that can be compared to the expected value for a known good AD6652 with the exact same configuration. If the values are the same, then there is a very low probability that there is an error in the channel.

CHIP SYNCHRONIZATION

Two types of synchronization can be achieved with the AD6652. These are Start and Hop. Each is described in detail below. The synchronization is accomplished with the use of a shadow register and a hold off counter. See Figure 33 below for a simplistic schematic of the NCO shadow register and NCO Freq Hold aOff counter to understand basic operation. Enabling the clock (AD6652 DCLK) for the hold off counter can occur with either a Soft_Sync (via the micro port), or a Pin Sync (via any of the four AD6652 SYNC pins A, B, C, and D). The functions that include shadow registers to allow synchronization are Start and Hop (NCO Frequency).

Start

Start refers to the start-up of an individual channel, chip, or multiple chips. If a channel is not used, it should be put in the Sleep Mode to reduce power dissipation. Following a hard reset (low pulse on the AD6652 /Reset pin), all channels are placed in the Sleep Mode. Channels may also be manually put to sleep by writing to the mode register controlling the sleep function.

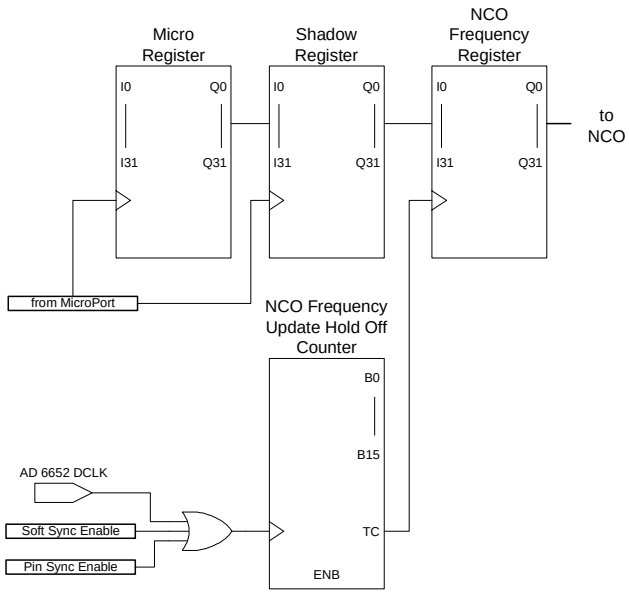


Figure 33. NCO Shadow Register and Hold Off Counter

Start With No Sync

If no synchronization is needed to start multiple channels or multiple AD6652s, the following method should be used to initialize the device.

1. To program a channel, it must first be set to Sleep Mode (bit high) (Ext Address 3). All appropriate control and memory registers (filter) are then loaded. The Start Update Hold Off Counter (0x83) should be set to 1.

2. Set the Sleep bits low (Ext Address 3). This enables the channel. The channel must the Sleep Mode low to activate a channel.

Start With Soft Sync

The AD6652 includes the ability to synchronize channels or chips under microprocessor control. One action to synchronize is the start of channels or chips. The Start Update Hold Off Counter (0x83) in conjunction with the Start bit and Sync bit (Ext Address 5) allow this synchronization. Basically the Start Update Hold Off Counter delays the Start of a channel(s) by its value (number of AD6652 CLKs. The following method is used to synchronize the start of multiple channels via microprocessor control.

1. Set the appropriate channels to sleep mode (a hard reset to the AD6652 Reset pin brings all 4 channels up in sleep mode).
2. Note that the time from when the RDY (pin 57) goes high to when the NCO begins processing data is the contents of the Start Update Hold Off Counter(s) (0x83) + 6 master clock cycles.
3. Write the Start Update Hold Off Counter(s) (0x83) to the appropriate value (greater than 1 and less than 2^16-1). If the chip(s) is not initialized, all other registers should be loaded at this step.
4. Write the Start bit and the SYNC bit high (Ext Address 5).
5. This starts the Start Update Hold Off Counter counting down. The counter is clocked with the AD6652 DCLK signal. When it reaches a count of one the Sleep bit of the appropriate channel(s) is set low to activate the channel(s).

Start With Pin Sync

The AD6652 has 4 Sync pins A, B, C and D that can be used to provide for very accurate synchronization channels. Each channel can be programmed to look at any of the 4 sync pins. Additionally, any or all channels can monitor a single Sync pin or each can monitor a separate pin, providing complete flexibility of synchronization. Synchronization of Start with one of the external signal is accomplished with the following method.

1. Set the appropriate channels to sleep mode (a hard reset to the AD6652 Reset pin brings all 4 channels up in sleep mode).
2. Note that the time from when the SYNC pin goes high to when the NCO begins processing data is the contents of the Start Update Hold Off Counter(s) (0x83) + 3 master clock cycles.
3. Write the Start Update Hold Off Counter(s) (0x83) to the appropriate value (greater than 1 and less than 2^16-1). If the chip(s) is not initialized, all other registers should be loaded at this step.
4. Set the Start on Pin Sync bit and the appropriate Sync Pin Enable high (Ext Address 4) (A, B, C or D).
5. When the Sync pin is sampled high by the AD6652 DCLK this enables the count down of the Start Update Hold Off Counter. The counter is clocked with the AD6652 DCLK signal. When it reaches a count of one the Sleep bit of the appropriate channel(s) is set low to activate the channel(s).

Hop

Hop is a jump from one NCO frequency to a new NCO frequency. This change in frequency can be synchronized via microprocessor control (Soft Sync) or an external Sync signal (PIN Sync) as described below.

To set the NCO frequency without synchronization the following method should be used.

Set Freq No Hop

1. Set the NCO Freq Hold Off counter to 0.
2. Load the appropriate NCO frequency. The new frequency will be immediately loaded to the NCO.

Hop With Soft Sync

The AD6652 includes the ability to synchronize a change in NCO frequency of multiple channels or chips under microprocessor control. The NCO Freq Hold Off counter (0x84) in conjunction with the Hop bit and the Sync bit (Ext Address 4) allow this synchronization. Basically the NCO Freq Hold Off counter delays the new frequency from being loaded into the NCO by its value (number of AD6652 CLKs). The following method is used to synchronize a hop in frequency of multiple channels via microprocessor control.

1. Note that the time from when the RDY (pin 57) goes high to when the NCO begins processing data is the contents of the NCO Freq Hold Off counter (0x84) + 7 master clock cycles.
2. Write the NCO Freq Hold Off (0x84) counter to the appropriate value (greater than 1 and less then 2^16-1).
3. Write the NCO Frequency register(s) to the new desired frequency.
4. Write the Hop bit and the Sync(s) bit high (Ext Address 4).
5. This starts the NCO Freq Hold Off counter counting down. The counter is clocked with the AD6652 DCLK signal. When it reaches a count of one the new frequency is loaded into the NCO.

Hop With Pin Sync

The AD6652 include 4 Sync pins to provide the most accurate synchronization, especially between multiple AD6652s. Synchronization of Hopping to a new NCO frequency with an external signal is accomplished with the following method.

1. Note that the time from when the SYNC pin goes high to when the NCO begins processing data is the contents of the NCO Freq Hold Off counter (0x84) + 5 master clock cycles.
2. Write the NCO Freq Hold Off counter(s) (0x84) to the appropriate value (greater than 1 and less than 2^16-1).
3. Write the NCO Frequency register(s) to the new desired frequency.
4. Set the Hop on Pin Sync bit and the appropriate Sync Pin Enable high.
5. When the selected Sync pin is sampled high by the AD6652 DCLK this enables the count down of the NCO Freq Hold Off counter. The counter is clocked with the AD6652 DCLK signal. When it reaches a count of one the new frequency is loaded into the NCO.

PARALLEL OUTPUT PORTS

The AD6652 incorporates two independent 16-bit parallel ports for output data transfer. To minimize package ball count, the eight LSBs of each 16-bit port are shared with their respective DSP Link Port data bits (see Figure 34). This means that an output port can transmit 16-bit parallel data or 8-bit link port data, but not both. Transmitting both Link and Parallel data simultaneously requires that the second AD6652 output port be configured for that purpose.

Each parallel output port has six data sources routed to it (see front page "FUNCTIONAL BLOCK DIAGRAM"):

- Non-interpolated RAM Coefficient FIR Filter output data from channels 1, 2, 3 and 4
- Interpolated, Interleaved and/or AGC modified Channel A data
- Interpolated, Interleaved and/or AGC modified Channel B data

Any of the six sources may be output on any port(s). A port may be configured to output parallel data or DSP link data. Output port control registers (Table XVI) perform these multiplexing & selection tasks.

Parallel port configuration is specified by accessing Port Control Register addresses 0x18 and 0x1A for parallel ports A and B, respectively. Port clock Master/Slave mode (described later) is configured using the Port Clock Control register at address 0x1C. Note that to access these registers, bit 5 (Access Port Control Registers) of external address 3 (SLEEP register) must be set. The address is then selected by programming the CAR register at external address 6.

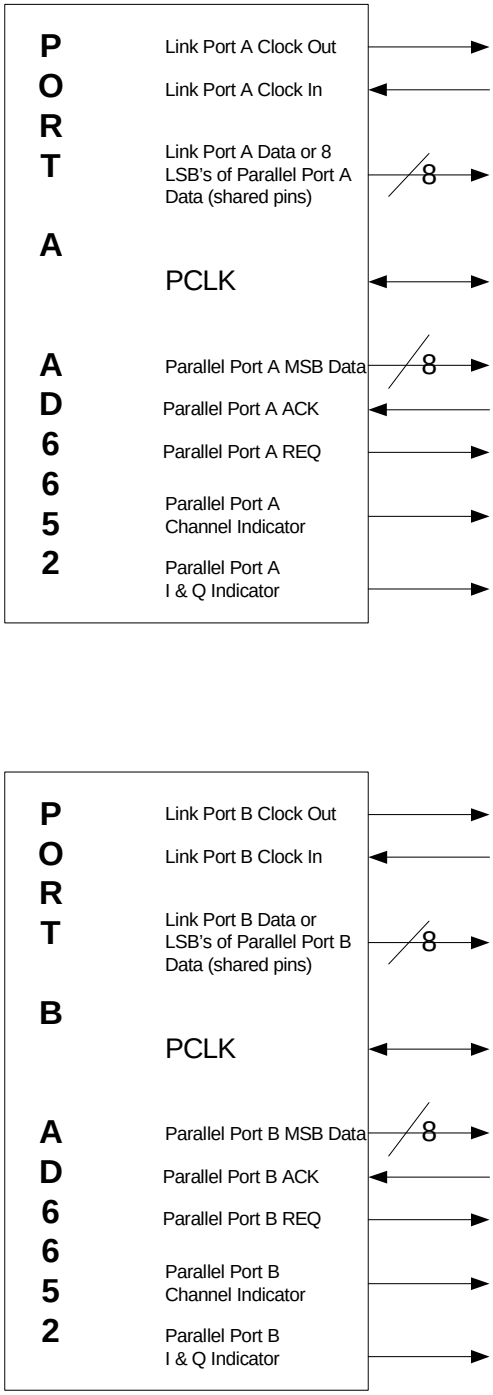


Figure 34. Output Port Configuration

The parallel ports are enabled by setting bit 7 of the Link Control registers at addresses 0x19 and 0x1B for ports A and B, respectively.Each parallel port is capable of operating in either Channel mode or AGC mode. Each mode is described in detail below.

Channel mode

Parallel port Channel mode is selected by setting bit 0 of addresses 0x18 and 0x1A for parallel ports A and B, respectively. In Channel mode, I and Q words from each channel is directed to the parallel port, bypassing the AGC. The specific channels output by the port is selected by setting bits 1 through 4 of Input Port Control Register 0x18 (port A) and 0x1A (port B).

Channel mode provides two data formats. Each format requires a different number of parallel port clock (PCLK) cycles to complete the transfer of data. In each case, each data element is transferred during one PCLK cycle. See Figures 35 and 36, which present Channel mode parallel port timing.

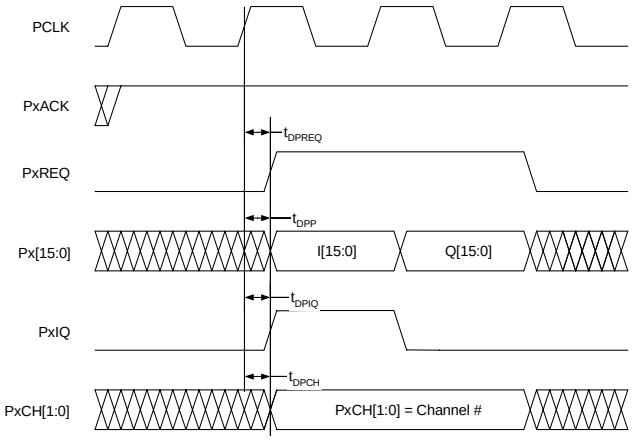


Figure 35. Channel mode interleaved format.

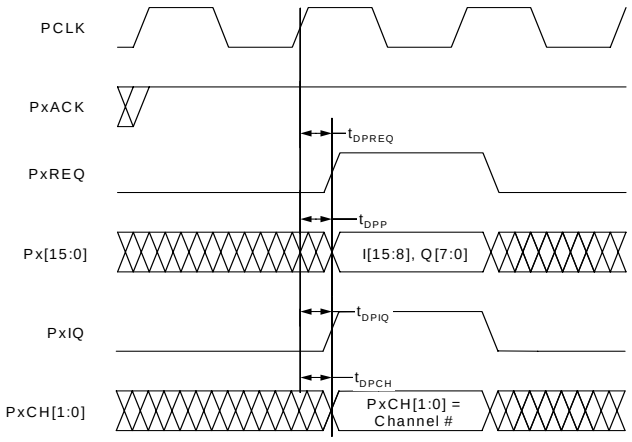


Figure 36. Channel mode 8I/8Q parallel format.

The 16-bit Interleaved format provides I and Q data for each output sample on back-to-back PCLK cycles. Both I and Q words consist of the full port width of 16 bits. Data output is triggered on the rising edge of PCLK when both REQ and ACK are asserted. I data is output during the first PCLK cycle; and the PAIQ and PBIQ output indicator pins are set high to indicate that I data is on the bus. Q data is output during the subsequent PCLK cycle; and the PAIQ and PBIQ output indicator pins are low during this cycle.

The 8-bit Concurrent format provides 8 bits of I data and 8 bits of Q data simultaneously during one PCLK cycle, also triggered on the rising edge of PCLK. The I byte occupies the most significant byte of the port, while the Q byte occupies the least significant byte. The PAIQ and PBIQ output indicator pins are set high during the PCLK cycle. Note that if data from multiple channels are output consecutively, the PAIQ and PBIQ output indicator pins will remain high until data from all channels has been output.

The PACH[1:0] and PBCH[1:0] pins provide a 2-bit binary value indicating the source channel of the data currently being output.

Care should be taken to read data from the port as soon as possible. If not, the sample will be overwritten when the next new data sample arrives. This occurs on a per-channel basis; i.e., a channel 0 sample will only be overwritten by a new channel 0 sample, etc.

The order of data output is dependent on when data arrived at the port, which is is a function of total decimation rate, Start-Holdoff values, etc. Priority order is, from highest to lowest, channels 0, 1, 2, 3.

AGC mode
Parallel port Channel mode is selected by clearing bit 0 of addresses 0x18 and 0x1A for parallel ports A and B, respectively. I and Q data output in AGC mode are output from the AGC, not the individual channels. Each AGC receives data from only two AD6652 channels; AGC A accepts data from channels 0 and 1, while AGC B accepts data from channels 2 and 3. Each pair of channels is required to be configured such that the generation of output samples from the channels is out of phase (by typically 180 degrees). Each parallel port can provide data from either one or both AGCs. Bits 1 and 2 of register addresses 0x18 (port A) and 0x1A (port B) control the inclusion of data from AGCs A and B, respectively.

AGC mode provides only one I&Q format, which is similar to the 16-bit Interleaved format of Channel mode. When both REQ and ACK are asserted, the next rising edge of PCLK triggers the output of a 16-bit AGC I word for one PCLK cycle. The PAIQ and PBIQ output indicator pins are high during this cycle, and is low otherwise. A 16 bit AGC Q word is provided during the subsequent PCLK cycle. If the AGC Gain word has been updated since the last sample, a 16-bit Gain word is provided during the PCLK cycle following the Q word.

The data provided by the PACH[1:0] and PBCH[1:0] pins in AGC mode is different than that provided in Channel mode. In AGC mode, PACH[0] and PBCH[0] indicate the AGC source of the data currently being output (0=AGC A, 1=AGC B). PACH[1] and PBCH[1] indicate whether the current data is and I/Q word or an AGC Gain word (0=I/Q word, 1=AGC Gain word). The two AGC modes are shown below in Figures 39 and 40.

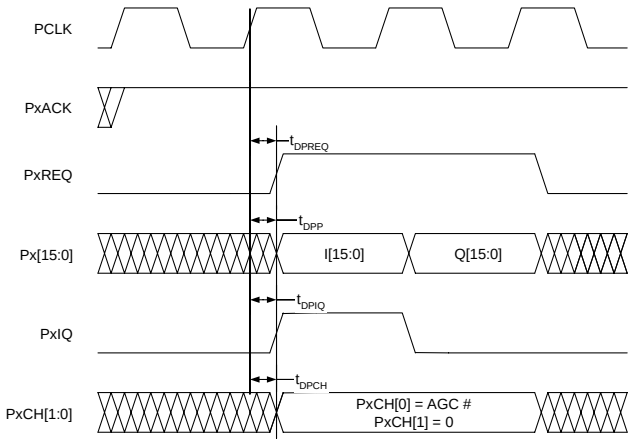


Figure 37. AGC with no gain word.

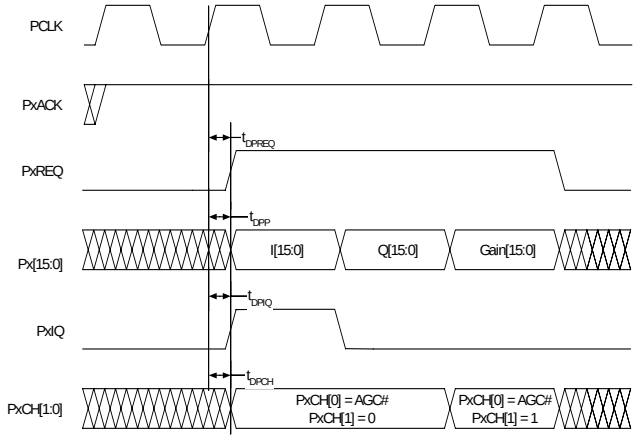


Figure 38. AGC with gain word.

Master/Slave PCLK modes
The parallel ports may operate in either Master or Slave mode. The mode is set via the Port Clock Control register (address 0x1C). The parallel ports power up in Slave mode to avoid possible contentions on the PCLK pin.

In Master mode, PCLK is an output whose frequency is the AD6652 clock frequency divided by the PCLK divisor. Since values for PCLK_divisor[2:1] can range from 0 to 3, integer divisors of 1 to 4, respectively, can be obtained. Since the maximum clock rate of the AD6652 is 65 MHz, the highest PLCK rate in Master mode is also 65 MHz. Master mode is selected by setting bit 0 of address 0x1C.

In Slave mode, external circuitry provides the PCLK signal. Slave-mode PCLK signals may be either synchronous or asynchronous. The maximum Slave-mode PCLK frequency is 100 MHz.

Parallel Port Pin Functionality
The following describes the functionality of the pins used by the parallel ports.

PCLK: Input/output. As an output (Master mode), the maximum frequency is DCLK/N, where DCLK is AD6652 clock and N is an integer divisor from 1 to 4. As an input (Slave mode), it may be asynchronous relative to the AD6652 DCLK. This pin powers up as an input to avoid possible contentions. Other port outputs change on the rising edge of PCLK.

REQ: Active HIGH output, synchronous to PCLK. A logic HIGH on this pin indicates that data is available to be shifted out of the port. A logic HIGH value remains high until all pending data has been shifted out.

ACK: Active HIGH asynchronous input. Applying a logic LOW on this pin inhibits parallel port data shifting.

Applying a logic HIGH to this pin when REQ is high causes the parallel port to shift out data according the programmed data mode. ACK is sampled on the rising edge of PCLK. Assuming REQ is asserted, the latency from the assertion of ACK to data appearing at the parallel port output is no more than 1.5 PCLK cycles (see Figure 13). ACK may be held high continuously; in this case, when data becomes available, shifting begins 1 PCLK cycle after the assertion of REQ (see Figure 37).

PAIQ, PBIQ: High whenever I data is present on the port output, low otherwise.

PACH[1:0], PBCH[1:0]: These pins serve to identify data in both of the data modes. In Channel mode, these pins form a 2-bit binary number identifying the source channel of the current data word. In AGC mode, [0] indicates the AGC source (0=AGC A, 1=AGC B), and [1] indicates whether the current data word is I/Q data (0) or a Gain word (1).

PA[15:0], PB[15:0]: Parallel output data ports. Contents and format are mode-dependent.

LINK PORT

The AD6652 has two configurable link ports that provide a seamless data interface with the TigerSHARC DSP. Each link port allows the AD6652 to write output data to the receive DMA channel in the TigerSHARC for transfer to memory. Since they operate independently of each other, each link port can be connected to a different TigerSHARC or different link ports on the same TigerSHARC. The figure 39 below shows how to connect one of the two AD6652 link ports to one of the four TigerSHARC link ports. Link Port A is configured through register 0x19 and Link Port B is configured through register 0x1B.

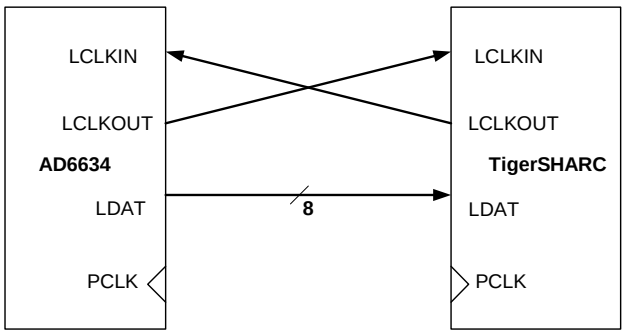


Figure 39. Link Port Connection Between AD6652 and TigerSHARC

Link Port Data Format

Each link port can output data to the TigerSHARC in 5 different formats: 2 channel, 4 channel, dedicated AGC, redundant AGC with gain, and redundant AGC without gain. Each format outputs 2 bytes of I data and 2 bytes of Q data to form a 4 byte IQ pair. Since the TigerSHARC link port transfers data in quad-word (16-byte) blocks, four IQ pair can make up one quad-word. If the channel data is selected (Bit 0 = 0), then 4-byte IQ words of the four channels can be output in succession or alternating channel pair IQ words can be output. The following figures 40 and 41 show the quad-word transmitted for each scenario with corresponding register values for configuring each link port.

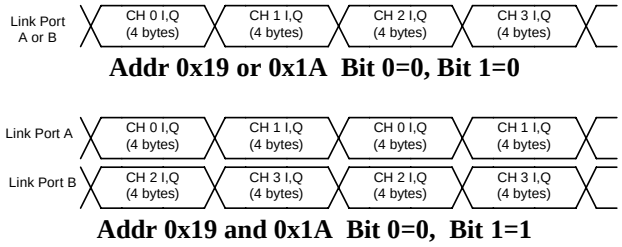


Figure 40. Link Port Data from RCF

If AGC output is selected (Bit 0 = 1), then gain information can be sent with the IQ pair from each AGC. Each link port can be configured to output data from one AGC or both link ports can output data from the same AGC. If both link ports are transmitting the same data, then gain data must be sent with the IQ words (Bit 2 = 0). Note that the actual AGC gain is only 2 bytes, so the link port sends 2 bytes of 0's immediately after each gain word to make a full 16-byte quad-word.

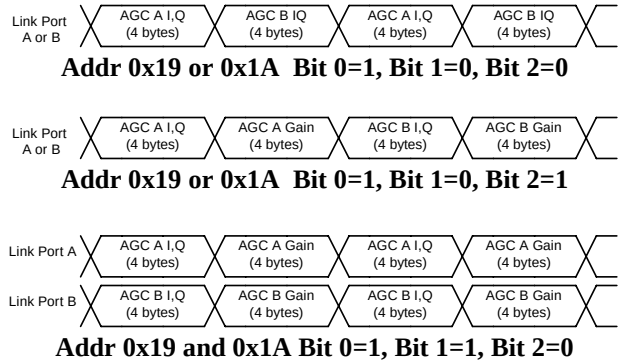


Figure 41. Link Port Data from AGC

Note that Bit 0 =1 Bit 1 = 0, and Bit 2 = 1 is not a valid configuration. Bit 2 must be set to 0, to output AGC A IQ and gain words on link port A and AGC B IQ and gain words on link port B.

Link Port Timing

Both link ports run off of PCLK, which can be externally provided to the chip (Addr 0x1C Bit 0 = 0) or generated from the master clock of the AD6652 (Addr 0x1C Bit 0 = 1). This register boots to 0 (slave mode) and allows the user to control the data rate coming from the AD6652. PCLK can be run as fast as 100 MHz.

The link port provides a 1-byte data words (LA[7:0], LB[7:0] pins) and output clocks (LACLKOUT, LBCLKOUT pins) in response to a ready signals (LACLKIN, LBCLKIN pins) from the receiver. Each link port transmits 8 bits on each edge of LCLKOUT, requiring 8 LCLKOUT cycles to complete transmission of the full 16 bytes of a TigerSHARC quad-word.

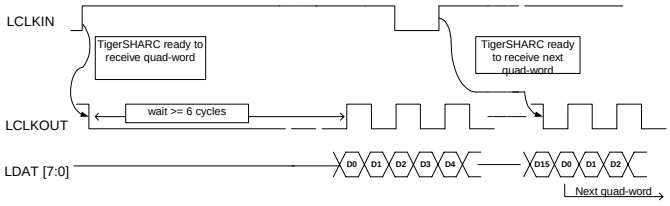


Figure 42. Link Port Data Transfer

Due to the TigerSHARC link port protocol, the AD6652 must wait at least 6 PCLK cycles after the TigerSHARC is ready to receive data, as indicated by the TigerSHARC setting the respective AD6652 LCLKIN pin high. Once the AD6652 link port has waited the appropriate number of PCLK cycles and has begun transmitting data, the TigerSHARC does a connectivity check by sending the AD6652 LCLKIN low and then high while the data is being transmitted. This tells the AD6652 link port that the TigerSHARC's DMA is ready to receive the next quad-word after completion of the current quad-word. Because the connectivity check is done in parallel to the data transmission, the AD6652 is able to stream uninterrupted data to the TigerSHARC.

The length of the wait before data transmission is a 4-bit programmable value in the link port control registers (0x19 and 0x1B bits 6-3). This value allows the AD6652 PCLK and the TigerSHARC PCLK to be run at different rates and out of phase.

$$WAIT \geq ceil\left(6 \cdot \frac{f_{LCLK\_34}}{f_{LCLK\_TSHARC}}\right)$$

WAIT ensures that the amount of time the AD6652 needs to wait to begin data transmission is at least equal to the minimum amount of time the TigerSHARC is expecting it to wait. If the PCLK of the AD6652 is out of phase with the PCLK of the TigerSHARC and the argument to the ceil() function is an integer, then WAIT must be strictly greater than the value given in the above formula. If the LCLKs are in phase, then the maximum output data rate is

$$f_{LCLK\_34} \leq \frac{15}{6} \cdot f_{LCLK\_TSHARC}$$

otherwise it is

$$f_{LCLK\_34} \leq \frac{14}{6} \cdot f_{LCLK\_TSHARC}$$

TigerSHARC Configuration

Since the AD6652 is always the transmitter in this link and the TigerSHARC is always the receiver, the following values can be programmed into the LCTL register for the link port used to receive AD6652 output data. "User" means that the actual register value depends on the user's application.

VERE	0
SPD	User
LTEN	0
PSIZE	1
TTOE	0
CERE	0
LREN	1
RTOE	1

Table XI. TigerSHARC LCTLx Register Configuration

AD6652 CHANNEL ADDRESS REGISTERS (partial listing)

Ch Address	Register	Bit Width	Comments
00-7F	Coefficient Memory(CMEM)	20	128x20-bit Memory
80	CHANNEL SLEEP	1	0: SLEEP bit from EXT_ADDRESS 3

81	Soft_Sync Control Register	2	1: Hop 0: Start
82	Pin_SYNC Control Register	3	2: First SYNC Only 1: Hop_En 0: Start_En
83	Start Hold-Off Counter	16	Start Hold-Off Value
84	NCO Frequency Hold-Off Counter	16	NCO_FREQ Hold-Off Value
85	NCO Frequency Register 0	16	NCO_FREQ[15:0]
86	NCO Frequency Register 1	16	NCO_FREQ[31:16]
87	NCO Phase Offset Register	16	NCO_PHASE[15:0]
88	NCO Control Register	9	8-7: SYNC Input Select[1:0] 6: Input Port Select B or A 5-4: Reserved, write both bits logic low 3: Clear Phase Accumulator on HOP 2: Amplitude Dither 1: Phase Dither 0: By-Pass (A-Input -> I-Path, B -> Q)
89-8F	Unused		

Table XII. Initial Channel Address Memory Map Listing

0x00-0x7F: Coefficient Memory(CMEM)
This is the Coefficient Memory(C-MEM) used by the RCF. It is memory mapped as 128 words by 20 bits. A second 128 words of RAM may be accessed via this same location by writing bit 8 of the RCF control register high at channel address 0xA4. The filter calculated will always use the same coefficients for I and Q. By using memory from both of these 128 blocks a filter up to 160 taps can be calculated. Multiple filters can be loaded and selected with a single internal access to the Coefficient Offset Register at channel address 0xA3.

0x80: Channel Sleep Register
This register contains the SLEEP bit for the Channel. When this bit is high then the channel is placed in a low power state. When this bit is low then the channel processes data. This bit can also be set by accessing the SLEEP register at external address 3. When the External SLEEP register is accessed then all four channels are accessed simultaneously and the SLEEP bits of the channels are set appropriately.

0x81: Soft_SYNC Register
This register is used to initiate SYNC events through the micro port. If the Hop bit is written high then the Hop Hold-Off Counter at address 0x84 is loaded and begins to count down. When this value reaches 1 then the NCO Frequency register used by the NCO accumulator, is loaded with the data from channel addresses 0x85 and 0x86. When the Start bit is set high then the Start Hold-Off Counter is loaded with the value at address 0x83 and begins to count down. When this value hits 1 then the Sleep bit in address 0x80 is dropped low and the channel is started.

0x82: Pin_SYNC Register
This register is used to control the functionality of the SYNC pins. Any of the four SYNC pins can be chosen and monitored by the channel. The channel can be configured to initiate either a Start or Hop SYNC event by setting the Hop or Start bit high. These bits function as enables so that when a SYNC pulse occurs then either the Start or Hop Hold-Off Counters are activated in the same manner as with a Soft_SYNC.

0x83: Start Hold-Off Counter
The Start Hold-Off Counter is loaded with the value written to this address when a Start_Sync is initiated. It can be initiated by either a Soft_SYNC or Pin_SYNC. The counter begins decrementing and when it reaches a value of 1 the channel is brought out of SLEEP and begins processing data. If the channel is already running then the phase of the filters are adjusted such that multiple AD6652s can be synchronized. A periodic pulse on the SYNC pin can be used in this way to adjust the timing of the filters with the resolution of the ADC sample clock. If this register is written to a 1 then the Start will occur immediately when the SYNC comes into the channel. If it is written to a 0 then no SYNC will occur.

0x84: NCO Frequency Hold-Off Counter

The NCO Frequency Hold-Off Counter is loaded with the value written to this address when either a Soft_SYNC or Pin_SYNC comes into the channel. The Counter begins counting down so that when it reaches 1 the NCO frequency word is updated with the values of addresses 0x85 and 0x86. This is known as a Hop or Hop_SYNC. If this register is written to a 1 then the NCO Frequency will be updated immediately when the SYNC comes into the channel. If it is written to a 0 then no HOP will occur. NCO HOPs can be either phase continuous or non-phase continuous depending upon the state of bit 3 of the NCO control register at channel address 0x88. When this bit is low then the Phase Accumulator of the NCO is not cleared but starts to add the new NCO Frequency word to the accumulator as soon as the SYNC occurs. If this bit is high then the Phase Accumulator of the NCO is cleared to 0 and the new word is then accumulated.

0x85: NCO Frequency Register 0
This register represents the 16 LSBs of the NCO Frequency word. These bits are shadowed and are not updated to the register used for the processing until the channel is either brought out of SLEEP or a Soft_SYNC or Pin_SYNC has been issued. In the latter two cases the register is updated when the Frequency Hold-Off Counter hits a value of 1. If the Frequency Hold-Off Counter is set to 1 then the register will be updated as soon as the shadow is written.

0x86: NCO Frequency Register 1
This register represents the 16 MSBs of the NCO Frequency word. These bits are shadowed and are not updated to the register used for the processing until the channel is either brought out of SLEEP or a Soft_SYNC or Pin_SYNC has been issued. In the latter two cases the register is updated only when the Frequency Hold-Off Counter hits a value of 1. If the Frequency Hold-Off Counter is set to 1 then the register will be updated as soon as the shadow is written.

0x87: NCO Phase Offset Register
This register represents a 16-bit phase offset to the NCO. It can be interpreted as values ranging from 0 to just under 2π.

0x88: NCO Control Register
This 9-bit Register controls features of the NCO and the channel. The bits are defined below. For more detail the NCO section should be consulted.

Bits 8-7 of this register choose which of the four SYNC pins are used by the channel. The SYNC pin selected can be used to initiate a START, HOP, or timing adjustment to the Channel. The Synchronization Section of the Data-Sheet provides more details on this.

Bit 6 of this register defines whether the A or B input port is used by the channel. If this bit is low then the A Input Port is selected and if this bit is high the B Input Port is selected.

Bits 5-4 are reserved and must be written logic low.

Bit 3 determines whether or not the phase accumulator of the NCO is cleared when a Hop occurs. The Hop can originate from either the Pin_SYNC or Soft_SYNC. When this bit is set to 0 the Hop is phase continuous and the accumulator is not cleared. When this bit is set to 1 the accumulator is cleared to 0 before it begins accumulating the new frequency word. This is appropriate when multiple channels are hopping from different frequencies to a common frequency.

Bits 2-1 control whether or not the dithers of the NCO are activated. The use of these features is heavily determined by the system constraints. Consult the NCO section of the data sheet for more detailed information on the use of dither.

Bit 0 of this register allows the NCO Frequency translation stage to be bypassed. When this occurs the data from the A Input Port is passed down the I path of the channel and the data from the B Input Port is passed down the Q path of the channel. This allows a real filter to be performed on baseband I and Q data.

AD6652 CHANNEL ADDRESS REGISTERS (Continued)

Ch Address	Register	Bit Width	Comments
90	rCIC2 Decimation – 1	12	M_{rCIC2}-1
91	rCIC2 Interpolation – 1	9	L_{rCIC2}-1
92	rCIC2 Scale	12	11: Reserved, write to logic low 10: Reserved, write to logic low 9-5: SrCIC2 (rCIC2 scale factor) 4-0: Re-enter the above SrCIC2 scale factor

93	Reserved	8	Reserved (Must be written low)
94	CIC5 Decimation –1	8	M_{CIC5}-1
95	CIC5 Scale	5	4-0: CIC5_SCALE[4:0]
96	Reserved	8	Reserved(Must be written low)
97-9F	Unused		
A0	RCF Decimation – 1	8	M_{RCF}-1
A1	RCF Decimation Phase	8	P_{RCF}
A2	RCF Number of Taps –1	8	N_{Taps}-1
A3	RCF Coefficient Offset	8	CO_{RCF}
A4	RCF Control Register	11	10: RCF By-pass BIST 9: RCF Input Select (own 0, other 1) 8: Program RAM Bank 1/0 7: Use Common Exponent 6: Force Output Scale 5-4: Output Format 1x: Floating Point 12+4 01: Floating Point 8+4 00: Fixed Point 3-0: Output Scale
A5	BIST Signature for I path	16	BIST-I
A6	BIST Signature for Q path	16	BIST-Q
A7	# of BIST outputs to accumulate	20	19-0: # of outputs(Counter Value Read)
A8	RAM BIST Control Register	3	2: D-RAM Fail/Pass 1: C-RAM Fail/Pass 0: RAM BIST Enable
A9	Output Control Register		9: Map RCF Data to BIST registers 5: Output Format 1: 16-bit I and 16-bit Q 0: 12-bit I and 12-bit Q

Table XIII. Conclusion of the Channel Address Memory Map

0x90: rCIC2 Decimation – 1 (M_{rCIC2}-1)
This register is used to set the decimation in the rCIC2 filter. The value written to this register is the decimation minus one. The rCIC2 decimation can range from 1 to 4096 depending upon the Interpolation of the channel. The decimation must always be greater than the interpolation. M_{rCIC2} must be chosen larger than L_{rCIC2} and both must be chosen such that a suitable rCIC2 Scalar can be chosen. For more details the rCIC2 section should be consulted

0x91: rCIC2 Interpolation – 1 (L_{rCIC2}-1)
This register is used to set the interpolation in the rCIC2 filter. The value written to this register is the interpolation minus one. The rCIC2 interpolation can range from 1 to 512 depending upon the decimation of the rCIC2. There is no timing error associated with this interpolation. See the rCIC2 section of the data sheet for further details.

0x92: rCIC2 Scale

The rCIC2 Scale register is used to provide attenuation to compensate for the gain of the rCIC2 and to adjust the linearization of the data from the floating-point input. The use of this scale register is influenced both by the rCIC2 growth and Floating Point Input Port Considerations. The rCIC2 section should be consulted for details. The rCIC2 scalar has been combined with the Exponent Offset and will need to be handled appropriately in both the Input Port and rCIC2 sections.

Bit 11 determines the polarity of the exponent. Normally, this bit will be cleared unless and ADC such as the AD6600 is used, in which case this bit will be set.

Bit 10 determines the weight of the Exponent word associated with the input port. When this bit is low then each exponent step is considered to be worth 6.02dB. When this bit is high then each exponent step is considered to be worth 12.02dB.

Bits 9-5 are the actual scale value used when the Level Indicator, LI pin associated with this channel is active.

Bits 4-0 are the actual scale value used when the Level Indicator, LI pin associated with this channel is active.

0x93:
Reserved (Must be written low)

0x94: CIC5 Decimation – 1 (M_{CIC5}-1)
This register is used to set the decimation in the CIC5 filter. The value written to this register is the decimation minus one. Although this is an 8-bit register the decimation is usually limited to between 1 and 32. Decimations higher than 32 would require more scaling than the CIC5 is capable of.

0x95: CIC5 Scale
The CIC5 Scale factor is used to compensate for the growth of the CIC5 filter. Consult the CIC5 section for details.

0x96:
Reserved (Must be written low)

0xA0: RCF Decimation – 1 (M_{RCF}-1)
This register is used to set the decimation of the RCF stage. The value written is the decimation minus one. Although this is an 8-bit register which allows decimation up to 256, for most filtering scenarios the decimation should be limited between 1 and 32. Higher decimations are allowed but the alias protection of the RCF may not be acceptable for some applications.

0xA1: RCF Decimation Phase (P_{RCF})
This register allows any one of the M_{RCF} phases of the filter to be used and can be adjusted dynamically. Each time a filter is started then this phase is updated. When a channel is synchronized then it will retain the phase setting chosen here. This can be used as part of a timing recovery loop with an external processor or can allow multiple RCFs to work together while using a single RCF pair. The RCF section of the data sheet should be consulted for further details.

0xA2: RCF Number of Taps minus one (N_{RCF}-1)
The number of taps for the RCF filter minus one is written here.

0xA3: RCF Coefficient Offset (CO_{RCF})
This register is used to specify which section of the 256-word coefficient memory is used for a filter. It can be used to select between multiple filters that are loaded into memory and referenced by this pointer. This register is shadowed and the filter pointer is updated every time a new filter is started. This allows the Coefficient Offset to be written even while a filter is being computed with disturbing operation. The next sample that comes out of the RCF will be with the new filter.

0xA4: RCF Control Register
The RCF Control Register is an 11-bit register that controls general features of the RCF as well as output formatting. The bits of this register and their functions are described below.

Bit 10 bypasses the RCF filter and sends the CIC5 output data to the BIST-I and BIST-Q registers. The 16 MSBs of the CIC5 data can be accessed from this register if bit 9 of the RCF Control Register 2 at channel address 0xA9 is set.

Bit 9 of this register controls the source of the input data to the RCF. If this bit is 0 then the RCF processes the output data of it's own channel. If this bit is 1 then it processes the data from the CIC5 of another channel. The CIC5 that the RCF is connected to when this bit is 1 are shown in the table XIV below. These can be used to allow multiple RCFs to be used together to process wider bandwidth channels. See the Multi-Processing section of the data-sheet for further details.

Channel	RCF Input Source When Bit-9 is 1
0	1
1	0
2	1
3	1

Table XIV. RCF Input Configurations

Bit 8 is used as an extra address to allow a second block of 128 words of CMEM to be addressed by the channel addresses at 0x00-0x7F. If this bit is 0 then the first 128 words are written and if this bit is 1 then a second 128 words is written. This bit is only used to program the Coefficient Memory. It is not used in any way by the processing and filters longer than 128 taps can be performed.

Bit 7 is used to help control the output formatting of the AD6652s RCF data. This bit is only used when the 8+4 or 12+4 floating-point modes are chosen. These modes are enable by bits 5 and 4 of this register below. When this bit is 0 then the I and Q output exponents are determined separately based on their individual magnitudes. When this bit is 1 then the I and Q data is a Complex Floating-Point number where I and Q use a single exponent that is determined based on the maximum magnitude of I or Q.

Bit 6 is used to force the Output Scale Factor in bits 3-0 of this register to be used to scale the data even when one of the Floating Point Output Modes is used. If the number

was too large to represent with the Output Scale chosen then the mantissas of the I and Q data clip and do not overflow.

Bits 5 and 4 choose the output formatting option used by the RCF data. The options are defined in the Table XV below and are discussed further in the output format section of the data sheet.

Bit Values	Output Option
1x	12-bit Mantissa and 4-bit Exponent(12+4)
01	8-bit Mantissa and 4-bit Exponent(8+4)
00	Fixed Point Mode

Table XV. Output Formats

Bits 3-0 of this register represent the Output Scale Factor of the RCF. It is used to scale the data when the output format is in fixed-point mode or when the Force Exponent bit is high.

0xA5: BIST Register for I
This register serves two purposes. The first is to allow the complete functionality of the I data path in the channel to be tested in the system. The BIST section of the data sheet should be consulted for further details. The second function is to provide access to the I output data through the micro-port. To accomplish this the Map RCF data to BIST bit in the RCF Control register 2, 0xA9, should be set high. 16-bits of I data can then be read through the micro port in either the 8+4, 12+4, 12 bit linear or 16-bit linear output modes. This data may come from either the formatted RCF output or the CIC5 output.

0xA6: BIST Register for Q
This register serves two purposes. The first is to allow the complete functionality of Q data path in the channel to be tested in the system. The BIST section of the data sheet should be consulted for further details. The second function is to provide access to the Q output data through the micro-port. To accomplish this the Map RCF data to BIST bit in the RCF Control register 2, 0xA9, should be set high. 16-bits of Q data can then be read through the micro port in either the 8+4, 12+4, 12 bit linear or 16-bit linear output modes. This data may come from either the formatted RCF output or the CIC5 output.

0xA7: BIST Control Register
This register controls the number of outputs of the RCF or CIC filter that are observed when a BIST test is performed. The BIST signature registers at addresses 0xA5 and 0xA6 will observe this number of outputs and then terminate. The loading of this register also starts the BIST engine running. Details of how to utilize the BIST circuitry are defined in the BIST section of the data sheet.

0xA8: RAM BIST Control Register
This register is used to test the memories of the AD6652 should they ever be suspected of a failure. Bit 0 of this register is written with a 1 when the channel is in SLEEP and the user waits for 1600 CLKs and then polls the bits. If bit 1 is high then the CMEM failed the test and if bit 2 is high then the data memory used by the RCF failed the test.

0xA9: Output Control Register
Bit 9 of this register allows the RCF or CIC5 data to be mapped to the BIST registers at addresses 0xA5 and 0xA6. When this bit is 0 then the BIST register is in signature mode and ready for a self-test to be run. When this bit is 1 then the output data from the RCF after formatting or the CIC5 data is mapped to these registers and can be read through the micro-port.

Bits 5 determines the word length used by the parallel port. If this bit is 0 then the parallel port uses 12 bit words for I and Q. If this bit is 1 then the parallel port uses 16 bit words for I and Q. When the fixed point output option is chosen from the RCF control register then these bits also set the rounding correctly in the output formatter of the RCF.

Remaining bits in this register are reserved and should be written low when programming.

OUTPUT PORT CONTROL REGISTERS
In order to access the Output Port Registers, bit 5 of the Sleep register located in the external memory map must be written logic high. The CAR (Channel Address Register) is then written with the address to the correct Output Port Register. Refer to Table XVI below for a complete description of all registers.

0x00 through 0x07
These eight addresses are reserved and should be written logic low.

0x08 Port A Control Register
Bit 0 enables the use of interpolating half band filter corresponding to Port A. Half band A can be used to interleave the data streams of multiple channels and interpolate by two providing a maximum output data rate of 4x the chip rate. It can be configured to listen to all four channels; channels 0, 1, 2, 3; channels 0, 1, 2; channels 0, 1; or only channel 0. Half band A is bypassed when bit 0 = 1, in which case the outputs of the RCFs are directly sent to the AGC. The channel data streams still get interleaved

with the half band bypassed, but they are not filtered and interpolated. The maximum data rate from this configuration would be 2x the chip rate.

0x09 Port B Control Register
Bit 0 enables the use of interpolating half band filter corresponding to Port B. Half band B can be used to interleave the data streams of multiple channels and interpolate by two providing a maximum output data rate of 4x the chip rate. It can be configured to listen to channels 2 and 3; or only channel 2. Half band B is bypassed when bit 0 = 1, in which case the outputs of the RCFs are directly sent to the AGC. The channel data streams still get interleaved with the half band bypassed, but they are not filtered and interpolated. The maximum data rate from this configuration would be 2x the chip rate.

0x0A AGC A Control Register
This 8-bit register controls features of the AGC A. The bits are defined below:

Bits 7-5 define the output word length of the AGC. The output word can be 4-8, 10, 12, or 16 bits wide. The control register bit representation to obtain different output word lengths is given in the Memory Map table.

Bit 4 of this register sets the mode of operation for the AGC. When this bit is 0, the AGC tracks to maintain the output signal level and when this bit is 1, the AGC tracks to maintain a constant clipping error. Consult the AGC section for more details about these modes.

The bits 3-1 are used to configure the synchronization of the AGC. The CIC decimator filter in the AGC can be synchronized to an external sync signal to output an update sample for the AGC error calculation and filtering. This way the AGC gain changes can be synchronized to an external block like a Rake receiver. Whenever an external sync signal is received, the hold off counter at 0x0B is loaded and begins to count down. When the counter reaches one the CIC filter dumps an update sample and starts working towards a new update sample. The AGC can be initialized on each SYNC or only on the first SYNC.

Bit 3 is used to issue a command to the AGC to SYNC immediately. If this bit is set the CIC filter will update the AGC with a new sample immediately and start operating towards the next update sample. The AGC can be synchronized by the microport control interface using this method.

Bit 2 is used to determine whether the AGC should initialize on a SYNC or not. When this bit is set, the CIC filter is cleared and new values for CIC decimation, number of averaging samples, CIC scale, Signal gain 'Gs', gain K and pole parameter 'P' are loaded. When bit2 = 0, the above-mentioned parameters are not updated and the CIC filter is not cleared. In both cases an AGC update sample is output from the CIC filter and the decimator starts operating towards the next output sample whenever a SYNC occurs.

Bit 1 is used to ignore repetitive synchronization signals. In some applications, the synchronization signal may occur periodically. If this bit is clear, each synchronization request will re-synchronize the AGC. If this bit is set only the first occurrence will cause the AGC to synchronize and will update AGC gain values periodically depending on the decimation factor of the AGC CIC filter.

Bit 0 is used to bypass the AGC section, when it is set. The 23-bit representation from interpolating half band filters is still reduced to a lower bit width representation as set by bits 7-5 of the AGC A Control Register. A truncation at the output of the AGC accomplishes this task.

0x0B AGC A Hold off Counter
The AGC A Hold-off counter is loaded with the value written to this address when either a Soft_SYNC or Pin_SYNC comes into the channel. The counter begins counting down so when it reaches one, a SYNC is given to AGC A. This SYNC may or may not initialize the AGC, as defined by the control word. The AGC loop is updated with a new sample from the CIC filter whenever a SYNC occurs. If this register is written to one, the AGC will be updated immediately when the SYNC occurs. If this register is written to a zero the AGC cannot be synchronized.

0x0C AGC A Desired level
This 8-bit register contains the desired output power level or desired clipping level depending on the mode of operation. This desired Request 'R' level can be set in dB from 0 to –23.99 in steps of 0.094dB. 8-bit binary floating-point representation is used with 2-bit exponent followed by 6 bit mantissa. Mantissa is in steps of 0.094 dB and exponent in 6.02 dB steps. For example: 10'100101 represents 2 * 6.02 + 37 * 0.094 = 15.518dB.

0x0D AGC A Signal Gain
This register is used to set the initial value for a Signal Gain used in the gain multiplier. This 12-bit value sets the initial signal gain between 0 and 96.296dB in steps of 0.024dB. 12-bit binary floating-point representation is used with 4-bit exponent followed by 8 bit mantissa. For example: 0111'10001001 is equivalent to 7 * 6.02 + 137 * 0.024 + 45.428dB.

0x0E AGC A Loop Gain

This 8-bit register is used to define the open loop gain 'K'. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of 'K' is updated in the AGC loop each time the AGC is initialized.

0x0F AGC A Pole Location
This 8-bit register is used to define the open loop filter pole location 'P'. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of 'P' is updated in the AGC loop each time the AGC is initialized. This open loop pole location will directly impact the closed loop pole locations as explained in the AGC section.

0x10 AGC A Average Samples
This 6-bit register contains the scale used for the CIC filter and the number of power samples to be averaged before being fed to the CIC filter.

Bits 5-2 define the scale used for the CIC filter.

Bits 1-0 define the number of samples to be averaged before they are sent to the CIC decimating filter. This number can be set between 1 and 4 with bit representation 00 meaning 1 sample and bit representation 11 meaning 4 samples.

0x11 AGC A Update Decimation
This 12-bit register sets the AGC decimation ratio from 1 to 4096. An appropriate scaling factor should be set factor to avoid loss of bits.

0x12 AGC B Control Register
This 8-bit register controls features of the AGC A. The bits are defined below:

Bits 7-5 define the output word length of the AGC. The output word can be 4-8, 10, 12, or 16 bits wide. The control register bit representation to obtain different output word lengths is given in the Memory Map table.

Bit 4 of this register sets the mode of operation for the AGC. When this bit is 0, the AGC tracks to maintain the output signal level and when this bit is 1, the AGC tracks to maintain a constant clipping error. Consult the AGC section for more details about these modes.

The bits 3-1 are used to configure the synchronization of the AGC. The CIC decimator filter in the AGC can be synchronized to an external sync signal to output an update sample for the AGC error calculation and filtering. This way the AGC gain changes can be synchronized to an external block like a Rake receiver. Whenever an external sync signal is received, the hold off counter at 0x0B is loaded and begins to count down. When the counter reaches one the CIC filter dumps an update sample and starts working towards a new update sample. The AGC can be initialized on each SYNC or only on the first SYNC.

Bit 3 is used to issue a command to the AGC to SYNC immediately. If this bit is set the CIC filter will update the AGC with a new sample immediately and start operating towards the next update sample. The AGC can be synchronized by the microport control interface using this method.

Bit 2 is used to determine whether the AGC should initialize on a SYNC or not. When this bit is set, the CIC filter is cleared and new values for CIC decimation, number of averaging samples, CIC scale, Signal gain 'Gs', gain K and pole parameter 'P' are loaded. When bit2 = 0, the above-mentioned parameters are not updated and the CIC filter is not cleared. In both cases an AGC update sample is output from the CIC filter and the decimator starts operating towards the next output sample whenever a SYNC occurs.

Bit 1 is used to ignore repetitive synchronization signals. In some applications, the synchronization signal may occur periodically. If this bit is clear, each synchronization request will re-synchronize the AGC. If this bit is set only the first occurrence will cause the AGC to synchronize and will update AGC gain values periodically depending on the decimation factor of the AGC CIC filter.

Bit 0 is used to bypass the AGC section, when it is set. The 23-bit representation from interpolating half band filters is still reduced to a lower bit width representation as set by bits 7-5 of the AGC A Control Register. A truncation at the output of the AGC accomplishes this task.

0x13 AGC B Hold off Counter
The AGC A Hold-off counter is loaded with the value written to this address when either a Soft_SYNC or Pin_SYNC comes into the channel. The counter begins counting down so when it reaches one, a SYNC is given to AGC A. This SYNC may or may not initialize the AGC, as defined by the control word. The AGC loop is updated with a new sample from the CIC filter whenever a SYNC occurs. If this register is written to one, the AGC will be updated immediately when the SYNC occurs. If this register is written to a zero the AGC cannot be synchronized.

0x14 AGC B Desired level

This 8-bit register contains the desired output power level or desired clipping level depending on the mode of operation. This desired Request 'R' level can be set in dB from 0 to –23.99 in steps of 0.094dB. 8-bit binary floating-point representation is used with 2-bit exponent followed by 6 bit mantissa. Mantissa is in steps of 0.094 dB and exponent in 6.02 dB steps. . For example: 10'100101 represents 2 * 6.02 + 37 * 0.094 = 15.518dB

0x15 AGC B Signal Gain
This register is used to set the initial value for a Signal Gain used in the gain multiplier. This 12-bit value sets the initial signal gain between 0 and 96.296dB in steps of 0.024dB. 12-bit binary floating-point representation is used with 4-bit exponent followed by 8 bit mantissa. For example: 0111'10001001 is equivalent to 7 * 6.02 + 137 * 0.024 + 45.428dB.

0x16 AGC B Loop Gain
This 8-bit register is used to define the open loop gain 'K'. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of 'K' is updated in the AGC loop each time the AGC is initialized.

0x17 AGC B Pole Location
This 8-bit register is used to define the open loop filter pole location 'P'. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of 'P' is updated in the AGC loop each time the AGC is initialized. This open loop pole location will directly impact the closed loop pole locations as explained in the AGC section.

0x18 AGC B Average Samples
This 6-bit register contains the scale used for the CIC filter and the number of power samples to be averaged before being fed to the CIC filter.

Bits 5-2 define the scale used for the CIC filter.

Bits 1-0 define the number of samples to be averaged before they are sent to the CIC decimating filter. This number can be set between 1 and 4 with bit representation 00 meaning 1 sample and bit representation 11 meaning 4 samples.

0x19 AGC B Update Decimation
This 12-bit register sets the AGC decimation ratio from 1 to 4096. An appropriate scaling factor should be set factor to avoid loss of bits.

0x1A Parallel Port Control A
Data is output through either a parallel port interface or a link port interface. When 0x1B,bit 7 = 0, the use of link port A is disabled and the use of parallel port A is enabled. The parallel port provides different data modes for interfacing with DSPs or FPGAs.

Bit 0 selects which data is output on parallel port A. When bit 0 = 0, parallel port A outputs data from the RCF according to the format specified by bits 1 through 4. When bit 0 = 1, parallel port A outputs the data from the AGCs according to the format specified by bits 1 and 2.

In AGC mode, bit 0 = 1 and bit 1 determines if parallel port A is able to output data from AGC A and bit 2 determines if parallel port A is able to output data from AGC B. The order of output depends on the rate of triggers from each AGC, which in turn is determined by the decimation rate of the channels feeding it. In channel mode, bit 0 = 0 and bits 1 through 4 determine which combination of the four processing channels is output. The output order depends on the rate of triggers received from each channel, which is determined by the decimation rate of each channel. The channel output indicator pins can be used to determine which data came from which channel.

Bit 5 determines the format of the output data words. When bit 5 = 0, parallel port A outputs 16-bit words on its 16-bit bus. This means that I and Q data are interleaved and the IQ indicator pin determines whether data on the port is I data or Q data. When bit 5 = 1, parallel port A is outputting an 8-bit I word and an 8-bit Q word at the same time, and the IQ indicator pins will be HIGH.

0x1B Link Port Control A
Data is output through either a parallel port interface or a link port interface. The link port provides an efficient data link between the AD6652 and a TigerSHARC DSP and can be enabled by setting 0x1D, bit 7 = 1.

Bit 0 selects which data is output on link port A. When bit 0 =0, link port A outputs data from the RCF according to the format specified by bit 1. When bit 0 = 1, link port A outputs the data from the AGCs according to the format specified by bits 1 and 2.

Bit 1 has two different meanings that depend on whether data is coming from the AGCs or from the RCFs. When data is coming from the RCFs (bit 0 = 0), bit 1 selects between two and four channel data mode. Bit 1 = 1 indicates link port A transmits RCF IQ words alternately from channels 0 and 1. When bit 1 = 1, link port A outputs RCF IQ words from each of the four channels in succession: 0, 1, 2, then 3. However, when AGC data is selected (bit 0 = 1), bit 1 selects the AGC data output mode. In this mode, when bit 1 = 1, link port A outputs AGC A IQ and gain words. With this mode, gain words must be included by setting bit 2 = 0. However, if bit 0 = bit 1 = 0, then AGC A and B are alternately output on link

port A and the inclusion or exclusion of the gain words is determined by bit 2.

Bit 2 selects if gain words are included or not in the data output. If bit 1 = 1, bit 2 =0. Since the gain words are only two bytes long and the IQ words are four bytes long, the gain words are padded with zeros to give a full 16-byte TigerSHARC quad-word. If AGC output is not selected (bit 0 = 0) then this bit can be any value.

Bits 6 through 3 specify the programmable delay value for link port A between the time the link port receives a data ready from the receiver and the time it transmits the first data word. The link port must wait at least 6 cycles of the receiver's clock, so this value allows the user to use clocks of differing frequency and phase for the AD6652 link port and the TigerSHARC link port. There is more information on the limitations and relationship of these clocks in the section on Link Ports.

Table XVI: Memory Map for Output Port Control Registers

Address	Register	Bit Width	Comments
00		10	Reserved – write all bits logic 0
01		10	Reserved – write all bits logic 0
02		20	Reserved – write all bits logic 0
03		6	Reserved – write all bits logic 0
04		10	Reserved – write all bits logic 0
05		10	Reserved – write all bits logic 0
06		20	Reserved – write all bits logic 0
07		5	Reserved – write all bits logic 0
08	Port A Control Register	4	3: Port A Enable 2-1: HB A Signal Interleaveing 11 All 4 Channels 10 Chs 0, 1, 2 01 Chs 0,1 00 Ch 0 0: ByPass
09	Port B Control Register	3	2: Port B Enable 1: HB A Signal Interleaveing 1 Chs 2, 3 0 Ch 2 0: ByPass
0A	AGC A Control Register	8	7-5: Output Word Length 111 4 bits 110 5 bits 101 6 bits 100 7 bits 011 8 bits 010 10 bits 001 12 bits 000 16 bits 4: Clipping Error 1: Maintain level of clipping error 0: Maintain output signal level 3: Sync now 2: Init on sync 1: First sync only 0: Bypass
0B	AGC A Hold Off Counter	16	15-0: Hold Off Value
0C	AGC A Desired Level	8	7-0: Desired output power level or clipping energy (R parameter)
0D	AGC A Signal Gain	12	11-0: Gs parameter
0E	AGC A Loop Gain	8	7-0: K parameter
0F	AGC A Pole Location	8	7-0: P parameter
10	AGC A Average Samples	6	5-2: Scale for CIC decimator 1-0: Number of averaging samples
11	AGC A Update Decimation	12	11-0: CIC decimation ratio
12	AGC B Control Register	8	7-5: Output Word Length 112 4 bits 110 5 bits 102 6 bits 101 7 bits 011 8 bits 010 10 bits 001 12 bits 000 16 bits 4: Clipping Error 1: Maintain level of clipping error 0: Maintain output signal level 3: Sync now 2: Init on sync 1: First sync only 0: Bypass

13	AGC B Hold Off Counter	16	15-0: Hold Off Value
14	AGC B Desired Level	8	7-0: Desired output power level or clipping energy (R parameter)
15	AGC B Signal Gain	12	11-0: Gs parameter
16	AGC B Loop Gain	8	7-0: K parameter
17	AGC B Pole Location	8	7-0: P parameter
18	AGC B Average Samples	6	5-2: Scale for CIC decimator 1-0: Number of averaging samples
19	AGC B Update Decimation	12	11-0: CIC decimation
1A	Parallel A Control	8	7-6: Reserved 5: Parallel Port Data Format 1: 8-bit Parallel I, Q 0: 16-bit Interleaved I, Q 4: Channel 3 3: Channel 2 2: Channel 1 / AGC B Enable 1: Channel 0 / AGC A Enable 0: AGC_CH Select 1: Data comes from AGCs 0: Data comes from Channels
1B	Link A Control	8	7: Link Port A Enable 6-3: Wait 2: No Gain Word 1: Don't output gain word 0: Output gain word 1: Channel Data Interleaved 1: 2 channel mode/separate AB 0: 4 channel mode/AB same port 0: AGC_CH Select 1: Data comes from AGCs 0: Data comes from Channels
1C	Parallel B Control	8	7-6: Reserved 5: Parallel Port Data Format 1: 8-bit Parallel I, Q 0: 16-bit Interleaved I, Q 4: Channel 3 3: Channel 2 2: Channel 1 / AGC B Enable 1: Channel 0 / AGC A Enable 0: AGC_CH Select 1: Data comes from AGCs 0: Data comes from Channels
1D	Link B Control	8	7: Link Port B Enable 6-3: Wait 2: No Gain Word 1: Don't output gain word 0: Output gain word 1: Channel Data Interleaved 1: 2 channel mode/separate AB 0: 4 channel mode/AB same port 0: AGC_CH Select 1: Data comes from AGCs 0: Data comes from Channels
1E	Port Clock Control	3	2-1: PCLK divisor 0: PCLK Master/Slave[1] 0: Slave 1: Master

[1]PCLK boots as slave.

0x1C Parallel Port Control B
Data is output through either a parallel port interface or a link port interface. When 0x1D, bit 7 = 0, the use of link port B is disabled and the use of parallel port B is enabled. The parallel port provides different data modes for interfacing with DSPs or FPGAs.

Bit 0 selects which data is output on parallel port B. When bit 0 = 0, parallel port B outputs data from the RCF according to the format specified by bits 1 through 4. When bit 0 = 1, parallel port B outputs the data from the AGCs according to the format specified by bits 1 and 2.

In AGC mode, bit 0 = 1 and bit 1 determines if parallel port B is able to output data from AGC A and bit 2 determines if parallel port B is able to output data from AGC B. The order of output depends on the rate of triggers from each AGC, which in turn is determined by the decimation rate of the channels feeding it. In channel mode, bit 0 = 0 and bits 1 through 4 determine which combination of the four processing channels is output. The output order depends on the rate of triggers received from each channel, which is determined by the decimation rate of each channel. The channel output indicator pins can be used to determine which data came from which channel.

Bit 5 determines the format of the output data words. When bit 5 = 0, parallel port B outputs 16-bit words on its 16-bit bus. This means that I and Q data are interleaved and the IQ indicator pin determines whether data on the port is I data or Q data. When bit 5 = 1, parallel port B is outputting an 8-bit I word and an 8-bit Q word at the same time, and the IQ indicator pins will be HIGH.

0x1D Link Port Control B
Data is output through either a parallel port interface or a link port interface. The link port provides an efficient data link between the AD6652 and a TigerSHARC DSP and can be enabled by setting 0x1D, bit 7 = 1.

Bit 0 selects which data is output on link port B. When bit 0 =0, link port B outputs data from the RCF according to the format specified by bit 1. When bit 0 = 1, link port B outputs the data from the AGCs according to the format specified by bits 1 and 2.

Bit 1 has two different meanings that depend on whether data is coming from the AGCs or from the RCFs. When data is coming from the RCFs (bit 0 = 0), bit 1 selects between two and four channel data mode. Bit 1 = 1 indicates link port A transmits RCF IQ words alternately from channels 0 and 1. When bit 1 = 1, link port B outputs RCF IQ words from each of the four channels in succession: 0, 1, 2, then 3. However, when AGC data is selected (bit 0 = 1), bit 1 selects the AGC data output mode. In this mode, when bit 1 = 1, link port B outputs AGC B IQ and gain words. With this mode, gain words must be included by setting bit 2 = 0. However, if bit 0 = bit 1 = 0, then AGC A and B are alternately output on link port B and the inclusion or exclusion of the gain words is determined by bit 2.

Bit 2 selects if gain words are included or not in the data output. If bit 1 = 1, bit 2 =0. Since the gain words are only two bytes long and the IQ words are four bytes long, the gain words are padded with zeros to give a full 16-byte TigerSHARC quad-word. If AGC output is not selected (bit 0 = 0) then this bit can be any value.

Bits 6 through 3 specify the programmable delay value for link port B between the time the link port receives a data ready from the receiver and the time it transmits the first data word. The link port must wait at least 6 cycles of the receiver's clock, so this value allows the user to use clocks of differing frequency and phase for the AD6652 link port and the TigerSHARC link port. There is more information on the limitations and relationship of these clocks in the section on Link Ports.

0x1E Port Clock Control
Bit 0 determines whether PCLK is supplied externally by the user or derived internally in the AD6652. If PCLK is derived internally from DCLK (Bit 0 = 1), it is output through the PCLK pin as a master clock. For most applications, PCLK will be provided by the user as an input to the AD6652 via the PCLK pin.

Bits 2 and 1 allow the user to divide DCLK by an integer value to generate PCLK (00 = 1, 01 = 2, 10 = 4, 11 = 8).

MICROPORT CONTROL

The AD6652 has an 8-bit microprocessor port and a serial control port. The use of each of these ports is described separately below. The interaction of the ports is then described. The Microport interface is a multi-mode interface that is designed to give flexibility when dealing with the host processor. There are two modes of bus operation: Intel non-multiplexed mode (INM), and Motorola non-multiplexed mode (MNM). The mode is selected based on host processor and which mode is best suited to that processor. The micro-port has an 8-bit data bus(D[7:0]), 3-bit address bus(A[2:0]), 3 control pins lines (/CS, /DS or /RD, RW or /WR), and one status pin(DTACK or RDY). The functionality of the control signals and status line changes slightly depending upon the mode that is chosen. Refer to the timing diagrams and the following descriptions for details on the operation of both modes.

External Memory Map
The External Memory Map is used to gain access to the Channel Address Space described previously. The 8-bit data and address buses are used to this set of 8 registers that can be seen in the following table 16. These registers are collectively referred to as the External Interface Registers since they control all accesses to the Channel Address space as well as output control registers. The use of each of these individual registers is described below in detail. It should be noted that the Serial Control interface has the same memory map as the micro-port interface and can carry out the EXACT same functions, although at a slower rate.

Access Control Register (ACR)
The Access Control Register serves to define the channel or channels that receive an access from the micro-port or serial port control.

Bit 7 of this register is the Auto-Increment bit. If this bit is a 1 then the CAR register described below will increment its value after every access to the channel. This allows blocks of address space such as Coefficient Memory to be initialized more efficiently.

A[2:0]	Name	Comment
111	Access Control Register (ACR)	7: Auto Increment 6: Broadcast 5-2: Instruction[3:0] 1-0: A[9:8]
110	Channel Address Registers (CAR)	7-0: A[7:0]
101	SOFT_SYNC Control Register (Write Only)	7: PN_EN 6: Test_MUX_Select 5: Hop 4: Start 3: SYNC D 2: SYNC C 1: SYNC B 0: SYNC A
100	PIN_SYNC Control Register (Write Only)	7: Reserved write to logic low 6: First SYNC Only 5: Hop_En 4: Start_En 3: SYNC_EN D 2: SYNC_EN C 1: SYNC_EN B 0: SYNC_EN A
011	SLEEP (Write Only)	7-6: Reserved write to logic low 5: Access Output Port Control Registers 4: Reserved low 3: SLEEP 3 2: SLEEP 2 1: SLEEP 1 0: SLEEP 0
010	Data Register 2 (DR2)	7-4: Reserved 3-0: D[19:16]
001	Data Register 1 (DR1)	15-8: D[15:8]
000	Data Register 0 (DR0)	7-0: D[7:0]

Table XII. External Memory Map

Bit 6 of the register is the Broadcast bit and determines how bits 5-2 are interpreted. If Broadcast is 0 then bits 5-2, which are refereed to as Instruction bits (Instruction[3:0]), are compared with the CHIP_ID[3:0] pins. The instruction which matches the CHIP_ID[3:0] pins will determine the access. This allows up to 16 chips to be connected to the same port and memory mapped without external logic. This also allows the same serial port of a host processor to configure up to 16 chips. If the Broadcast bit is high the Instruction[3:0] word allows multiple AD6652 channels and/or chips to be configured simultaneously independent of the CHIP_ID[3:0] pins. There are 10 possible instructions that are defined in table XIII below.

Instruction	**Comment:**
0000	All Chips and all Channels will get the access.
0001	Channel 0,1,2 of all Chips will get the access.
0010	Channel 1,2,3 of all Chips will get the access.
0100	All Chips will get the access.[1]
1000	All Chips with Chip_ID[3:0] = xxx0 will get the access.[1]
1001	All Chips with Chip_ID[3:0] = xxx1 will get the access.[1]
1100	All Chips with Chip_ID[3:0] = xx00 will get the access.[1]
1101	All Chips with Chip_ID[3:0] = xx01 will get the access.[1]
1110	All Chips with Chip_ID[3:0] = xx10 will get the access.[1]
1111	All Chips with Chip_ID[3:0] = xx11 will get the access.[1]

[1]A[9:8] bits control which channel is decoded for Access.

Table XIII. Microport Instructions

This is useful for smart antenna systems where multiple channels listing to a single antenna or carrier can be configured simultaneously. The x's in the comment portion of the table represent "don't cares" in the digital decoding.

When broadcast is enabled (bit 6 set high) read back is not valid because of the potential for internal bus contention. Therefore, if read back is subsequently desired, the broadcast bit should be set low.

Bits 1-0 of the ACR are address bits that decode which of the four channels are being accessed. If the Instruction bits decode an access to multiple channels then these bits are ignored. If the Instruction decodes an access to a subset of chips then the A[9:8] bits will otherwise determine the channel being accessed.

Channel Address Register (CAR)
This register represents the 8-bit internal address of each channel. If the Auto-Increment bit of the ACR is 1 then this value will be incremented after every access to the DR0 register, which will in turn access the location pointed to by this address. The Channel Address register cannot be read back while the Broadcast bit is set high.

SOFT_SYNC Control Register
External Address [5] is the SOFT_SYNC control register and is write only.

Bit 0-3 of this register are the SOFT_SYNC control bits. These pins may be written to by the controller to initiate the synchronization of a selected channel. Although there are 4 inputs, these do not necessarily go to the channel of the same number. This is fully configurable at the channel level as to which bit to look at. All 4 channels may be configured to synchronize from a single position, or they may be paired or all independent.

Bit 4 determines if the synchronization is to apply to a chip start. If this bit is set, a chip start will be initiated.

Bit 5 determines if the synchronization is to apply to a chip hop. If this bit is set, the NCO frequency will be updated when the when the SOFT_SYNC occurs.

Bit 6 configures how the internal data bus is configured. If this bit is set low, then the internal ADC data buses are configured normally. If this bit is set, then the internal test signals are selected. The internal test signals are configured in Bit 7 of this register.

Bit 7 if set clear, a negative full scale signal is generated and made available to the internal data bus. If this bit is high, then internal pseudorandom sequence generator is enabled and this data is available to the internal data bus. The combined functions of bit 6 and 7 facilitate verification of a given filter design. Also, in conjunction with the MISR registers allows for detailed in-system chip testing. In conjunction with the JTAG test board, very high levels of chip verification can be done during system test, both in the factory and field.

PIN_SYNC Control Register
External Address [4] is the PIN_SYNC control register and is write only.

Bit 0-3 of this register are the SYNC_EN control bits. These pins may be written to by the controller to allow pin synchronization of a selected sync channel. Although there are 4 inputs, these do not necessarily go to the channel of the same number. This is fully configurable at the channel level as to which bit to look at. All 4 channels may be configured to synchronize from a single position, or they may be paired or all independent.

Bit 4 determines if the synchronization is to apply to a chip start. If this bit is set, a chip start will be initiated when the PIN_SYNC occurs.

Bit 5 determines if the synchronization is to apply to a chip hop. If this bit is set, the NCO frequency will be updated when the when the PIN_SYNC occurs.

Bit 6 is used to ignore repetitive synchronization signals. In some applications, this signal may occur periodically. If this bit is clear, each PIN_SYNC will restart/hop the channel. If this bit is set, then only the first occurrence will cause the chip to take action.

Bit 7 is used with bit 6 and 7 of external address 5. When this bit is cleared, the data supplied to the internal data bus simulates a normal ADC. When this bit is set, the data supplied is in the form of a time multiplexed ADC such as the AD6600 (this allows the equivalent of testing in the 4 channel input mode). Internally, when set, this bit forces the IEN pin to toggle as if it were driven by the A/B signal of the AD6600.

SLEEP Control Register
External Address [3] is the sleep register.

Bits 3-0 control the state of each of the channels. Each bit corresponds to one of the possible RSP channels within the device. If this bit is cleared, the channel operates normally. However, when this bit is set, the indicated channel enters a low power sleep mode.

Bit 4 is reserved and should be set to 0 always.

Bit 5 allows access to the Output Control Port Registers at channel addresses 00-1E. When this bit is set low, the channel memory map is accessed. However, when this bit is set high, it allows access to the Output Port Control Registers. When this bit is set high, the value in external address 6 (CAR) points to the memory map for the Output Port Control Registers instead of the normal channel memory map. See Output Port Control Registers in the Output memory map section.

Bit 6-7 are reserved and should be written low.

Data Address Registers
External Address [2-0] form the data registers DR2, DR1 and DR0 respectively. All internal data words have widths that are less than or equal to 20 bits. Accesses to External Address [0] DR0 trigger an internal access to the AD6652 based on the address indicated in the ACR and CAR. Thus during writes to the internal registers, External Address [0] DR0 must be written last. At this point data is transferred to the internal memory indicated in A[9:0]. Reads are performed in the opposite direction. Once the address is set, External Address [0] DR0must be the first data register read to initiate an internal access. DR2 is only 4 bits wide. Data written to the upper 4 bits of this register will be ignored. Likewise reading from this register will produce only 4 LSBs.

Write Sequencing
Writing to an internal location is achieved by first writing the upper two bits of the address to bits 1 through 0 of the ACR. Bits 7:2 may be set to select the channel as indicated above. The CAR is then written with the lower eight bits of the internal address (it doesn't matter if the CAR is written before the ACR as long as both are written before the internal access). Data register 2,(DR2) and register 1 (DR1) must be written first because the write to data register DR0 triggers the internal access. Data register DR0 must always be the last register written to initiate the internal write.

Read Sequencing
Reading from the micro port is accomplished in the same manner. The internal address is set up the same way as the write. A read from data register DR0 activates the internal read, thus register DR0 must always be read first to initiate an internal read followed by DR1and DR2. This provides the 8 LSBs of the internal read through the micro port (D[7:0]). Additional data registers can be read to read the balance of the internal memory.

Read/Write Chaining

The micro port of the AD6652 allows for multiple accesses while /CS is held low (/CS can be tied permanently low if the micro port is not shared with additional devices). The user can access multiple locations by pulsing the /WR or /RD line and changing the contents of the external three bit address bus. External access to the external registers of Table 13 is accomplished in one of two modes using the /CS, /RD, /WR, and MODE inputs. The access modes are Intel Non-Multiplexed mode and Motorola Non-Multiplexed mode. These modes are controlled by the MODE input (MODE=0 for INM, MODE=1 for MNM). /CS, /RD, and /WR control the access type for each mode.

Intel Non-Multiplexed Mode (INM)
MODE must be tied low to operate the AD6652 microprocessor in INM mode. The access type is controlled by the user with the /CS, /RD (/DS), and /WR (RW) inputs. The RDY (/DTACK) signal is produced by the micro port to communicate to the user that an access has been completed. RDY (/DTACK) goes low at the start of the access and is released when the internal cycle is complete. See the timing diagrams for both the read and write modes in the Specifications.

Motorola Non-Multiplexed Mode (MNM)
MODE must be tied high to operate the AD6652 microprocessor in MNM mode. The access type is controlled by the user with the /CS, /DS (/RD), and RW (/WR) inputs. The /DTACK (RDY) signal is produced by the micro port to communicate to the user that an access has been completed. /DTACK (RDY) goes low when an internal access is complete and then will return high after /DS (/RD) is de-asserted. See the timing diagrams for both the read and write modes in the Specifications.

SERIAL PORT CONTROL

The AD6652 has a serial port serving as a control interface apart from the microport control interface. Serial Port input pin (SDIN) can access all of the internal registers for all of the channels and has preemptive access over the microport. In this manner, a single DSP could be used to control the AD6652 over the serial port control interface.

The Serial control port uses the Serial Clock (SCLK). The Serial Input Port is self-framing as described below and allows more efficient use of the Serial Input Bandwidth for Programming. The beginning of a Serial Input Frame is signaled by a Frame bit that appears on the SDIN pin. This is the MSB of the Serial Input Frame. After the FRAME bit has been sampled high on the Falling Edge of SCLK a State Counter will start and enable an 11 bit Serial Shifter 4 Serial Clock Cycles later. These 4 SCLK cycles represent the "Don't Care" bits of the Serial Frame that are

ignored. After all of the bits are shifted then the Serial Input Port will pass along the 8-bit data and 3-bit address to the arbitration block.

The Serial Word Structure for the SDIN input is illustrated in the figure 48 below. Only 15 bits are listed so that the second bit in a standard 16-bit serial word is considered the FRAME bit. This is done for compatibility with the AD6620 Serial Input Port. The Shifting order begins with FRAME and shifts the Address MSB first and then the data MSB first.

Serial Port Timing Specifications

The AD6652 serial control channel can operate only in the slave mode. The diagrams below indicate the required timing for each of the specification.

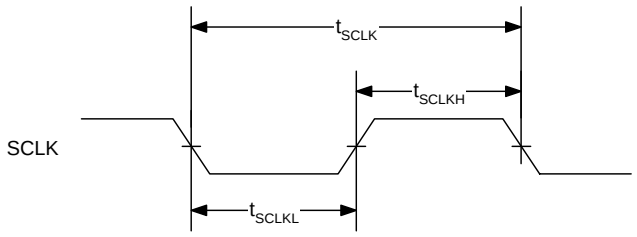


Figure 43. SCLK Timing Requirements

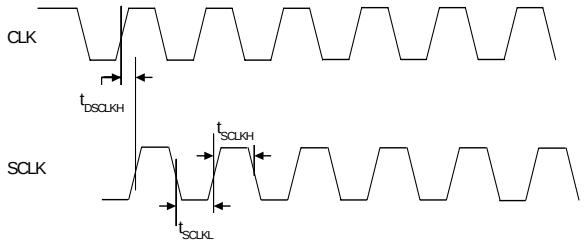


Figure 44. SCLK Switching Characteristics (Divide by 1*)*

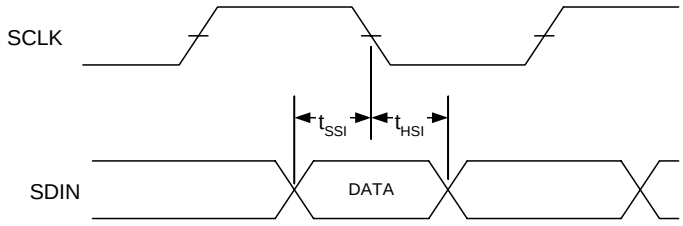


Figure 45. Serial Input Data Timing Requirements

SDIN

SDIN is the Serial Data Input. Serial Data is sampled on the falling edge of SCLK. This pin is used in the serial control mode to write the internal control registers of the AD6652.

SCLK

SCLK is a clock input and the SDIN input is sampled on the falling edge of SCLK and all outputs are switched on the rising edge of SCLK. The maximum speed of this port is 65Mhz.

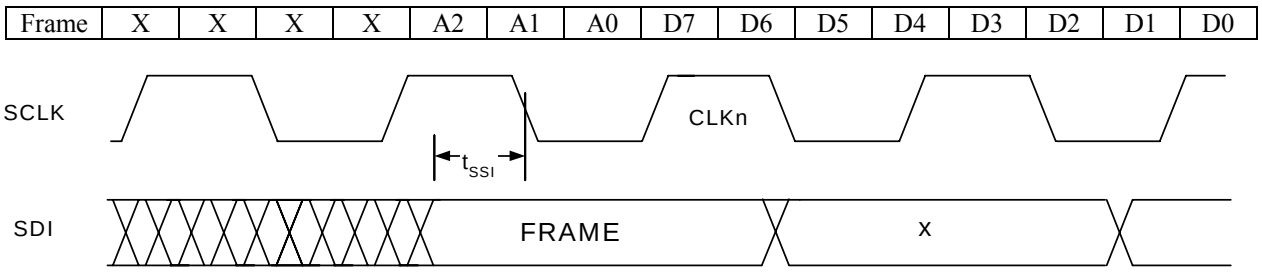


Figure 46. Serial Word Structure and Serial Port Control Timing

JTAG BOUNDARY SCAN

The AD6652 supports a subset of IEEE Standard 1149.1 specification. For additional details of the standard, please see "IEEE Standard Test Access Port and Boundary-Scan Architecture," IEEE-1149 publication from IEEE.

The AD6652 has five pins associated with the JTAG interface. These pins are used to access the on-chip Test Access Port and are listed in the table below. All input JTAG pins are pull up except for TCLK which is a pull down.

Name	Pin Number	Description
/TRST	67	Test Access Port Reset
TCLK	68	Test Clock
TMS	69	Test Access Port Mode Select
TDI	72	Test Data Input
TDO	70	Test Data Output

Table XX. Boundary Scan Test Pins

The AD6652 supports six op codes as shown below. These instructions set the mode of the JTAG interface.

Instruction	Op Code
IDCODE	001
BYPASS	111
SAMPLE/PRELOAD	010
EXTEST	000
HIGHZ	011
CLAMP	100

Table XXI. Boundary Scan Op Codes

The Vendor Identification Code can be accessed through the IDCODE instruction and has the following format.

MSB Version	Part Number	Manufacturing ID #	LSB Mandatory
0000	0010 0111 1000 1100	000 1110 0101	1

Table XXII. Vendor ID Code

A BSDL file for this device is available, please contact Analog Devices Inc. for more information.

EXTEST (3'b000) -> Places the IC into an external boundary-test mode and selects the boundary-scan register to be connected between tdi and tdo. During this, the boundary-scan register is accessed to drive test data off-chip via boundary outputs and receive test data off-chip from boundary inputs.

IDCODE (3'b001) -> Allows the IC to remain in its functional mode and selects device id register to be connected between tdi and tdo. Accessing the id register does not interfere with the operation of the IC.

SAMPLE/PRELOAD (3'b010) -> Allows the IC to remain in normal functional mode and selects the boundary-scan register to be connected between tdi and tdo. The boundary-scan register can be accessed by a scan operation to take a sample of the functional data entering and leaving the IC. Also, test data can be preloaded into the boundary scan register before an EXTEST instruction.

HIGHZ (3'b011) -> Sets all outputs to high impedance state. Selects one-bit bypass register to be connected between tdi and tdo.

CLAMP (3'b100) -> Sets the outputs of the IC to logic levels determined by the boundary-scan register and selects one-bit bypass register to be connected between tdi and tdo. Before this instruction, boundary-scan data can be preloaded with the SAMPLE/PRELOAD instruction.

BYPASS (3'b111) -> Allows the IC to remain in normal functional mode and selects one-bit bypass register between tdi and tdo. During this instruction, serial data is transferred from tdi to tdo without affecting operation of the IC.

INTERNAL WRITE ACCESS

Up to 20-bits of data (as needed) can be written by the process described below. Any high order bytes that are needed are written to the corresponding data registers defined in the external 3-bit address space. The least significant byte is then written to DR0 at address (000). When a write to DR0 is detected, the internal microprocessor port state machine then moves the data in DR2-DR0 to the internal address pointed to by the address in the LAR and AMR.

Write Pseudocode

```
void write_micro(ext_address, int data);

main();
{
/* This code shows the programming of the NCO phase
offset register using the write_micro function as defined
above. The variable address is the External Address
```

```
A[2:0]  and data is the  value to be placed in the external
interface register.
Internal Address = 0x087
 */
// holding registers for NCO phase byte wide access data
int d1, d0;
// NCO frequency word  (16-bits wide)
NCO_PHASE = 0xCBEF;
// write ACR
write_micro(7, 0x03 );
// write CAR
write_micro(6, 0x87);
// write DR1 with D[15:8]
d1 = (NCO_PHASE & 0xFF00) >> 8;
write_micro(1, d1);
// write DR0 with D[7:0]
// On this write all data is transferred to the internal address
d0 = NCO_FREQ & 0xFF;
write_micro(0, d0);
}  // end of main
```

INTERNAL READ ACCESS

A read is performed by first writing the CAR and AMR as with a write. The data registers (DR2-DR0) are then read in the reverse order that they were written. First, the Least Significant Byte of the data (D[7:0]) is read from DR0. On this transaction the high bytes of the data are moved from the internal address pointed to by the CAR and AMR into the remaining data registers (DR2-DR1). This data can then be read from the data registers using the appropriate 3 bit addresses. The number of data registers used depends solely on the amount of data to be read or written. Any unused bit in a data register should be masked out for a read.

Read Pseudocode

```
int read_micro(ext_address);

main();
{
/* This code shows the reading of  the first RCF coefficient
using the read_micro function as defined above.  The
variable address is the External Address A[2..0].

Internal Address = 0x000
 */
// holding registers for the coefficient
int d2, d1, d0;
// coefficient  (20-bits wide)
long coefficient;
// write AMR
write_micro(7, 0x00 );
// write LAR
write_micro(6, 0x00);
/* read D[7:0] from DR0,  All data is moved from the
Internal Registers to the interface registers on this access
*/
d0 = read_micro(0) & 0xFF;
// read D[15:8] from DR1
d1 = read_micro(1) & 0xFF;
// read D[23:16] from DR2
d2 = read_micro(2) & 0x0F;
coefficient = d0 + (d1 << 8) + (d2 << 16);
}  // end of main
```

AD6652 EVALUATION BOARD AND SOFTWARE

A fully populated AD6652 evaluation board kit, operating software and digital filter design software are available. The evaluation PCB kit is provided with a comprehensive instruction manual.