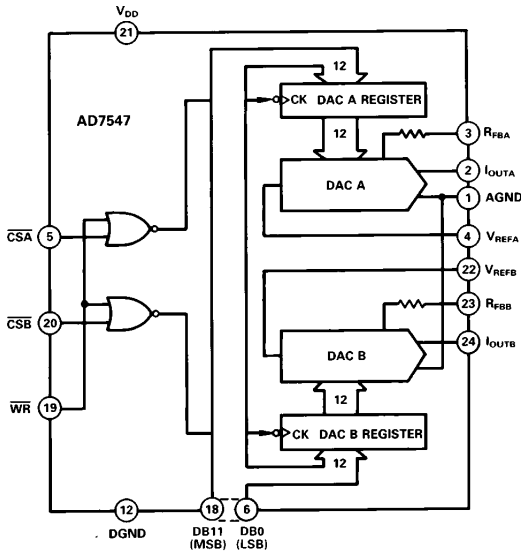
LC²MOS
Parallel Loading Dual 12-Bit DAC

AD7547

FEATURES
Two 12-Bit DACs in One Package
DAC Ladder Resistance Matching: 0.5%
Space Saving Skinny DIP and Surface Mount Packages
4-Quadrant Multiplication
Low Gain Error (1 LSB max Over Temperature)
Fast Interface Timing

APPLICATIONS
Automatic Test Equipment
Programmable Filters
Audio Applications
Synchro Applications
Process Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7547 contains two 12-bit current output DACs on one monolithic chip. Also on-chip are the level shifters, data registers and control logic for easy microprocessor interfacing. There are 12 data inputs. $\overline{CSA}$, $\overline{CSB}$, $\overline{WR}$ control DAC selection and loading. Data is latched into the DAC registers on the rising edge of $\overline{WR}$. The device is speed compatible with most microprocessors and accepts TTL, 74HC and 5 V CMOS logic level inputs.

The D/A converters provide 4-quadrant multiplication capabilities with separate reference inputs and feedback resistors. Monolithic construction ensures that thermal and gain error tracking is excellent. 12-bit monotonicity is guaranteed for both DACs over the full temperature range.

The AD7547 is manufactured using the Linear Compatible CMOS (LC²MOS) process. This allows fast digital logic and precision linear circuitry to be fabricated on the same die.

PRODUCT HIGHLIGHTS

1. DAC to DAC Matching
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. Many applications which are not practical using two discrete DACs are now possible. Typical matching: 0.5%.
2. Small Package Size
   The AD7547 is available in 0.3" wide 24-pin DIPs and SOICs and in 28-terminal surface mount packages.
3. Wide Power Supply Tolerance
   The device operates on a +12 V to +15 V V_{DD}, with ±10% tolerance on this nominal figure. All specifications are guaranteed over this range.

REV. A

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AD7547–SPECIFICATIONS[1] (V_{DD} = +12 V to +15 V, ±10%, V_{REFA} = V_{REFB} = 10 V; I_{OUTA} = I_{OUTB} = AGND = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	J, A Versions	K, B Versions	L, C Versions	S Version	T Version	U Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Gain Error	±6	±3	±l	±6	±3	±2	LSB max	Both DAC registers loaded with all 1s.
Gain Temperature Coefficient[2];								
ΔGain/ΔTemperature	±5	±5	±5	±5	±5	±5	ppm/°C max	Typical value is 1 ppm/°C
Output Leakage Current								
I_{OUTA}								
+25°C	10	10	10	10	10	10	nA max	DAC A Register loaded
T_{MIN} to T_{MAX}	150	150	150	250	250	250	nA max	with all 0s.
I_{OUTB}								
+25°C	10	10	10	10	10	10	nA max	DAC B Register loaded
T_{MIN} to T_{MAX}	150	150	150	250	250	250	nA max	with all 0s.
REFERENCE INPUT								
Input Resistance	9	9	9	9	9	9	kΩ min	Typical Input Resistance = 14 kΩ
	20	20	20	20	20	20	kΩ max	
V_{REFA}, V_{REFB}								
Input Resistance Match	±3	±3	±1	±3	±3	±1	% max	Typically ±0.5%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (lnput Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)								
+25°C	±1	±1	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{MIN} to T_{MAX}	±10	±10	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	10	10	10	10	10	10	pF max	
POWER SUPPLY[3]								
V_{DD}	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	
I_{DD}	2	2	2	2	2	2	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.
(V_{DD} = +12 V to +15 V; V_{REFA} = V_{REFB} = +10 V, I_{OUTA} = I_{OUTB} = AGND = 0 V. Output Amplifiers are AD644 except where noted.)

Parameter	T_A = +25°C	T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time	1.5		μs max	To 0.01 % of full-scale range. I_{OUT} load = 100 Ω, C_{EXT} = 13 pF. DAC output measured from rising edge of $\overline{WR}$. Typical Value of Settling Time is 0.8 μs.
Digital-to-Analog Glitch Impulse	7		nV-s typ	Measured with V_{REFA} = V_{REFB} = 0 V. I_{OUTA}, I_{OUTB} load = 100 Ω, C_{EXT} = 13 pF. DAC registers alternately loaded with all 0s and all 1s.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	–70	–65	dB max	V_{REFA}, V_{REFB} = 20 V p-p, 10 kHz sine wave. DAC
V_{REFB} to I_{OUTB}	–70	–65	dB max	registers loaded with all 0s.
Power Supply Rejection				
$\Delta Gain/\Delta V_{DD}$	±0.01	±0.02	% per % max	ΔV_{DD} = V_{DD} max – V_{DD} min
Output Capacitance				
C_{OUTA}	70	70	pF max	DAC A, DAC B loaded with all 0s.
C_{OUTB}	70	70	pF max	
C_{OUTA}	140	140	pF max	DAC A, DAC B loaded with all 1s.
C_{OUTB}	140	140	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	–84		dB typ	V_{REFA} = 20 V p-p 10 kHz sine wave, V_{REFB} = 0 V. Both DACs loaded with all 1s.
V_{REFB} to I_{OUTA}	–84		dB typ	V_{REFB} = 20 V p-p 10 kHz sine wave, V_{REFA} = 0 V. Both DACs loaded with all 1s.
Digital Crosstalk	7		nV-s typ	Measured for a Code Transition of all 0s to all 1s. I_{OUTA}, I_{OUTB} Load = 100 Ω, C_{EXT} = 13 pF
Output Noise Voltage Density (10 Hz–100 kHz)	25		nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}. Frequency of measurement is 10 Hz–100 kHz.
Total Harmonic Distortion	–82		dB typ	V_{IN} = 6 V rms, 1 kHz. Both DACs loaded with all 1s.

NOTES
[1]Temperature range as follows: J, K, L Versions, –40°C to +85°C; A, B, C Versions, –40°C to +85°C; S, T, U Versions, –55°C to +125°C.
[2]Sample tested at +25°C to ensure compliance.
[3]Functional at V_{DD} = 5 V with degraded specifications.
[4]Pin 12 (DGND) on ceramic DIPs is connected to lid.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = 10.8 V to 16.5 V, V_{REFA} = V_{REFB} = +10 V, I_{OUTA} = I_{OUTB} = AGND = 0 V)

Parameter	Limit at T_A = +25°C	Limit at T_A = –40°C to +85°C	Limit at T_A = –55°C to +125°C	Units	Test Conditions/Comments
t_1	60	80	80	ns min	Data Setup Time
t_2	25	25	25	ns min	Data Hold Time
t_3	80	80	100	ns min	Chip Select to Write Setup Time
t_4	0	0	0	ns min	Chip Select to Write Hold Time
t_5	80	80	100	ns min	Write Pulse Width

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND ..... –0.3 V, +17 V
V_{REFA}, V_{REFB} to AGND ..... ±25 V
V_{RFBA}, V_{RFBB} to AGND ..... ±25 V
Digital Input Voltage to DGND ..... –0.3 V, V_{DD} +0.3 V
I_{OUTA}, I_{OUTB} to DGND ..... –0.3 V, V_{DD} +0.3 V
AGND to DGND ..... –0.3 V, V_{DD} +0.3 V
Power Dissipation (Any Package)
  To +75°C ..... 450 mW
  Derates above +75°C ..... 6 mW/°C
Operating Temperature Range
  Commercial Plastic (J, K, L Versions) .... –40°C to +85°C
  Industrial Hermetic (A, B, C Versions) ... –40°C to +85°C
  Extended Hermetic (S, T, U Versions) ... –55°C to +125°C
  Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table I. AD7547 Truth Table

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
↓	↓	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC from the Data Bus
0	1	↓	DAC A Register Loaded from Data Bus
1	0	↓	DAC B Register Loaded from Data Bus
0	0	↓	DAC A and DAC B Registers Loaded from Data Bus

NOTES
1. X = Don't care.
2. ↓ means rising edge triggered.

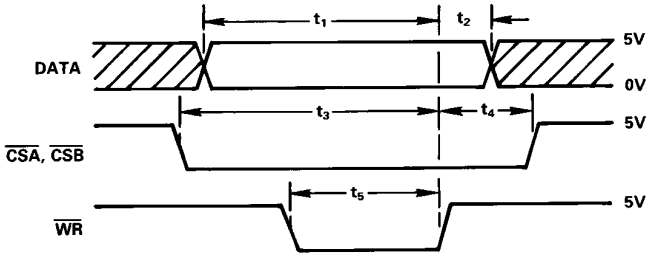


Figure 1. Timing Diagram

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7547JN	–40°C to +85°C	±1 LSB	±6 LSB	N-24
AD7547KN	–40°C to +85°C	±1/2 LSB	±3 LSB	N-24
AD7547LN	–40°C to +85°C	±1/2 LSB	±1 LSB	N-24
AD7547JP	–40°C to +85°C	±1 LSB	±6 LSB	P-28A
AD7547KP	–40°C to +85°C	±1/2 LSB	±3 LSB	P-28A
AD7547LP	–40°C to +85°C	±1/2 LSB	±1 LSB	P-28A
AD7547JR	–40°C to +85°C	±1 LSB	±6 LSB	R-24
AD7547KR	–40°C to +85°C	±1/2 LSB	±3 LSB	R-24
AD7547LR	–40°C to +85°C	±1/2 LSB	±1 LSB	R-24
AD7547AQ	–40°C to +85°C	±1 LSB	±6 LSB	Q-24
AD7547BQ	–40°C to +85°C	±1/2 LSB	±3 LSB	Q-24
AD7547CQ	–40°C to +85°C	±1/2 LSB	±1 LSB	Q-24
AD7547SQ	–55°C to +125°C	±1 LSB	±6 LSB	Q-24
AD7547TQ	–55°C to +125°C	±1/2 LSB	±3 LSB	Q-24
AD7547UQ	–55°C to +125°C	±1/2 LSB	±2 LSB	Q-24
AD7547SE	–55°C to +125°C	±1 LSB	±6 LSB	E-28A
AD7547TE	–55°C to +125°C	±1/2 LSB	±3 LSB	E-28A
AD7547UE	–55°C to +125°C	±1/2 LSB	±2 LSB	E-28A

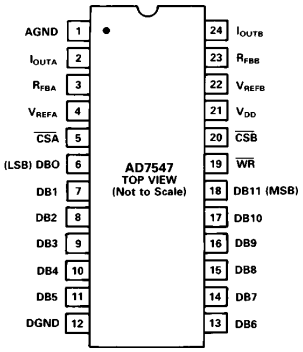
NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-24A) in lieu of cerdip packages (Q-24).
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheets.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

CAUTION

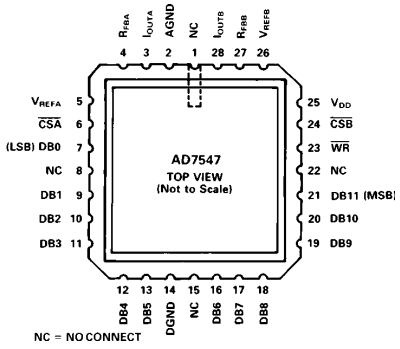
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7547 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

DIP, SOIC



LCCC



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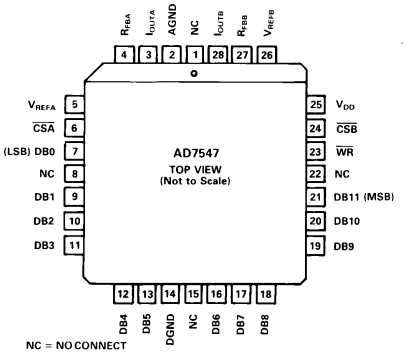


PIN FUNCTION DESCRIPTION (DIP)

Pin	Mnemonic	Description
1	AGND	Analog Ground.
2	I_{OUTA}	Current output terminal of DAC A.
3	R_{FBA}	Feedback resistor for DAC A.
4	V_{REFA}	Reference input to DAC A.
5	$\overline{CSA}$	Chip Select Input for DAC A. Active low.
6–18	DB0–DB11	12 data inputs, DB0 (LSB)–DB11 (MSB).
12	DGND	Digital Ground.
19	$\overline{WR}$	Write Input. Data transfer occurs on rising edge of $\overline{WR}$. See Table I.
20	$\overline{CSB}$	Chip Select Input for DAC B. Active low.
21	V_{DD}	Power supply input. Nominally +12 V to +15 V with ±10% tolerance.
22	V_{REFB}	Reference input to DAC B.
23	R_{FBB}	Feedback resistor of DAC B.
24	I_{OUTB}	Current output terminal of DAC B.

CIRCUIT INFORMATION

D/A SECTION

The AD7547 contains two identical 12-bit multiplying D/A converters. Each DAC consists of a highly stable R-2R ladder and 12 N-channel current steering switches. Figure 2 shows a simplified D/A circuit for DAC A. In the R-2R ladder, binary weighted currents are steered between I_{OUTA} and AGND. The current flowing in each ladder leg is constant, irrespective of switch state. The feedback resistor R_{FBA} is used with an op amp (see Figures 4 and 5) to convert the current flowing in I_{OUTA} to a voltage output.

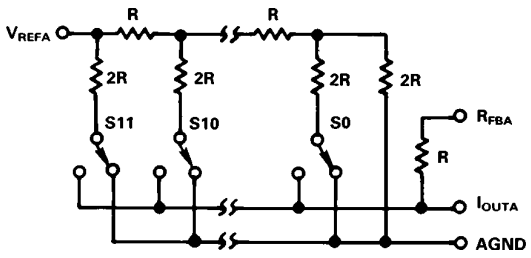


Figure 2. Simplified Circuit Diagram for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows the equivalent circuit for one of the D/A converters (DAC A) in the AD7547. A similar equivalent circuit can be drawn for DAC B. Note that AGND is common to both DAC A and DAC B.

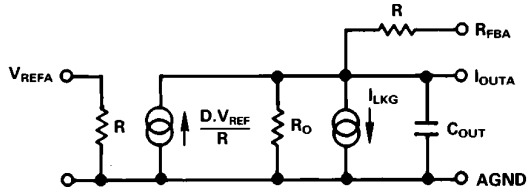


Figure 3. Equivalent Analog Circuit for DAC A

C_{OUT} is the output capacitance due to the N-channel switches and varies from about 50 pF to 150 pF with digital input code. The current source I_{LKG} is composed of surface and junction leakages and approximately doubles every 10°C. R_O is the equivalent output resistance of the device which varies with input code.

DIGITAL CIRCUIT INFORMATION

The digital inputs are designed to be both TTL and 5 V CMOS compatible. All logic inputs are static-protected MOS gates with typical input currents of less than 1 nA.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 4 is given in Table II.

Operational amplifiers A1 and A2 can be in a single package (AD644, AD712) or separate packages (AD544, AD711, AD OP27). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high speed op amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all 0s and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is 0 V. Full-scale trimming is accomplished by loading the DAC register with all 1s and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = – V_{IN} (4095/4096). For high temperature operation, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7547, Gain Error trimming is not necessary. In fixed reference applications, full-scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

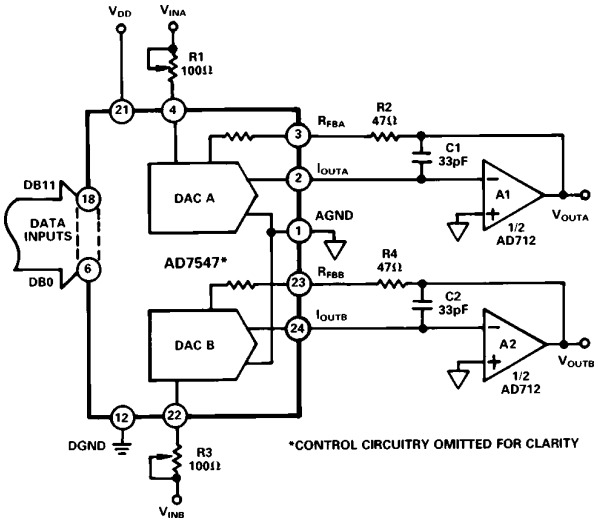


Figure 4. Unipolar Binary Operation

Table II. Unipolar Binary Code Table for Circuit of Figure 4

Binary Number In DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\,V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0 V

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0 V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, R10) varied for V_{OUT}A (V_{OUTB}) = 0 V. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

If R1, R2 (R3, R4) are not used, then resistors R5, R6, R7 (R8, R9, R10) should be ratio matched to 0.01% to ensure gain error performance to the data sheet specification. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 5 is given in Table III.

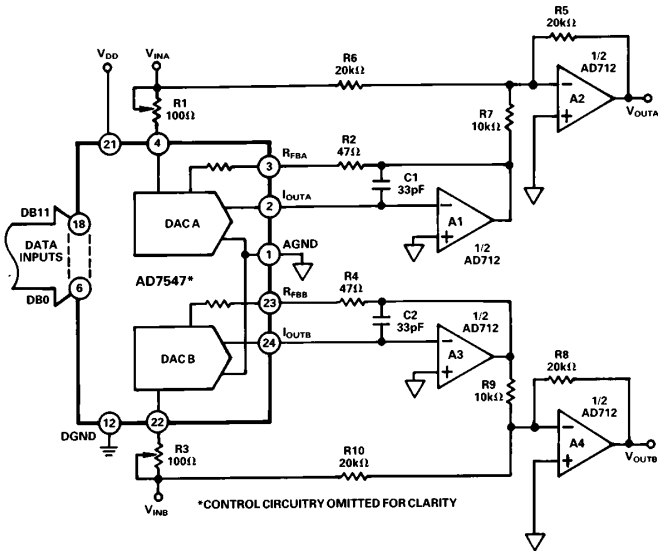


Figure 5. Bipolar Operation (Offset Binary Coding)

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

Binary Number In DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0 V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right) = -V_{IN}$

PROGRAMMABLE STATE VARIABLE FILTER

The circuit shown in Figure 6 provides three filter outputs: low pass, high pass and bandpass. It is called a State Variable Filter and the particular version shown in Figure 6 uses two AD7547s to control the critical parameters f_O, Q and A_O. Instead of several fixed resistors, the circuit uses the DAC equivalent resistances as circuit elements. Thus, R1 in Figure 6 is controlled by the 12-bit digital word loaded to DAC A of the AD7547. This is also the case with R2, R3 and R4. The fixed resistor R5 is the feedback resistor, R_{FBB}.

$$\text{DAC Equivalent Resistance, Req} = \frac{4096 \times R_{LAD}}{N}$$

where R_{LAD} = DAC Ladder Resistance

N = DAC Digital Code in Decimal. (0<N<4095)

In the circuit of Figure 6:

C1 = C2, R7 = R8, R3 = R4 (i.e., the same code is in each DAC)

$$\text{Resonant frequency, } f_O = \frac{1}{2\pi R3C1}$$

$$\text{Quality Factor, Q} = \frac{R6}{R8} \times \frac{R2}{R5}$$

$$\text{Bandpass Gain, } A_O = \frac{-R2}{R1}$$

Using the values shown in Figure 6 the Q range is 0.3 to 5 and f_O range is 0 kHz to 12 kHz.

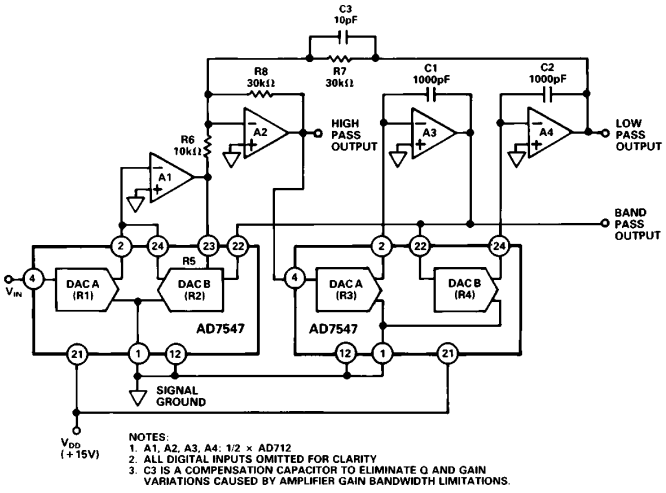


Figure 6. Programmable State Variable Filter

SINGLE SUPPLY APPLICATIONS

DAC A and DAC B of the AD7547 have termination resistors which are tied to the AGND line within the device. This arrangement is ideal for single supply operation because AGND may be biased at any voltage between DGND and V_{DD}. Figure 7 shows a circuit which provides two +5 V to +10 V analog outputs by biasing AGND to +5 V with respect to DGND, which in this case is also the system ground. The two DAC reference inputs are also tied to system ground.

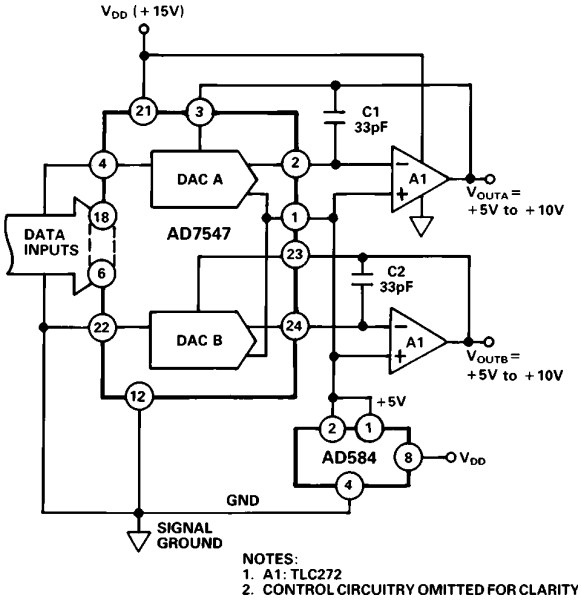


Figure 7. AD7547 Single Supply Operation

The transfer function for each channel is:

$$V_{OUT} = 5V\left(1 + \frac{R_{FB}}{R_{EQ}}\right)$$

With all 0s loaded to the DAC, $R_{EQ} = \infty$ and V_{OUT} = +5 V. With all 1s loaded $R_{EQ} = R_{LADDER} = R_{FB}$ and V_{OUT} = +10 V.

Figure 8 shows both DACs of the AD7547 connected in the voltage switching mode. For further information on this mode of operation see the CMOS DAC Application Guide from Analog Devices, publication number G872a-15-4/86. To optmize performance when using this circuit, V_{IN} must be in the range 0 V to +1.25 V and the output buffered. V_{IN} must be driven from a low impedance source (e.g., a buffer amplifier). Figure 9 shows how differential linearity degrades with increasing V_{IN}.

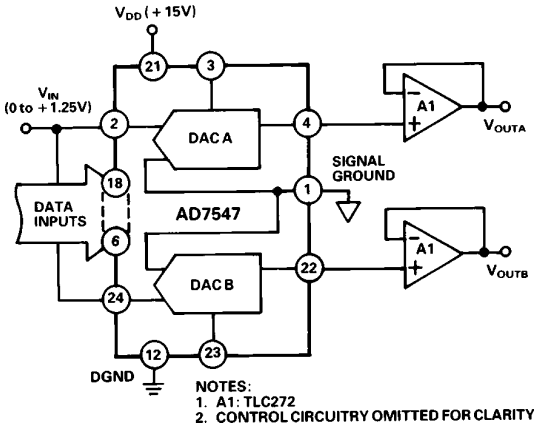


Figure 8. AD7547 Operated in Single Supply, Voltage Switching Mode

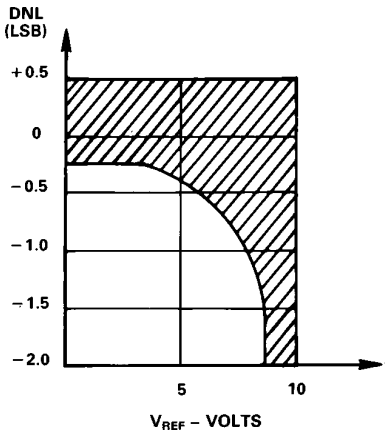


Figure 9. Differential Nonlinearity vs. Reference Voltage for Circuit of Figure 8. V_{DD} = 15 V. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C and U Grades

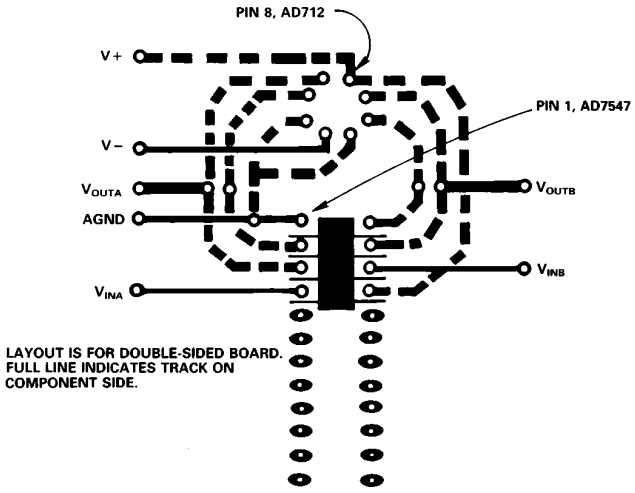


Figure 10. Suggested Layout for Circuit of Figure 4

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 4 and 5 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. To maintain specified operation, it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are the AD711C and its dual version, the AD712C. These op amps have a wide bandwidth and high slew rate and are recommended for wide bandwidth ac applications. AD711/AD712 settling time to 0.01% is typically 1 μs.

Temperature Coefficients: The gain temperature coefficient of the AD7547 has a maximum value of 5 ppm/°C and typical value of 1 ppm/°C. This corresponds to worst case gain shifts of 2 LSBs and 0.4 LSBs respectively over a 100°C temperature range. When trim resistors R1(R3) and R2(R4) are used to adjust full-scale range as in Figure 4, the temperature coefficient of R1(R3) and R2(R4) should also be taken into account. For further information see "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Application Note, Publication Number E630c-5-3/86 available from Analog Devices.

High Frequency Considerations: AD7547 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor. This is shown as C1 and C2 in Figures 4 and 5.

Feedthrough: The dynamic performance of the AD7547 depends upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 4 is shown in Figure 10 which minimizes feedthrough from V_{REFA}, V_{REFB} to the output in multiplying applications.

MICROPROCESSOR INTERFACING

The AD7547 is designed for easy interfacing to 16-bit microprocessors. Figures 11 and 12 show the interface circuits for two of the most popular 16-bit microprocessors; the 8086 and the 68000. Note that the amount of external logic needed is minimal.

Since data is loaded into the DAC registers on the rising edge of WR, the possibility of invalid data being loaded temporarily to the DAC is removed. This considerably eases the interface circuit design.

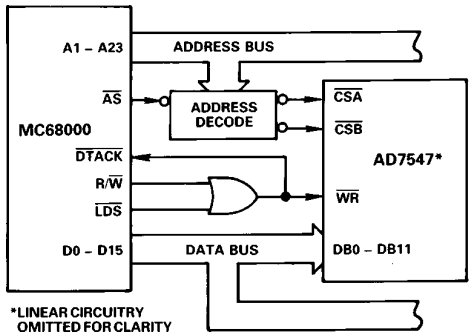


Figure 11. AD7547-MC68000 Interface

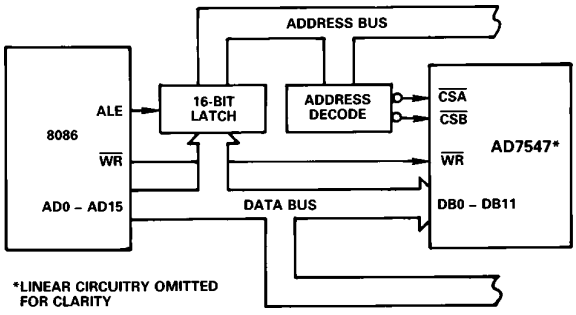
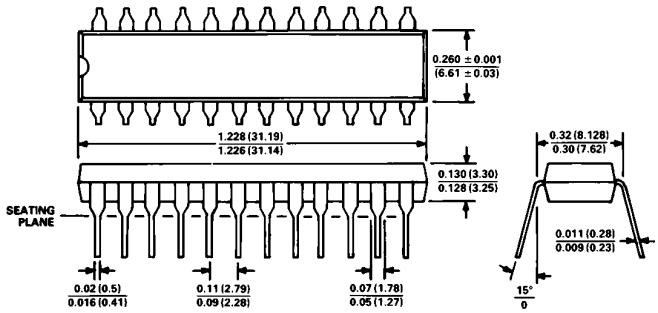


Figure 12. AD7547-8086 Interface

OUTLINE DIMENSIONS

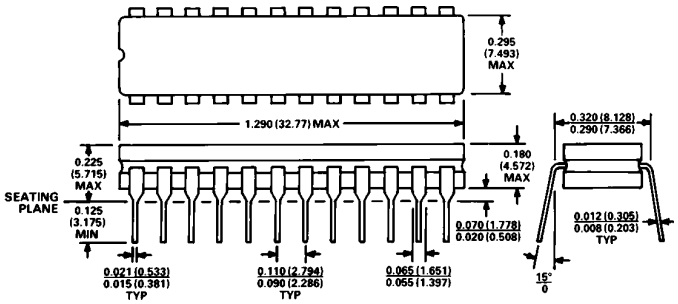
Dimensions shown in inches and (mm).

24-Pin Plastic DIP (N-24)



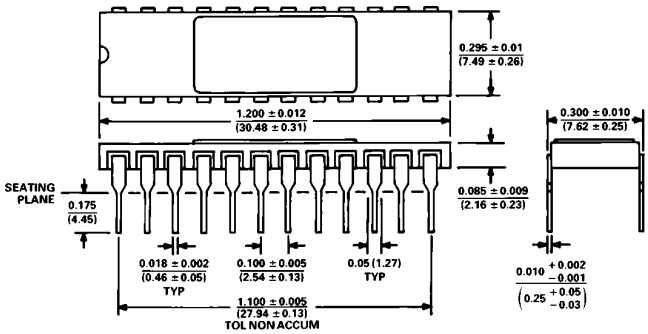
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Pin Cerdip (Q-24)



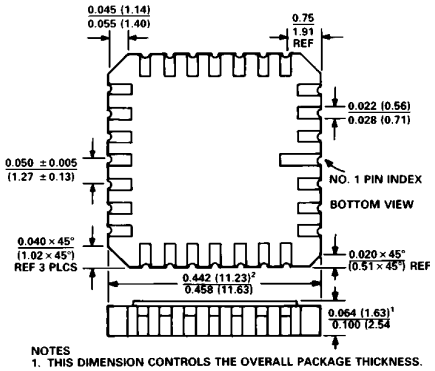
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Pin Ceramic DIP (D-24A)



NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-385 TO REQUIREMENTS.
3. METAL LID IS CONNECTED TO DGND.

28-Terminal Leadless Ceramic Chip Carrier (E-28A)



NOTES
1. THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2. APPLIES TO ALL FOUR SIDES.
3. ALL TERMINALS ARE GOLD PLATED.

28-Terminal Plastic Leaded Chip Carrier (P-28A)