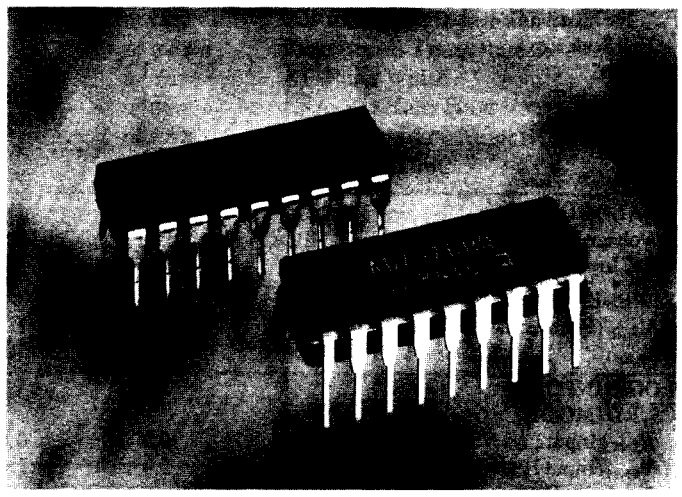
ANALOG DEVICES

LC²MOS 10µs µP Compatible 8-Bit ADC

AD7576

FEATURES
- **Single +5V Operation with External Positive Reference**
- **Fast Conversion Time: 10µs**
- **No Missed Codes Over Full Temperature Range**
- **Microprocessor Compatible**
- **Low Cost**
- **Low Power (15mW)**
- **100ns Data Access Time**



GENERAL DESCRIPTION

The AD7576 is a low cost, low power, microprocessor compatible 8-bit analog-to-digital converter, which uses the successive approximation technique to achieve a fast conversion time of 10µs. The device is designed to operate with an external reference of +1.23V (standard bandgap reference) and converts input signals from 0V to $2V_{REF}$.

The part is designed for ease of microprocessor interface with three control inputs ($\overline{CS}$, $\overline{RD}$ and MODE) controlling all ADC operations such as starting conversion and reading data. The interface logic allows the part to be easily configured as a memory mapped device. All data outputs use latched, three-state output buffer circuitry to allow direct connection to a microprocessor data bus or system input port. The output latches serve to make the conversion process transparent to the microprocessor.

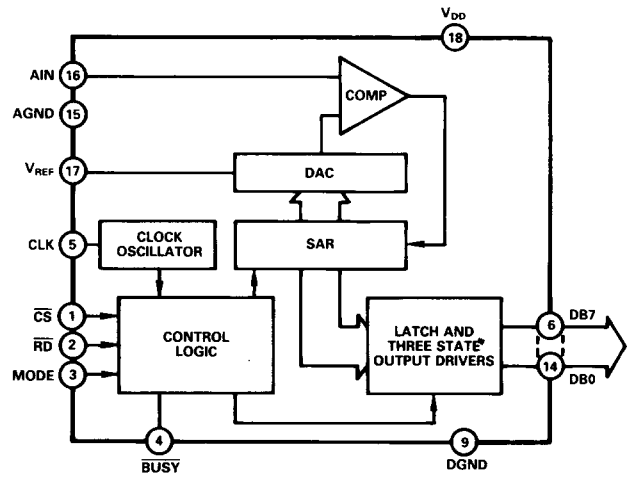
The part is designed for single +5V operation, has on-board comparator, interface logic, and internal/external clock option. This makes the AD7576 ideal for most ADC/µP interface applications.

The AD7576 is fabricated in an advanced, all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process and is packaged in a small, 0.3" wide, 18-pin DIP.

PRODUCT HIGHLIGHTS

1. Single Supply Operation
   Operation from a single +5V supply with a +1.23V reference allows operation of the AD7576 with microprocessor systems without any additional power supplies.
2. Low Power
   CMOS fabrication of the AD7576 results in a very low power dissipation figure of 15mW typical.
3. Versatile Interface Logic
   The AD7576 can be configured to perform continuous conversions or to convert on command. It can be interfaced as SLOW-MEMORY or ROM, allowing versatile interfacing to most microprocessors.
4. Fast Conversion Time
   The fabrication of the AD7576 on Analog Devices' Linear Compatible CMOS (LC²MOS) process enables fast conversion times of 10µs, eliminating the need for expensive Sample-and-Holds in many low frequency applications.

AD7576 FUNCTIONAL DIAGRAM



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SPECIFICATIONS

(V_{DD} = +5V; V_{REF} = +1.23V; AGND = DGND = 0V; f_{CLK} = 2MHz external; All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	AD7576JN[1] AD7576AQ	AD7576KN AD7576BQ	AD7576SQ	AD7576TQ	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	
Relative Accuracy	±1	±½	±1	±½	LSB max	
Minimum Resolution for which						
No Missing Codes is Guaranteed	8	8	8	8	Bits max	
Full Scale Error						
25°C	±1	±1	±1	±1	LSB max	Full Scale TC is typically 5ppm/°C
T_{min} to T_{max}	±1	±1	±1	±1	LSB max	
Offset Error[2]						
25°C	±½	±½	±½	±½	LSB max	Offset TC is typically 5ppm/°C
T_{min} to T_{max}	±½	±½	±½	±½	LSB max	
ANALOG INPUT						
Voltage Range	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	Volts	1LSB = $2V_{REF}$/256; See Figure 4
DC Input Impedance	10	10	10	10	MΩ min	
REFERENCE INPUT						
V_{REF} (For specified Performance)	1.23	1.23	1.23	1.23	Volts	±5%
I_{REF}	500	500	500	500	μA max	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, MODE						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{IN}, Input Current						
25°C	±1	±1	±1	±1	μA max	V_{IN} = 0 or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Input Capacitance[3]	10	10	10	10	pF max	
CLK						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{INL}, Input Low Current	700	700	800	800	μA max	V_{INL} = 0V
I_{INH}, Input High Current	700	700	800	800	μA max	V_{INH} = V_{DD}
LOGIC OUTPUTS						
$\overline{BUSY}$, DB0 to DB7						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40μA
DB0 to DB7						
Floating State Leakage Current	±1	±1	±10	±10	μA max	V_{OUT} = 0 to V_{DD}
Floating State Output Capacitance[3]	10	10	10	10	pF max	
CONVERSION TIME[4]						
With External Clock	10	10	10	10	μs	f_{CLK} = 2MHz
With Internal Clock, T_A = 25°C	10	10	10	10	μs min	Using recommended clock
	20	20	20	20	μs max	components shown in Figure 3.
POWER REQUIREMENTS[5]						
V_{DD}	+5	+5	+5	+5	Volts	±5% for Specified Performance
I_{DD}	6	6	7	7	mA max	Typically 3mA with V_{DD} = +5V
Power Dissipation	15	15	15	15	mW typ	
Power Supply Rejection	±¼	±¼	±¼	±¼	LSB max	4.75V≤V_{DD}≤5.25V

NOTES

[1]Temperature Ranges are as follows:
AD7576JN, KN 0 to +70°C
AD7576AQ, BQ −25°C to +85°C
AD7576SQ, TQ −55°C to +125°C

[2]Offset error is measured with respect to an ideal first code transition which occurs at 1/2LSB.

[3]Sample tested at 25°C to ensure compliance.

[4]Accuracy may degrade at conversion times other than those specified.

[5]Power supply current is measured when AD7576 is inactive i.e. when $\overline{CS}$ = $\overline{RD}$ = MODE = $\overline{BUSY}$ = logic HIGH.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +5V, V_{REF} = +1.23V, AGND = DGND = 0V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, A, B Grades)	Limit at T_{min}, T_{max} (S, T Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	100	100	120	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	100	100	120	ns max	Data Access Time after $\overline{RD}$
t_4	100	100	120	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	80	80	100	ns max	Data Access Time after $\overline{BUSY}$
t_7[3]	10	10	10	ns min	Data Hold Time
	80	80	100	ns max	
t_8	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Delay

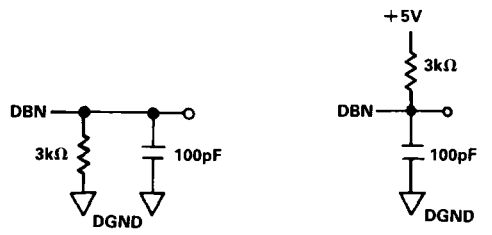
NOTES

[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

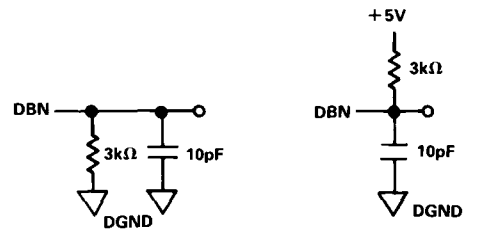
[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Data Hold Time Test

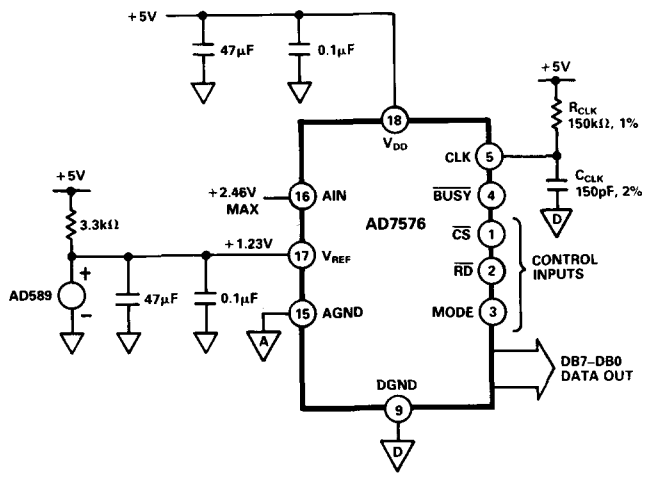


Figure 3. AD7576 Operational Diagram

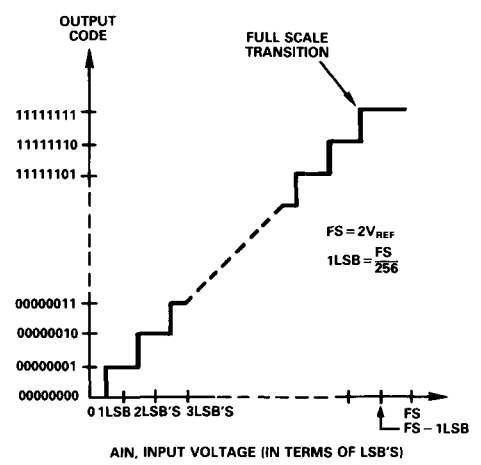


Figure 4. Nominal Transfer Characteristic for Unipolar Operation

ABSOLUTE MAXIMUM RATINGS*

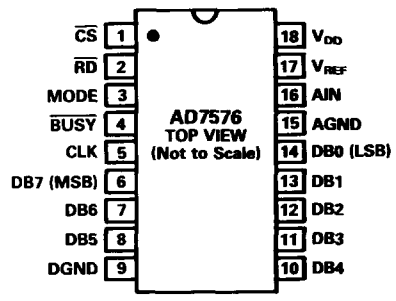
V_{DD} TO AGND	−0.3V, +7V
V_{DD} TO DGND	−0.3V, +7V
AGND TO DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND (Pins 1-3)	−0.3V, V_{DD}
Digital Output Voltage to DGND (Pins 4, 6-8, 10-14)	−0.3V, V_{DD}
CLK Input Voltage (Pin 5) to DGND	−0.3V, V_{DD}
V_{REF} to AGND	−0.3V, V_{DD}
AIN TO AGND	−0.3V, V_{DD}
Operating Temperature Range	
JN, KN	0 to +70°C
AQ, BQ	−25°C to +85°C
SQ, TQ	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 secs)	300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above 75°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATION



ORDERING INFORMATION

Relative Accuracy (T_{min} to T_{max})	Temperature Range and Package: Plastic 0 to +70°C	Cerdip[1] −25°C to +85°C	Cerdip[1] −55°C to +125°C
±1LSB	AD7576JN	AD7576AQ	AD7576SQ
±½LSB	AD7576KN	AD7576BQ	AD7576TQ

NOTE

[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

An ADC with 8-bits resolution can resolve 1 part in 2^8 (i.e., 256) of full scale. For the AD7576 with +2.46V full scale one LSB is 9.61mV.

TOTAL UNADJUSTED ERROR

This is a comprehensive specification which includes full scale error, relative accuracy and offset error.

RELATIVE ACCURACY

Relative Accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the devices measured first LSB transition point and the measured full scale transition point.

FULL SCALE ERROR (GAIN ERROR)

The gain of a unipolar ADC is defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation of the actual span from the ideal span of FS – 2LSB's.

ANALOG INPUT RANGE

With V_{REF} = +1.23V the maximum analog input voltage range is 0 to +2.46V. The output data in LSB's is related to the analog input voltage by the integer value of the following expression:

$$\text{Data (LSB's)} = \frac{256\ \text{AIN}}{2V_{REF}} + 0.5$$

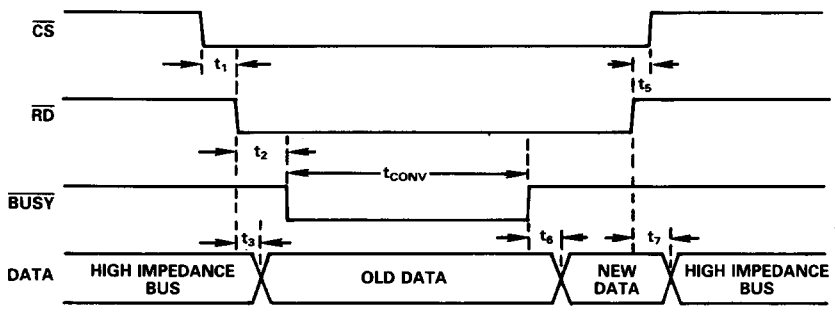


Figure 5. Slow Memory Interface Timing Diagram

TIMING AND CONTROL OF THE AD7576

The AD7576 is capable of two basic operating modes which are outlined in the timing diagrams below. These two operating modes are an Asynchronous Conversion Mode and a Synchronous Conversion Mode. The selection of the required operating mode is determined by the status of the MODE pin. When this pin is HIGH, the device performs conversions only when the required control signals ($\overline{CS}$ and $\overline{RD}$) are applied; with this pin LOW the device performs continuous conversions and $\overline{CS}$ and $\overline{RD}$ are used only to access the output data.

SYNCHRONOUS CONVERSION MODE

In the Synchronous Conversion mode the AD7576 will perform a conversion when requested to do so by the microprocessor. The MODE pin of the AD7576 is tied HIGH to place the device in Synchronous Conversion operation. Two interface options exist for reading the output data from the AD7576.

Slow Memory Interface

The first of these interface options is intended for use with microprocessors which can be forced into a WAIT STATE for at least 10μs (such as the 8085A). The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7576 address. $\overline{BUSY}$ subsequently goes LOW (forcing the microprocessor READY input LOW) placing the processor in a WAIT state. When conversion is complete ($\overline{BUSY}$ goes HIGH) the processor completes the memory READ.

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT, and then READ data with a single READ instruction. The fast conversion time of the

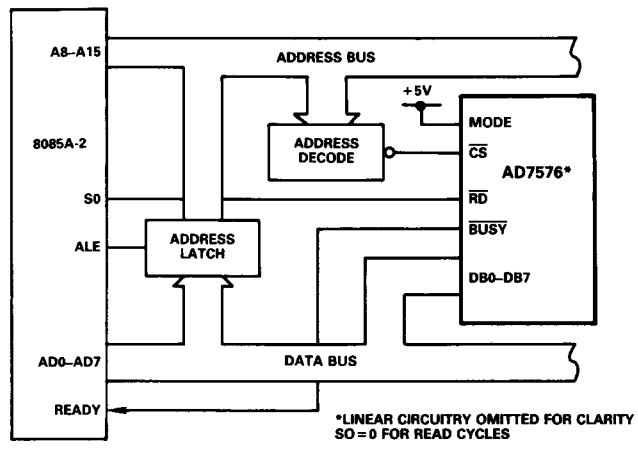


Figure 6. AD7576 to 8085A-2 Slow Memory Interface

AD7576 ensures that the microprocessor is not placed in a WAIT state for an excessive amount of time. The timing diagram for this interface is shown in Figure 5.

Faster versions of many processors, including the 8085A-2, test the condition of the READY input very soon after the start of an instruction cycle. Therefore, $\overline{BUSY}$ of the AD7576 must go LOW very early in the cycle for the READY input to be effective in forcing the processor into a WAIT state. When using the 8085A-2, the processor S0 status signal provides the earliest possible indication that a READ operation is about to occur. Hence, S0 (which is 0 for a READ cycle) provides the READ signal to the AD7576. The AD7576 connection diagram to the 8085A-2 is shown in Figure 6.

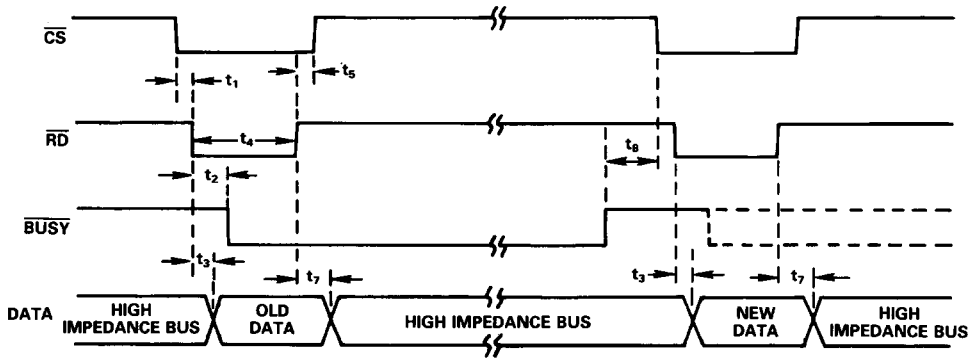


Figure 7. ROM Interface Timing Diagram

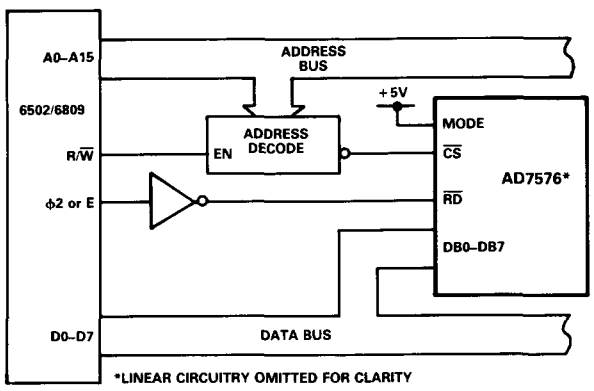


Figure 8. AD7576 to 6502/6809 ROM Interface

ROM Interface

The alternative interface option in the Synchronous Conversion mode avoids placing the microprocessor into a WAIT state. In this interface, conversion is started with the first read instruction and a second read instruction accesses the data and starts a second conversion. The timing diagram for this interface is shown in Figure 7 while Figure 8 shows the connection diagram for the AD7576 with the 6502/6809 microprocessors.

Conversion is initiated by executing a memory READ instruction to the AD7576 address. Data is also obtained from the AD7576 during this instruction. This is old data and may be disregarded if not required. $\overline{BUSY}$ goes LOW during conversion and returns HIGH when conversion is complete.

The $\overline{BUSY}$ line may be used to generate an interrupt to the microprocessor indicating that conversion is complete. The processor then reads the newly-converted data. Alternatively, the delay between the convert start (first READ instruction) and the data READ (second READ instruction) must be at least as great as the AD7576 conversion time. For the AD7576 to operate correctly in the ROM Interface mode $\overline{CS}$ and $\overline{RD}$ should not go low before $\overline{BUSY}$ returns HIGH.

Normally, the second READ instruction starts another conversion as well as accessing the output data. However, if $\overline{CS}$ and $\overline{RD}$ are brought LOW within one external clock period of $\overline{BUSY}$ going HIGH then a second conversion does not occur.

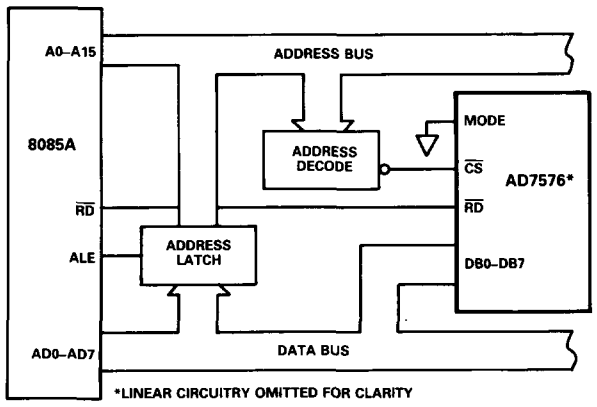


Figure 10. AD7576 to 8085A Asynchronous Conversion Mode Interface

ASYNCHRONOUS CONVERSION MODE

When the MODE pin of the AD7576 is tied LOW, the device performs continuous conversions, and the control lines $\overline{CS}$ and $\overline{RD}$ are used only to read the data from the converter. The timing diagram for this operating mode is outlined in Figure 9, with the connection diagram to the 8085A shown in Figure 10.

Data is obtained from the AD7576 by executing a memory READ instruction to its address. The A/D process is completely transparent to the microprocessor and the AD7576 will behave like a ROM. Data may be read at any time completely independent of the clock. This is especially useful in internal clock applications where the user no longer has to worry about synchronizing the clock with the READ line of the microprocessor.

The data latches are normally updated by $\overline{BUSY}$ going HIGH. However, if $\overline{CS}$ and $\overline{RD}$ are LOW when $\overline{BUSY}$ goes HIGH, the contents of the data latches are frozen until $\overline{CS}$ or $\overline{RD}$ returns HIGH. This ensures that incorrect data cannot be read from the AD7576. The output latches are updated when $\overline{CS}$ or $\overline{RD}$ return HIGH and the converter is re-enabled. If $\overline{CS}$ or $\overline{RD}$ do not return HIGH the AD7576 will stop performing continuous conversions, and will not start again until either line goes HIGH.

The advantage of this mode is its simplicity. The disadvantage of this mode is that the data which is read is not clearly defined in time. However, it will not be older than one conversion period and if this uncertainty is a problem it can be overcome by monitoring the $\overline{BUSY}$ line.

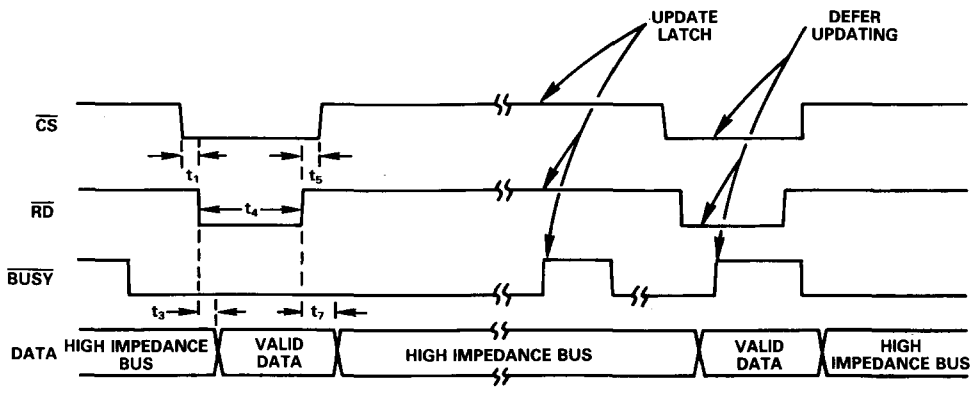


Figure 9. Asynchronous Conversion Mode Timing Diagram

Mode Pin	Operating Mode	Device Operation
High	Synchronous Conversion	1. $\overline{BUSY}$ connected to µP ready input. Memory Read instruction starts conversion. µP is driven into wait state for duration of AD7576 conversion. 2. Memory Read instruction starts conversion. $\overline{BUSY}$ generates interrupt when conversion is complete. Second Memory Read instruction reads newly-converted data. Alternatively, when software delay between the two read instructions is longer than conversion time, the second read instruction will access the newly-converted data. In both cases the second read normally starts a second conversion.
Low	Asynchronous Conversion	AD7576 performs continuous conversions. The data may be read from the device independent of CLK by executing a Memory Read instruction.

Table I. AD7576 Operating Modes

A SAMPLED-DATA INPUT

The AD7576 makes use of a sampled-data comparator. The equivalent input circuit is shown in Figure 11. When a conversion starts, switch S1 is closed and the equivalent input capacitance is charged to V_{IN}. With a switch resistance of typically 500Ω and an input capacitance of typically 2pF the input time constant is 1ns. Thus C_{IN} becomes charged to within ±¼ LSB in 6.9 time constants or about 7ns. Since the comparator switches are operating at one half the input clock frequency of 2MHz, there is ample time for the input voltage to settle before the comparator decision is made (at the end of a clock period). Increasing the source resistance increases the settling time required. Input bypass capacitors placed directly at the analog input act to average the input charging currents. This average current flowing through any source impedance can cause full-scale errors.

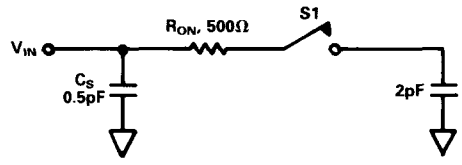


Figure 11. AD7576 Equivalent Input Circuit

INTERNAL/EXTERNAL CLOCK

The AD7576 can be used with either its own internal clock or with an externally applied clock. In either case, the clock signal appearing at the CLK pin is divided internally by two to provide an internal clock signal for the AD7576. A single conversion lasts for 20 input clock cycles (10 internal clock cycles).

INTERNAL CLOCK

Clock pulses are generated by the action of the external capacitor (C_{CLK}) charging through an external resistor (R_{CLK}) and discharging through an internal switch. When a conversion is complete, the internal clock stops operating. In addition to conversion, the internal clock also controls the automatic internal reset of the SAR. This reset occurs at the start of each conversion cycle during the first internal clock pulse.

Nominal conversion times versus temperature for the recommended R_{CLK} and C_{CLK} combination are shown in Figure 12.

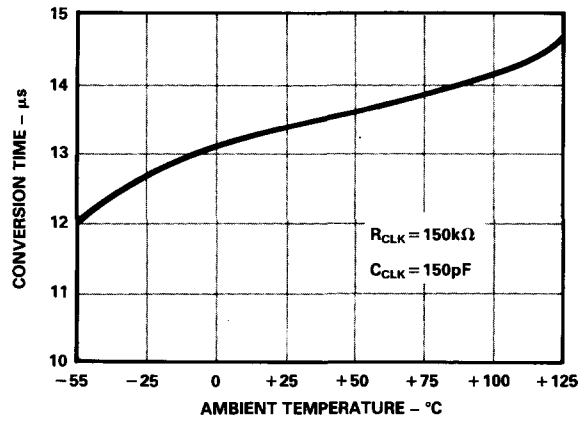


Figure 12. Typical Conversion Time vs. Temperature Using Internal Clock

The internal clock is useful in that it provides a convenient clock source for the AD7576. Due to process variations, the actual operating frequency for this R_{CLK}/C_{CLK} combination can vary from device to device by up to ±30%. For this reason it is recommended that an external clock be used in the following situations;

1. Applications requiring a conversion time which is within 30% of 10µs, the minimum conversion time for specified accuracy. A clock frequency of 2MHz at the CLK pin gives a conversion time of 10µs.
2. Applications where time related software constraints cannot accommodate time differences which may occur due to unit to unit clock frequency variations or temperature.

EXTERNAL CLOCK

The CLK input of the AD7576 may be driven directly from 74HC, 4000 B-series buffers (such as 4049) or from LS TTL with a 5.6kΩ pull-up resistor. When conversion is complete the internal clock is disabled even if the external clock is still applied. This means that the external clock can continue to run between conversions without being disabled. The mark/space ratio of the external clock can vary from 70/30 to 30/70.

APPLICATION HINTS

1. NOISE: Both the input signal lead to AIN, and the signal return lead from AGND should be kept as short as possible to minimize input-noise coupling. In applications where this is not possible, either a shielded cable or a twisted pair transmission line between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible. In general, the source resistance should be kept below 2kΩ. Larger values of source resistance can cause undesired system noise pickup.
2. PROPER LAYOUT: Layout for a printed circuit board should ensure that digital and analog lines are kept separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track.

Both the analog input and the reference input should be screened by AGND. A single point analog ground which is separate from the logic system ground should be established at or near the AD7576. This single point analog ground subsystem should be connected to the digital system ground by a single-track connection only. Any reference bypass capacitors, analog input filter capacitors or input signal shielding should be returned to the analog ground point.

3. OFFSET ERROR: Offset error adjustment in single-supply systems may be easily achieved by means of the offset null facility of an op-amp when used as a voltage follower for the analog input signal AIN (see Figure 13). The op-amp chosen should be able to operate from a single supply and allow a common-mode input voltage range that includes 0V, e.g. TL091. To adjust for zero offset error the input signal source is set to +4.8mV (i.e., ½ LSB) while the 100kΩ potentiometer is varied until the ADC output code flickers between 000...00 and 000....01.
4. FULL-SCALE ADJUST: The full-scale or gain adjustment is made by forcing the analog input AIN to +2.445V (i.e., Full-Scale Voltage – 3/2 LSB). The magnitude of the reference voltage V_{REF} is then adjusted until the ADC output code flickers between 111...10 and 111...11.
5. REFERENCE CIRCUIT: Figure 14 shows how an AD589 can be configured to produce a nominal reference voltage of +1.23V.

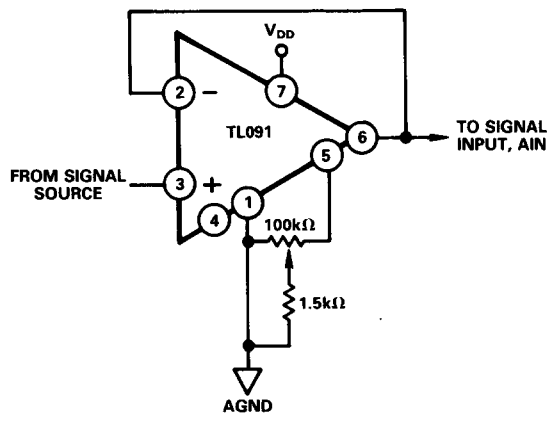


Figure 13. Offset Adjust Circuit

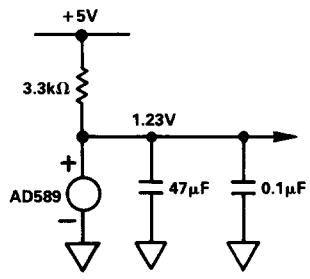
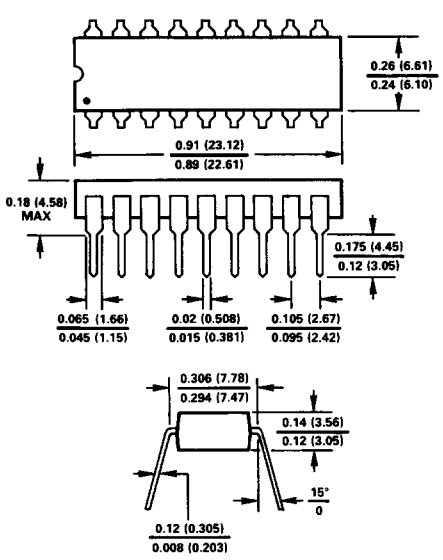


Figure 14. Reference Circuit

MECHANICAL INFORMATION
OUTLINE DIMENSIONS

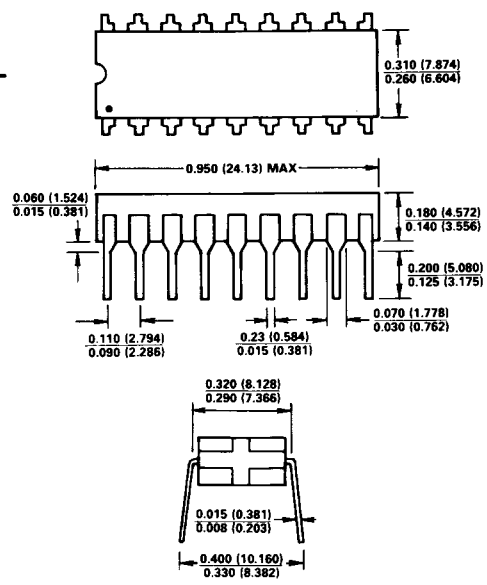
Dimensions shown in inches and (mm).

18-PIN PLASTIC DIP (SUFFIX N)



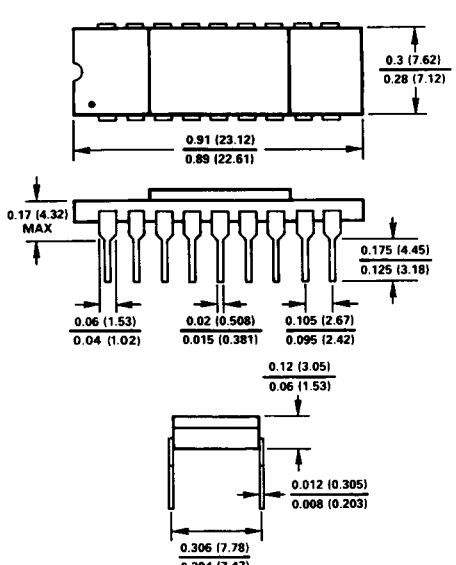
NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

18-PIN CERDIP (SUFFIX Q)



NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

18-PIN CERAMIC



NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.