



DI CMOS Analog Switches with Data Latches

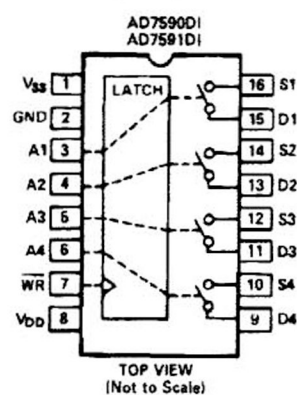
AD7590DI/AD7591DI/AD7592DI

FEATURES

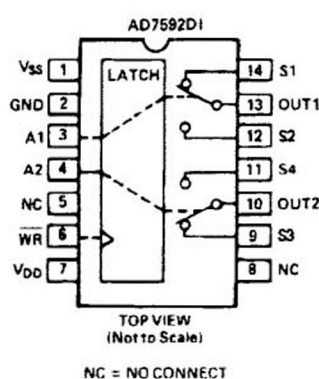
SCR Latch-Proof
Overvoltage-Proof: $\pm 25V$
Low R_{on} : $80\Omega_{typ}$
Buffered Switch Logic
TTL, CMOS Compatible
Monolithic Dielectrically-Isolated CMOS
Pin Compatible with AD7510DI Series

FUNCTIONAL BLOCK DIAGRAMS

16-Pin DIP



14-Pin DIP



GENERAL DESCRIPTION

The AD7590DI, AD7591DI and AD7592DI are a family of protected (latch-proof) dielectrically isolated CMOS switches featuring overvoltage protection up to $\pm 25V$ above the power supplies. Microprocessor interfacing is facilitated by the provision of on-chip data latches.

The AD7590DI and AD7591DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the switch control logic is inverted. The AD7592DI has two independent SPDT switches packaged in a 14-pin DIP.

CONTROL LOGIC ($\overline{WR}$ HELD LOW)

AD7590DI: Switch "ON" for Address "HIGH"

AD7591DI: Switch "ON" for Address "LOW"

AD7592DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

REV. A

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD7590DI/AD7591DI/AD7592DI—SPECIFICATIONS ($V_{DD} = 15V$, $V_{SS} = -15V$ unless otherwise noted)

Parameter	Model	$T_A = +25^\circ\text{C}$ (K, B, T)	$T_A =$ 0 to $+70^\circ\text{C}$ (K) -25°C to $+85^\circ\text{C}$ (B) -55°C to $+125^\circ\text{C}$ (T)	Units	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range	All	± 10	± 10	Volts	$-10V \leq V_S \leq +10V$, $I_{DS} = 1mA$; Test Circuit 1
R_{ON}^1	All	60	120	Ω typ	
R_{ON} Match ²	All	90	150	Ω max	$V_S = 0$, $I_{DS} = 1mA$ $V_S = 0$, $I_{DS} = 1mA$ Test Circuit 2
R_{ON} Match Drift ²	All	2		Ω typ	
$I_{D, OFF}^1$	AD7590DI	0.01		$\Omega/^\circ\text{C}$ typ	Test Circuit 2
	AD7591DI	0.5		nA typ	
I_S OFF ¹	All	5	50	nA max	Test Circuits 2 & 4
	All	0.5		nA typ	
$I_U(I_S)$ ON ¹	All	5	50	nA max	Test Circuit 3
	All	0.5		nA typ	
I_{OUT}^1	AD7592DI	5	50	nA max	Test Circuit 4
	AD7592DI	1		nA typ	
$C_S(C_D)$ OFF ³	All	10	100	nA max	Test Circuit 4
$C_S(C_D)$ ON ³	All	10		pF typ	
$C_{DS}(C_{SS})$ OFF ³	All	30		pF typ	
$C_{DS}(C_{SS})$ ON ³	All	1		pF typ	
$C_{DD}(C_{SS})$ OFF ³	All	0.5		pF typ	
$C_{DD}(C_{SS})$ ON ³	All	0.5		pF typ	
DIGITAL CONTROL					
V_{INI}^1	All	0.8	0.8	V max	$V_{IN} = 0$ or V_{DD}
V_{INH}^1	All	2.4	2.4	V min	
C_{IN}^1	All	7	7	pF typ	
I_{INL} or $I_{INH}^{1,4}$	All	1	1	μA max	
DYNAMIC CHARACTERISTICS					
t_{ON}^2	AD7590DI	250	380	ns max	Test Circuit 5
	AD7591DI	400	500	ns max	
t_{OFF}^2	AD7590DI	400	500	ns max	Test Circuit 5
	AD7591DI	250	380	ns max	
$t_{TRANSITION}^2$	AD7592DI	350	450	ns max	Test Circuit 6
Write Pulse-Width (t_{WR}) ²	All	250	300	ns min	
Address Setup Time (t_{AS}) ²	All	300	300	ns min	See Figure 1
Address Hold Time (t_{AH}) ²	All	20	30	ns min	
Off Isolation ³	All	-85		dB typ	A, $\overline{WR} = 0.8V$; $V_S = 10V$ (Pk-Pk); $f = 1kHz$, $R_L = 10k\Omega$
Crosstalk ³	All	5		mV peak, typ	
Q_{INJ}^3 (Charge Injection)	All	55		pC typ	Test Circuit 7
POWER SUPPLY					
I_{DD}^1	All	1	1.5	mA max	Digital Inputs = V_{INL} or V_{INH}
I_{SS}^1	All	1	1	mA max	

NOTES

¹100% tested.

²Guaranteed, not production tested.

³Typical values for information only, not subject to test.

⁴Inputs are MOS gates typical current less than 10nA.

Specifications subject to change without notice.

TIMING AND CONTROL SEQUENCE

Figure 1 shows the timing sequence for latching the switch address inputs. The latches are level sensitive and, therefore, while $\overline{WR}$ is held low the latches are transparent and the switches respond to the address inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.

NOTE: All digital input signals rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 20ns$.

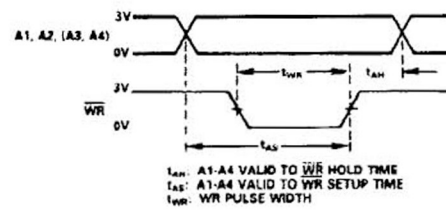


Figure 1. Timing and Control Sequence

AD7590DI/AD7591DI/AD7592DI

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V _{DD} to GND	+17V
V _{SS} to GND	-17V
Overvoltage at V _D (V _S), One Switch Only (1sec surge)	V _{DD} + 25V or V _{SS} - 25V
(Continuous)	V _{DD} + 20V or V _{SS} - 20V or 20mA, Whichever Occurs First
Switch Current (I _{DS} , Continuous)	50mA
Switch Current (I _{DS} , Surge) 1ms Duration, 10% Duty Cycle	150mA
Digital Input Voltage Range	-0.3V to V _{DD} + 0.3V
Power Dissipation (Any Package) Up to +75°C	450mW
Derates above +75°C by	6mW/°C
Storage Temperature	-65°C to +150°C
Operating Temperature	
Plastic (KN Versions)	0 to +70°C
Cerdip (BQ Versions)	-25°C to +85°C
Cerdip (TQ Versions)	-55°C to +125°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model ¹	Temperature Range	Package Option ²
AD7590DIKN	0°C to +70°C	N-16
AD7590DIKP	0°C to +70°C	P-20A
AD7590DIBQ	-25°C to +85°C	Q-16
AD7590DITQ	-55°C to +125°C	Q-16
AD7591DIKN	0°C to +70°C	N-16
AD7591DIKP	0°C to +70°C	P-20A
AD7591DIBQ	-25°C to +85°C	Q-16
AD7591DITQ	-55°C to +125°C	Q-16
AD7592DIKN	0°C to +70°C	N-14
AD7592DIKP	0°C to +70°C	P-20A
AD7592DIBQ	-25°C to +85°C	Q-14
AD7592DITQ	-55°C to +125°C	Q-14

NOTES

¹To order MIL-STD-883C, Class B processed parts, add /883B to part number. Refer to the Analog Devices Military Products Databook (1990) for military data sheet.

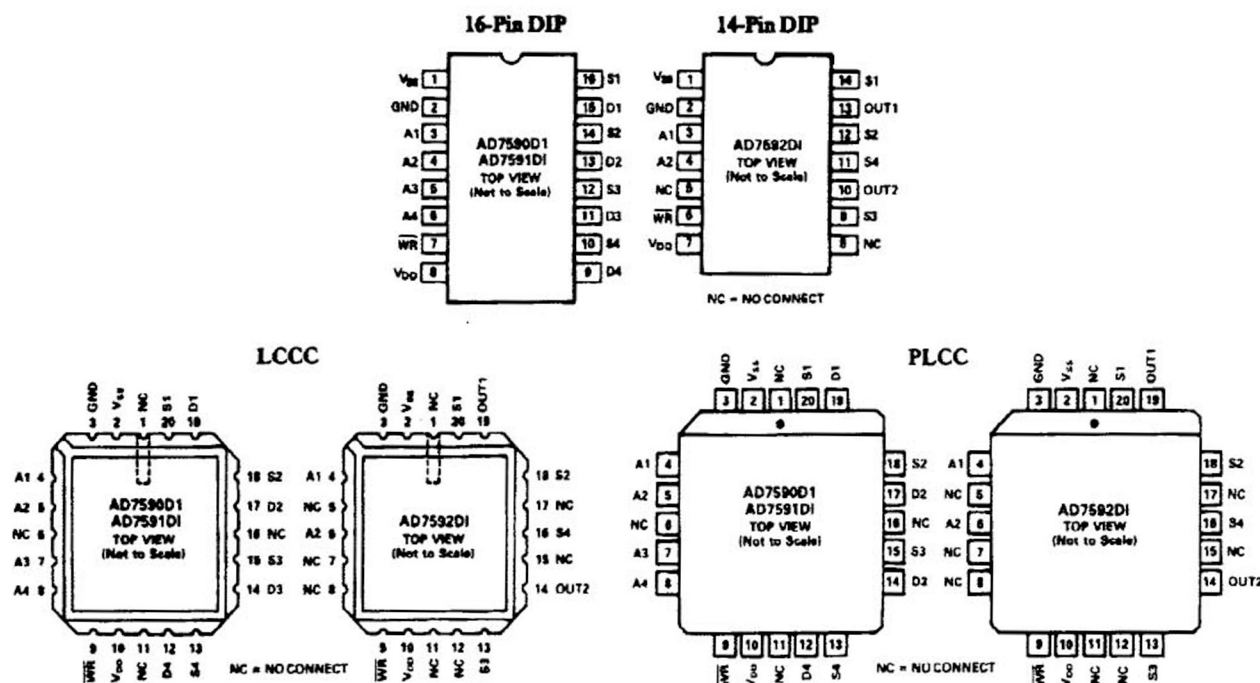
²N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier Q = Cerdip. For Hermetic Surface Mount package, contact your local sales office.

CAUTION:

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



PIN CONFIGURATIONS



AD7590DI/AD7591DI/AD7592DI

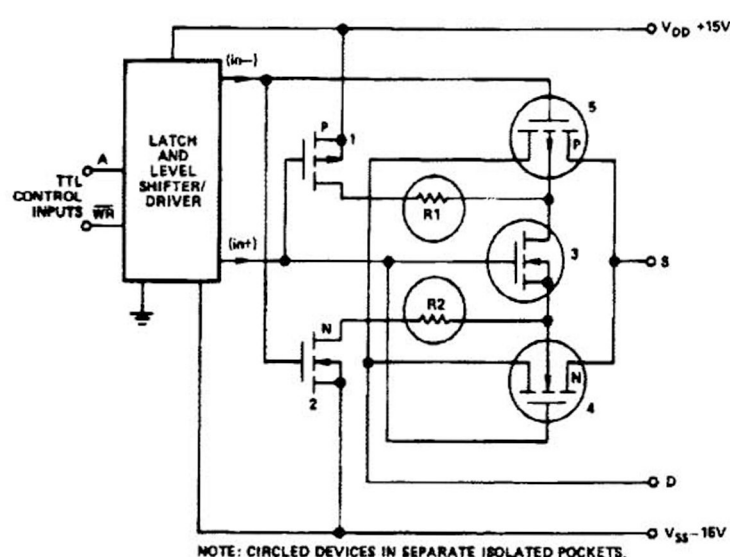


Figure 2. Typical Output Switch Circuitry of AD7590DI Series

CIRCUIT DESCRIPTION

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as R_{ON} or leakage, or provided only limited protection in the event of overvoltage.

The AD7590DI series switches utilize a dielectrically-isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 2. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is V_{DD} and (in-) is V_{SS} from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 is "ON". Hence, the backgates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. The circled devices are located in separate dielectrically isolated pockets. Floating the output switch backgates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter R_{ON} versus V_S response.

For an "OFF" switch, device number 3 is "OFF," and the backgates of devices 4 and 5 are tied through $1k\Omega$ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D (OUT) terminal which exceeds V_{DD} or V_{SS} , the S- or D-to-backgate diode is forward biased; however, R1 and R2 provide current limiting action to the supplies.

An equivalent circuit of the output switch element in Figure 3 shows that, indeed, the $1k\Omega$ limiting resistors are in series with the backgates of the P- and N-channel output devices – not in series with the signal path between the S and D terminals.

It is possible to turn on an "OFF" switch by applying a voltage in excess of V_{DD} or V_{SS} to the S or D terminal. If a positive stress voltage is applied to the S or D terminal which exceeds V_{DD} by a threshold, then the P-channel (device 5) will turn on creating a low impedance path between the S and D terminals. A similar situation exists for negative stress voltages which exceed V_{SS} . In this case the N-channel provides the low impedance path between the S and D terminals. The limiting factor on the overvoltage protection is the power dissipation of the package and is $\pm 20V$ continuous (or 20mA whichever occurs first) above the supply voltages.

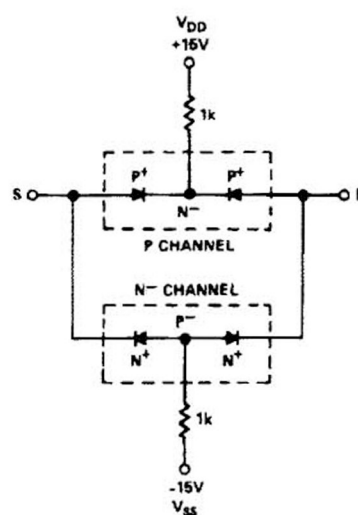
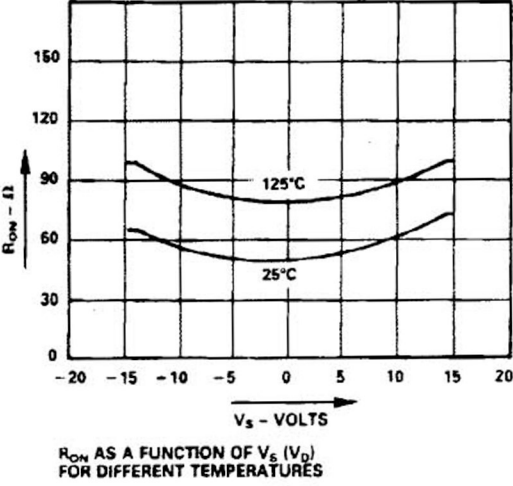
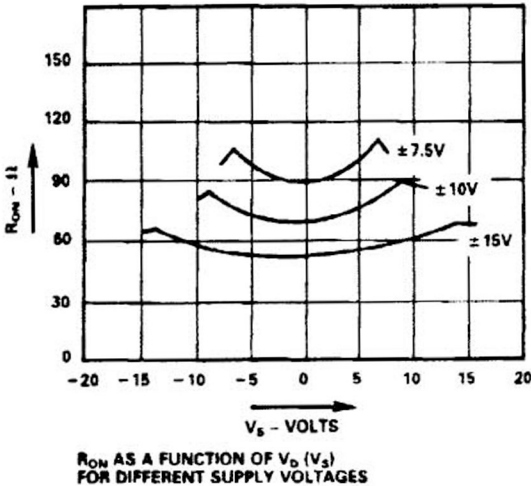
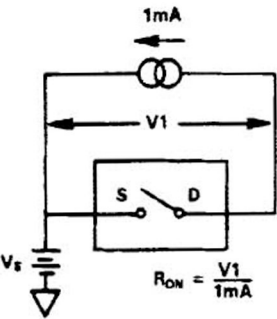


Figure 3. AD7590DI Series Output Switch Diode-Equivalent-Circuit

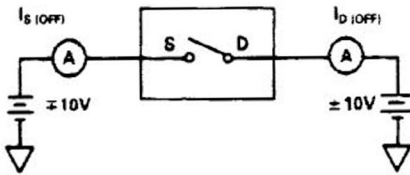
Typical Performance Characteristics and Test Circuits



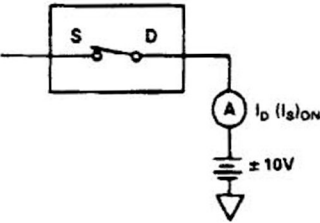
TEST CIRCUIT 1



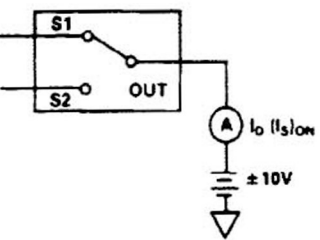
TEST CIRCUIT 2
(AD7590DI, AD7591DI)



TEST CIRCUIT 3

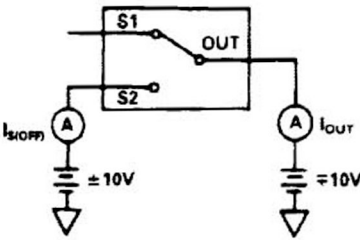


a. AD7590DI, AD7591DI



b. AD7592

TEST CIRCUIT 4
(AD7592DI ONLY)

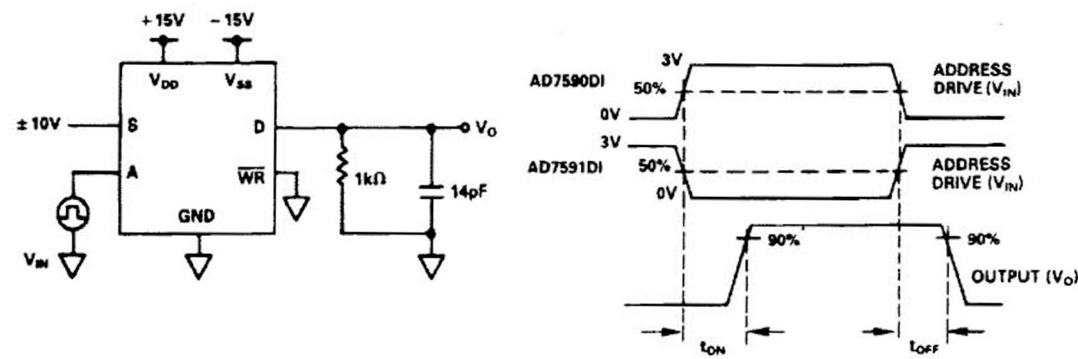


AD7590DI/AD7591DI/AD7592DI

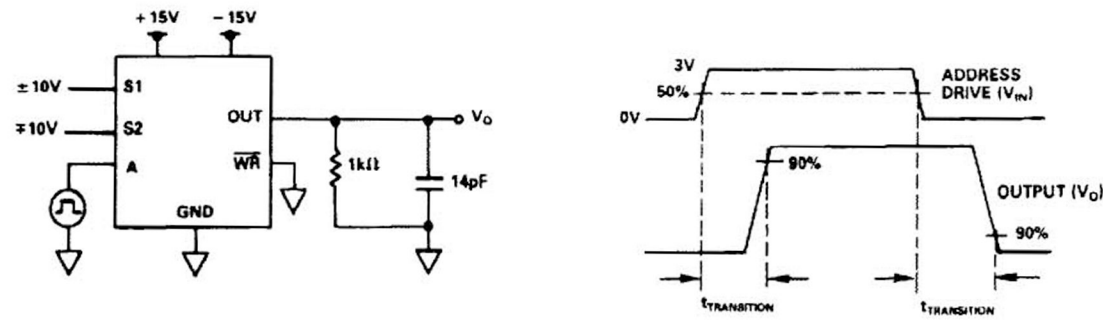
Typical Switching Characteristics and Test Circuits

Note: All digital input signal rise and fall times measured from 10% to 90% of 3V. $t_r = t_f = 20\text{ns}$.

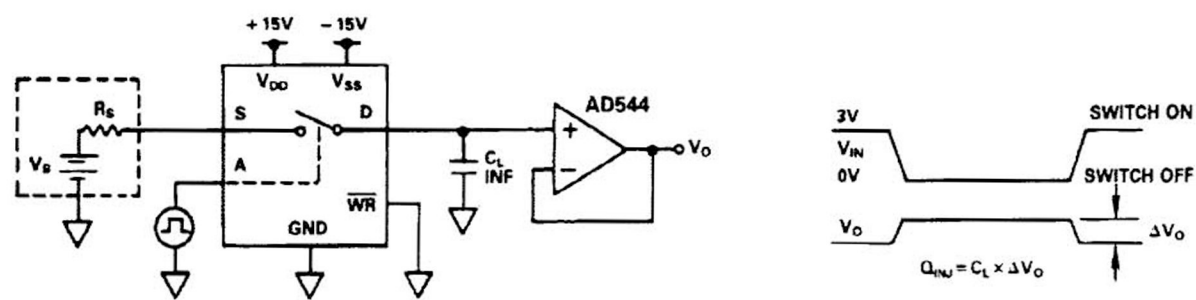
TEST CIRCUIT 5
SWITCHING TIME OF AD7590DI AND AD7591DI, t_{ON} , t_{OFF}



TEST CIRCUIT 6
SWITCHING TIME OF AD7592DI, $t_{TRANSITION}$



TEST CIRCUIT 7
CHARGE INJECTION

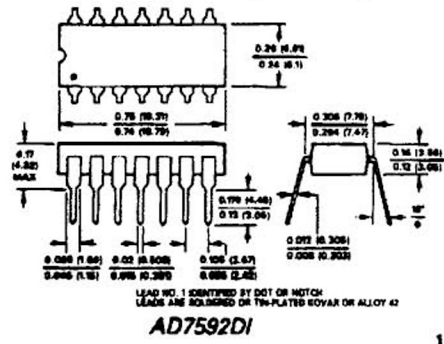


AD7590DI/AD7591DI/AD7592DI

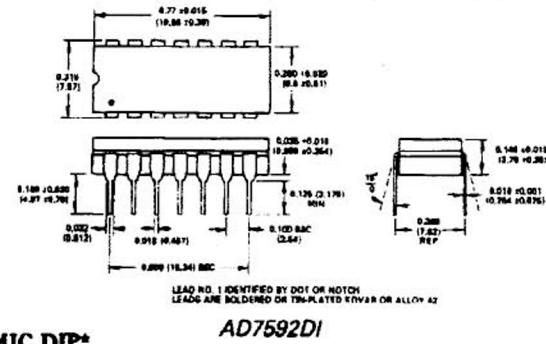
MECHANICAL INFORMATION OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

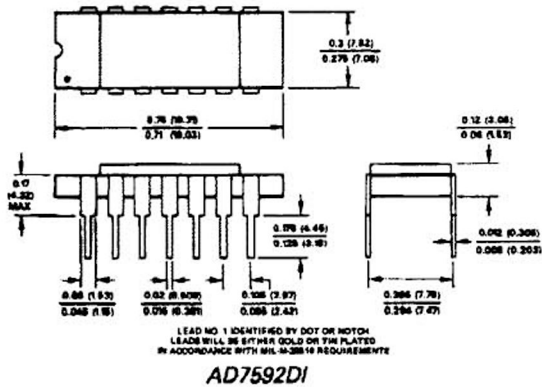
14-PIN PLASTIC DIP (SUFFIX N)



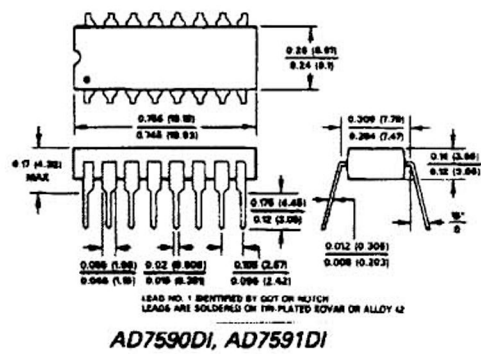
14-PIN CERP DIP PACKAGE (SUFFIX Q)



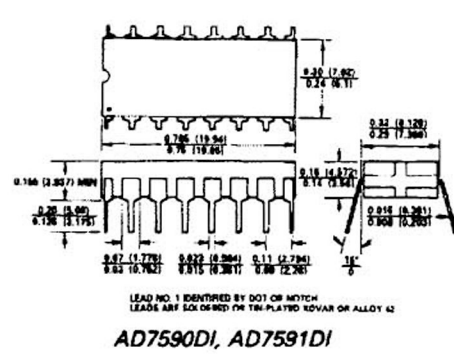
14-PIN CERAMIC DIP*



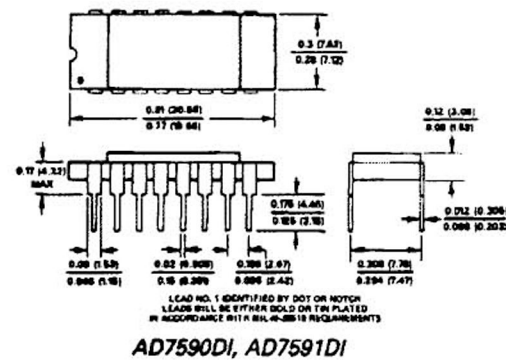
16-PIN PLASTIC DIP (SUFFIX N)



16-PIN CERP DIP PACKAGE (SUFFIX Q)



16-PIN CERAMIC DIP*



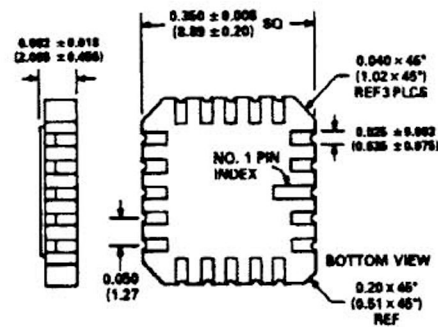
*ANALOG DEVICES RESERVES THE RIGHT TO SHIP CERAMIC
PACKAGES IN LRU OF CERP PACKAGES.

AD7590DI/AD7591DI/AD7592DI

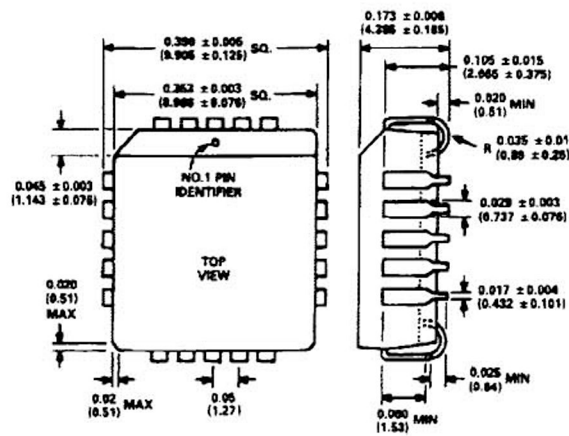
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

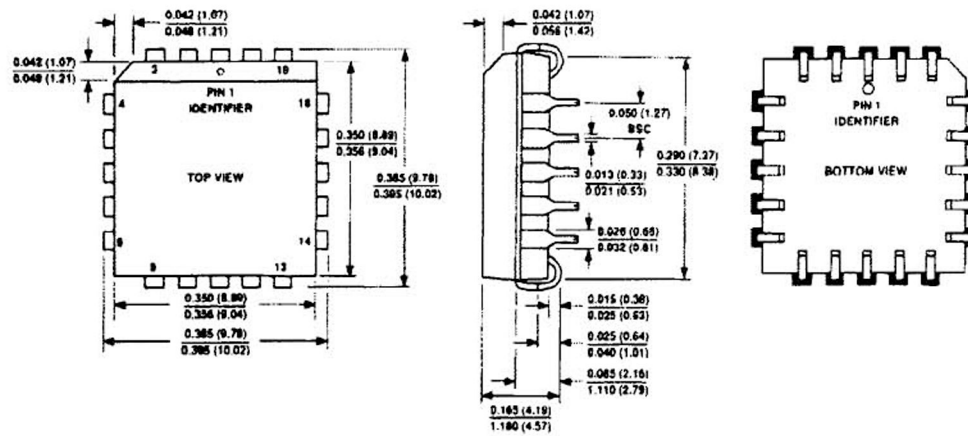
20-TERMINAL LEADLESS CERAMIC CHIP CARRIER (SUFFIX E)



20-TERMINAL PLASTIC LEADED CHIP CARRIER (SUFFIX P)



PLCC (P-20A)



C517C-21-11/86

PRINTED IN U.S.A.