16-BIT Differential ADC in μSO8

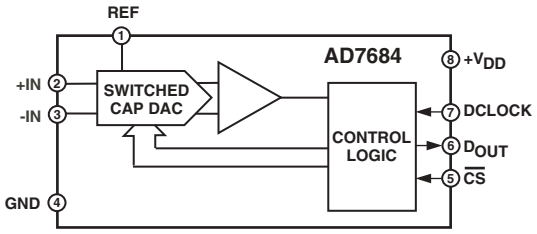
Preliminary Technical Data — AD7684

FEATURES

16 Bits No Missing Codes (B Grade)
INL: ± 1LSB Typ, ± 3LSB Max (B Grade)
True-Differential Analog input range: ± V_{REF}
0V to V_{REF} with V_{REF} up to VDD on both Inputs
No Pipeline Delay
Single Supply Operation 5V and 2.7V
Serial Interface SPI/QSPI/μWire/DSP compatible
Power Dissipation : 4.5 mW Typ @ 3V/100ksps,
0.45 mW @ 10 kSPS
Stand-by current (acquisition phase): 1 μA Max
μ-SO8 Package
Improved 2nd Source to ADS8321

Battery Powered Equipment
Data Acquisition
Instrumentation
Medical Instruments
Process Control

FUNCTIONAL BLOCK DIAGRAM



μSO/SOT23 16 Bit ADC

Type / kSPS	100 kSPS	250 kSPS	380 - 550 kSPS
True Differential	AD7684	AD7687	AD7688
Pseudo Differential	AD7683	AD7685	AD7686
Unipolar	AD7680		

GENERAL DESCRIPTION

The AD7684 is a 16-bit charge redistribution successive-approximation, truly differential Analog-to-Digital Converter which operates from a single power supply from 2.7V to 5.5V. It contains a high-speed 16-Bit sampling ADC without any missing codes and a flexible serial interface port. The part also contains a low noise, wide bandwidth, very short aperture delay track/hold circuit which can sample a $\pm V_{REF}$ analog input range. The reference voltage REF is applied externally and can be set up to the supply voltage.

The AD7684 is fabricated using a CMOS process and is housed in an 8-lead μSOIC package with operation specified from –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Superior INL and DNL
The AD7684 has a maximum integral non linearity error of 3 LSBs and 1 LSB typical with no missing 16-bit code.

2. 2.7V or 5V Single Supply Operation
The AD7684 operates from a single supply. Its power dissipation decreases with the throughput rate (for instance, 450 μW at 10 kHz data rate). It consumes 1 μA maximum during the acquisition phase.

3. Serial Interface compatible with SPI and DSP host.

REV. Pr F

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD7684–SPECIFICATIONS

(T_A = -40°C to +85°C, V_{REF} = V_{DD}, V_{DD} = 2.7V to 5.5 V, 100 kSPS unless otherwise noted.)

Parameter	Conditions	AD7684 All Grades Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	+IN+ - (-IN)	$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage	+IN, -IN	–0.3		V_{DD} + 0.3	V
Analog Input CMRR	f_{IN} = TBD kHz		TBD		dB
Leakage Current at 25 °C	100kSPS Throughput		TBD		nA
Input Impedance			See Analog Input Section		
THROUGHPUT SPEED					
Complete Cycle				10	µs
Throughput Rate		0		100	kSPS
DCLOCK Frequency		0		2.9	MHz
REFERENCE					
External Reference Voltage Range		0.5		V_{DD} + 0.3	V
External Reference Current Drain	100kSPS Throughput		TBD		µA
DIGITAL INPUTS					
Logic Levels					
V_{IH}		+2.0		V_{DD} + 0.3	V
V_{IL}		–0.3		+0.8	V
I_{IH}		–1		+1	µA
I_{IL}		–1		+1	µA
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Data Format			Serial 16-Bits Two's complement		
V_{OH}	I_{SOURCE} = –500 µA	V_{DD} – 0.3			V
V_{OL}	I_{SINK} = 500 µA			0.4	V
POWER SUPPLIES					
V_{DD}	Specified Performance	2.7		5.5	V
Operating Current	100 kSPS Throughput				
V_{DD}	V_{DD} = 5V		TBD		mA
	V_{DD} = 3V		TBD		mA
	During acquisition phase[1]		TBD	1000	nA
Power Dissipation[1]	V_{DD}=5V, 100 kSPS Throughput		TBD	TBD	mW
	V_{DD}=5V, 10 kSPS Throughput		TBD	TBD	mW
	V_{DD}=3V, 10 kSPS Throughput		450	TBD	µW
Power-Down Power[1]			TBD		nW
TEMPERATURE RANGE[2]					
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	°C

NOTES
[1]With all digital inputs forced to V_{DD} or GND respectively.
[2]Contact factory for extended temperature range.
[3]LSB means Least Significant Bit. With the 5 V input range, one LSB is 152.6 µV. With the 2.5 V input range, one LSB is 76.3 µV.
[4]See Definition of Specifications section. These specifications do not include the error contribution from the external reference.
[5]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale unless otherwise specified.

Specifications subject to change without notice.

V_{DD} = 5 V

(T_A = -40°C to +85°C, V_{REF} = 5V, 100 kSPS unless otherwise noted.)

Parameter	Conditions	AD7684A			AD7684B			Unit
		Min	Typ	Max	Min	Typ	Max	
DC ACCURACY								
No Missing Codes		15			16			Bits
Integral Linearity Error		–6	±3	+6	–3	±1	+3	LSB[3]
Offset Error[4]			±TBD	±TBD		±TBD	±TBD	LSB
Offset Temperature Drift			±TBD			±TBD		ppm/°C
Gain Error[4]	REF = 5 V			±TBD			±TBD	% of FSR
Gain Error Temperature Drift			±TBD			±TBD		ppm/°C
Transition Noise			0.4			0.4		LSB
Power Supply Sensitivity	V_{DD} = 5 V ± 5%		±TBD			±TBD		LSB
AC ACCURACY								
Signal-to-Noise	f_{IN} = 1 kHz		87		88	91		dB[5]
SFDR	f_{IN} = 1 kHz		100			108		dB
THD	f_{IN} = 1 kHz		–100			–106		dB
S/[N+D]	f_{IN} = 1 kHz		86		88	91		dB
	f_{IN} = 1 kHz, –60 dB Input		27			31		dB
Effective Number of Bits	f_{IN} = 1 kHz		14			14.8		Bits
–3 dB Input Bandwidth			9			9		MHz
Full-Power Bandwidth	f_{IN}, SINAD at -3dB		TBD			TBD		kHz

V_{DD} = 2.7 V

(T_A = -40°C to +85°C, V_{REF} = 2.5V, 100 kSPS unless otherwise noted.)

Parameter	Conditions	AD7684A			AD7684B			Unit
		Min	Typ	Max	Min	Typ	Max	
DC ACCURACY								
No Missing Codes		15			16			Bits
Integral Linearity Error		–6	±3	+6	–3	±1	+3	LSB[3]
Offset Error[4]			±TBD	±TBD		±TBD	±TBD	LSB
Offset Temperature Drift			±TBD			±TBD		ppm/°C
Gain Error[4]	REF = 5 V			±TBD			±TBD	% of FSR
Gain Error Temperature Drift			±TBD			±TBD		ppm/°C
Transition Noise			0.7			0.65		LSB
Power Supply Sensitivity	V_{DD} = 5 V ± 5%		±TBD			±TBD		LSB
AC ACCURACY								
Signal-to-Noise	f_{IN} = 1 kHz		85			86		dB[5]
SFDR	f_{IN} = 1 kHz		96			100		dB
THD	f_{IN} = 1 kHz		–94			–98		dB
S/[N+D]	f_{IN} = 1 kHz		85			86		dB
	f_{IN} = 1 kHz, –60 dB Input		25			26		dB
Effective Number of Bits	f_{IN} = 1 kHz		13.8			14		Bits
–3 dB Input Bandwidth			9			9		MHz
Full-Power Bandwidth	f_{IN}, SINAD at -3dB		TBD			TBD		kHz

NOTES

[1]With all digital inputs forced to V_{DD} or GND respectively.

[2]Contact factory for extended temperature range.

[3]LSB means Least Significant Bit. With the 5 V input range, one LSB is 76.3 µV. With the 2.5 V input range, one LSB is 38.15 µV.

[4]See Definition of Specifications section. These specifications do not include the error contribution from the external reference.

[5]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale unless otherwise specified.

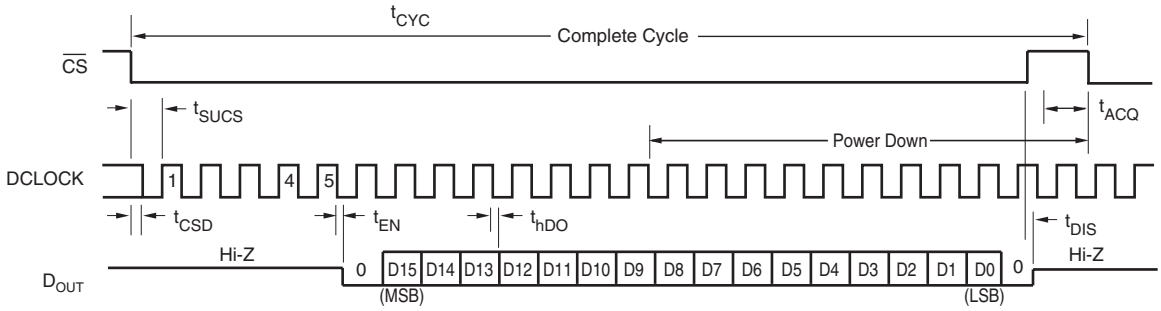
Specifications subject to change without notice.

AD7684–SPECIFICATIONS

TIMING SPECIFICATIONS (–40°C to +85°C, V_{DD}= 2.7 V to 5.5V, unless otherwise stated)

	Symbol	Min	Typ	Max	Unit
Refer to Figure 3					
Throughput rate	t_{CYC}			100	kHz
$\overline{CS}$ Falling to DCLOCK Low	t_{CSD}			0	ns
$\overline{CS}$ Falling to DCLOCK Rising	t_{SUCS}	20			ns
DCLOCK Falling to Data remains Valid	t_{hDO}	5	TBD		ns
$\overline{CS}$ Rising edge to D_{OUT} HiZ	t_{DIS}		TBD	100	ns
DCLOCK Falling to Data Valid	t_{EN}		TBD	50	ns
Acquisition Time	t_{ACQ}	400			ns
D_{OUT} Fall Time	t_F		TBD	25	ns
D_{OUT} Risel Time	t_R		TBD	25	ns

Specifications subject to change without notice.



NOTE: A minimum of 22 clock cycles are required for 16-bit conversion. Shown are 24 clock cycles.
D_{OUT} goes low on the DCLOCK falling edge following the LSB reading.

Figure 3. Serial Interface Timing.

ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs
+IN[2], -IN[2], REF, ... GND –0.3 V to V_{DD} + 0.3 V
Supply Voltages
V_{DD} to GND ..... -0.3 V to 6 V
Digital Inputs to GND ..... –0.3 V to V_{DD} + 0.3 V
Digital Outputs to GND ..... –0.3 V to V_{DD} + 0.3 V
Internal Power Dissipation[3] ..... 325 mW
Junction Temperature ..... 150°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature Range
(Soldering 10 sec) ..... 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]See Analog Input section.
[3]Specification is for device in free air: µSOIC-8: θ_{JA} = 200°C/W.

ORDERING GUIDE

Model	Maximum INL	No Missing Code	Temperature Range	Package Description	Package Option	Brand
AD7684ARM	±6 LSB	15bits	–40°C to +85°C	µSOIC-8	RM-8	C1M
AD7684ARMRL7	±6 LSB	15bits	–40°C to +85°C	µSOIC-8	RM-8 (reel)	C1M
AD7684BRM	±3 LSB	16bits	–40°C to +85°C	µSOIC-8	RM-8	C1D
AD7684BRMRL7	±3 LSB	16bits	–40°C to +85°C	µSOIC-8	RM-8 (reel)	C1D
EVAL-AD7684CB[1]				Evaluation Board		
EVAL-CONTROL BRD2[2]				Controller Board		
EVAL-CONTROL BRD3[2]				Controller Board		

NOTES
[1]This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRDx for evaluation/demonstration purposes.
[2]These boards allow a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

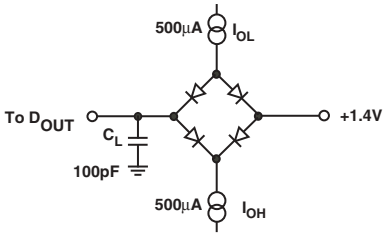
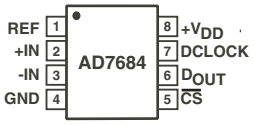


Figure 1. Load Circuit for Digital Interface Timing.

AD7684 PIN CONFIGUTION



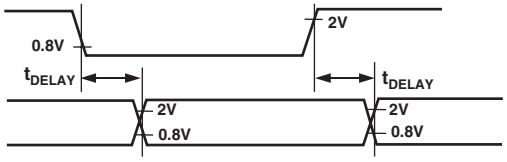


Figure 2. Voltage Reference Levels for Timing.

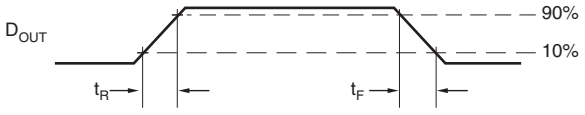


Figure 3. D_{OUT} Rise and Fall Timing.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7684 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin #	Mnemonic		Function
1	REF	AI	Reference Input Voltage. The REF range is from TBD to VDD. It is referred to the GND ground. This pin should be decoupled closely to the pin with a TBD μFcapacitor.
2	+IN	AI	Differential Positive Analog Input.
3	-IN	AI	Differential Negative Analog Input.
4	GND	P	Power Supply Ground.
5	$\overline{CS}$	DI	Chip Select Input. This input has multiple functions. It initiates a complete conversion process on its falling edge. The part returns in shutdown mode as soon as the conversion is done. It also enables D_{OUT}. When high, D_{OUT} is high impedance.
6	D_{OUT}	DO	Serial Data Output.
7	DCLOCK	DI	Serial Data Clock Input. It synchronizes the serial data transfer.
8	V_{DD}	P	Power Supply.

NOTES
AI = Analog Input
DI = Digital Input
DO = Digital Output
P = Power

DEFINITION OF SPECIFICATIONS

INTEGRAL NONLINEARITY ERROR (INL)

Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale". The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

DIFFERENTIAL NONLINEARITY ERROR (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

GAIN ERROR

The last transition (from 111 . . . 10 to 111 . . . 11) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset has been adjusted out.

OFFSET ERROR

The first transition should occur at a level 1/2 LSB above analog ground (38.1 μV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

EFFECTIVE NUMBER OF BITS (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula:

$$ENOB = (S/[N+D]_{dB} - 1.76)/6.02)$$

and is expressed in bits.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

SIGNAL TO (NOISE + DISTORTION) RATIO (S/[N+D])

S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead µSOIC
(RM-8)