LC²MOS Analog I/O Port

AD7774

FEATURES
Four-Channel, 8-Bit, 3.6 µs ADC
Three DACs with On-Chip Amplifiers:
One 11-Bit, 8 µs DAC
Two 8-Bit, 4 µs DACs
Simultaneous/Independent Sampling of Input Channels
Adjustable Span and Bias Voltage for Input Channels
Adjustable Bias Voltage for Output Channels
Operates from +5 V and +12 V Supplies

APPLICATIONS
HDD Dedicated Servo
HDD Hybrid Servo
Closed-Loop Servo Systems

GENERAL DESCRIPTION

The AD7774 is a complete analog I/O port comprising three DACs (two 8-bit and one 11-bit) with output amplifiers, four input channels, two track/hold amplifiers and an 8-bit ADC. It has versatile input and output signal-conditioning features which make it ideal for use in head-positioning servos in dedicated-only and combined dedicated/embedded disk systems and other closed-loop digital servo systems.

The part contains four input channels, grouped in pairs. V_{A1} and V_{A2} share a common track/hold amplifier, Track/Hold A, while V_{B1} and V_{B2} share Track/Hold B. Either single or double conversions can be performed. In single conversion mode, any one of the four input channels can be converted. In double conversion mode, either V_{A1} and V_{B1} or V_{A2} and V_{B2} are simultaneously held by Track/Hold A and Track/Hold B, and the held voltages are sequentially converted.

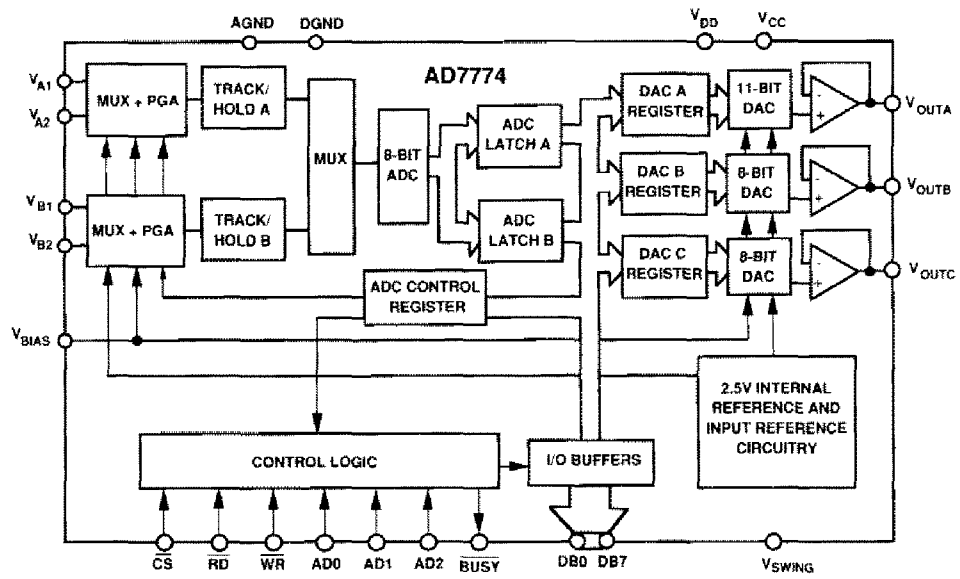
The center point of the transfer function (the bias voltage) can be set for all input and output channels. This makes the AD7774 especially useful in disk drives, where only a positive supply rail is available, as it allows the analog input and output voltages to be referred to a point other than analog ground. In addition, the input span (the swing around the bias voltage) can be set for the input channels. The output span for all three channels is set by the on-chip reference.

The AD7774 operates from +5 V and +12 V supplies. It is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 28-lead dual-in-line (DIP) package and in a 28-terminal plastic leaded chip carrier (PLCC) package.

PRODUCT HIGHLIGHTS

1. The AD7774 contains a four-channel, 3.6 µs ADC with input signal conditioning and three DACs with output amplifiers and output signal conditioning, on a single chip.
2. The midpoint of the ADC transfer function, the input voltage swing of the ADC and the midpoint output voltage of the DACs can be set by applying ground referenced control voltages.
3. The AD7774 interface timing is compatible with most modern microcontrollers and digital signal processors.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD7774—SPECIFICATIONS

ADC SPECIFICATIONS (V_{DD} = +10 V to +13.2 V; V_{CC} = +5 V ± 5%; AGND = DGND = 0 V; V_{BIAS} = +5 V unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	K Version[1]	Units	Conditions/Comments
DC ACCURACY			
Resolution[2]	8	Bits	
Relative Accuracy[3]	±1	LSB max	
Differential Nonlinearity[3]	±1	LSB max	No Missing Codes
Bias Offset Error[3]	±5	LSB max	
Relative Offset Error[3]	±2	LSB max	
Full-Scale Error[3]	±5	LSB max	
ANALOG INPUTS			
Input Voltage Range			
All Inputs	$V_{BIAS} \pm V_{SWING}$	V min to V max	DB0–DB3 of ADC Control Register = 0
All Inputs	$V_{BIAS} \pm V_{SWING}/2$	V min to V max	DB0–DB3 of ADC Control Register = 1
Input Current	±1	mA max	
REFERENCE INPUTS			
Input Voltage Levels			
V_{BIAS}[4]	+3 to +6.8	V min to V max	With Respect to AGND
V_{SWING}			
Internally Generated	+2.325 to +2.675	V min to V max	2.5 V ±7%; Available on V_{SWING} Pin[5]
Internal Tempco	±50	ppm/°C typ	
Externally Applied	+2 to +3	V min to V max	With Respect to AGND for Specified Performance
Input Current			
V_{BIAS} Input	1.5	mA max	
V_{SWING} Input	±100	μA min/μA max	
LOGIC OUTPUTS			
DB0–DB7, $\overline{BUSY}$			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 μA
Floating State Leakage Current	±10	μA max	
Floating State Capacitance[6]	10	pF max	
Output Coding	2s Complement		
LOGIC INPUTS	See DAC Specifications		
CONVERSION TIME	See Timing Characteristics		
POWER REQUIREMENTS			
V_{CC} Range	+4.75/+5.25	V min/V max	For Specified Performance
V_{DD} Range	+10/+13.2	V min/V max	For Specified Performance
I_{DD}	20	mA typ	DACs Loaded with Full Scale; All Analog Inputs = V_{BIAS}
I_{DD}	33	mA max	DACs Loaded with Full Scale; All Analog Inputs = V_{BIAS}
I_{CC}	8	mA max	Logic Inputs = 0.8 V or 2.4 V

NOTES
[1]Temperature range: 0°C to +70°C.
[2]With V_{SWING} = 2.5 V and DB0–DB3 of the ADC Control Register = 0, 1 LSB = (2*V_{SWING})/256 = 19.5 mV.
With V_{SWING} = 2.5 V and DB0–DB3 of the ADC Control Register = 1, 1 LSB = (V_{SWING})/256 = 9.75 mV.
[3]See Terminology.
[4]The maximum V_{BIAS} voltage is limited by the requirement $V_{BIAS} + V_{SWING}$ (or $V_{SWING}/2$) ≤ V_{DD} − 2 V.
[5]The source impedance of the internally generated V_{SWING} is nominally 10 kΩ. If this internally generated V_{SWING} is required for use external to the AD7774, it is recommended that the V_{SWING} output is buffered.
[6]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

DAC SPECIFICATIONS (V_{DD} = +10 V to +13.2 V; V_{CC} = +5 V ± 5%; AGND = DGND = 0 V; V_{BIAS} = +5 V; R_L = 10 kΩ, C_L = 100 pF to AGND.[1] All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	K Version[2]	Units	Conditions/Comments
STATIC PERFORMANCE			
DAC A			
Resolution[3]	11	Bits	
Relative Accuracy[4]	±2	LSB max	
Differential Nonlinearity[4]	±1	LSB max	Guaranteed Monotonic
Bias Offset Error[4]	±50	mV max	
Full-Scale Error[4]	±50	mV max	
DAC B, DAC C			
Resolution[3]	8	Bits	
Relative Accuracy[4]	±1	LSB max	
Differential Nonlinearity[4]	±1	LSB max	Guaranteed Monotonic
Bias Offset Error[4]	±5	LSB max	
Full-Scale Error[4]	±5	LSB max	
ANALOG OUTPUTS			
Output Voltage Range			
All Outputs	$V_{BIAS} - V_{SWING}$ or 1.0	V min	Whichever Is the Higher
	$V_{BIAS} + V_{SWING}$ or $V_{DD} - 2.0$	V max	Whichever Is the Lower
dc Output Impedance	0.5	Ω typ	
REFERENCE INPUTS			
Input Voltage Levels			
V_{BIAS}[5]	+3 to +6.8	V min to V max	With Respect to AGND
V_{SWING}			
Internally Generated	+2.325 to +2.675	V min to V max	2.5 V ±7%; Available on the V_{SWING} Pin[6, 7]
Internal Tempco	±50	ppm/°C typ	
Input Current	As Per ADC Specifications		
AC CHARACTERISTICS[8]			
Voltage Output Settling Time			
DAC A			
Full-Scale Change	3	μs max	Settling Time to Within ±1/2 LSB of Final Value
DAC B, DAC C			
Full-Scale Change	2	μs max	Settling Time to Within ±1/2 LSB of Final Value
Digital-to-Analog Glitch Impulse[4]	15	nV sec typ	
Digital Feedthrough[4]	1	nV sec typ	
LOGIC INPUTS			
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, AD0–AD2, DB0–DB7			
Input Low Voltage, V_{INL}	0.8	V max	
Input High Voltage, V_{INH}	2.4	V min	
Input Leakage Current	10	μA max	
Input Capacitance[8]	10	pF max	
DB0–DB7			
Input Coding	2s Complement		
POWER REQUIREMENTS	See ADC Specifications		

NOTES

[1]The DACs will also operate to specification with a load of 5 kΩ and 100 pF to V_{BIAS}.

[2]Temperature range: 0°C to +70°C.

[3]1 LSB = $(2*V_{SWING})/2^N$, where N is the DAC resolution. 1 LSB = 2.44 mV for DAC A with V_{SWING} = 2.5 V; 1 LSB = 19.5 mV for DAC B, DAC C with V_{SWING} = 2.5 V.

[4]See Terminology.

[5]The maximum V_{BIAS} voltage is limited by the requirement $V_{BIAS} + V_{SWING} \leq V_{DD} - 2$ V.

[6]The source impedance of the internally generated V_{SWING} is nominally 10 kΩ. If this internally generated V_{SWING} is required for use external to the AD7774, it is recommended that the V_{SWING} output is buffered.

[7]DAC output span cannot be adjusted externally, i.e., adjusting V_{SWING} does not change the DAC output span.

[8]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (See Figures 2, 3, 4.)
(V_{DD} = +10 V to +13.2 V, V_{CC} = +5 V ± 5%, AGND = DGND = 0 V.)

Parameter	Limit at T_{min}, T_{max}	Units	Conditions/Comments
t_1[2]	10/65	ns min/ns max	Data Access Time after $\overline{CS}$
t_2[2]	10/65	ns min/ns max	Data Access Time after $\overline{RD}$
t_3[3]	5/45	ns min/ns max	Bus Relinquish Time after $\overline{CS}$
t_4[3]	5/45	ns min/ns max	Bus Relinquish Time after $\overline{RD}$
t_5	10/75	ns min/ns max	Data Access Time after Address Valid; C_L = 50 pF
t_6	58	ns min	$\overline{WR}$ Pulse Width, t_{11} = 58 ns, t_{12} = 18 ns
	128	ns min	$\overline{WR}$ Pulse Width, t_{11} = 128 ns, t_{12} = 0 ns
t_7	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_8	0	ns min	Address Valid to $\overline{WR}$ Setup Time
t_9	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_{10}	0	ns min	Address Valid to $\overline{WR}$ Hold Time
t_{11}	58	ns min	Data Setup Time Prior to $\overline{WR}$ Rising Edge, t_6 = 58 ns, t_{12} = 18 ns
	128	ns min	Data Setup Time Prior to $\overline{WR}$ Rising Edge, t_6 = 128 ns, t_{12} = 0 ns
t_{12}	18	ns min	Data Hold Time after $\overline{WR}$ Rising Edge, $t_6 = t_{11}$ = 58 ns
	0	ns min	Data Hold Time after $\overline{WR}$ Rising Edge, $t_6 = t_{11}$ = 128 ns
t_{13}			ADC Conversion Time; Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{BUSY}$
	3.6	µs max	DB4 of ADC Control Register = 1; C_L = 20 pF
	3.7	µs max	DB4 of ADC Control Register = 1; C_L = 100 pF
	6	µs max	DB4 of ADC Control Register = 0; C_L = 20 pF
	6.1	µs max	DB4 of ADC Control Register = 0; C_L = 100 pF
t_{14}	100	ns max	Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{BUSY}$; C_L = 20 pF
	150	ns max	Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{BUSY}$; C_L = 100 pF
t_{15}	10	ns min	Address Valid to $\overline{CS}$ or $\overline{RD}$ Setup Time
t_{SAMP}	±50	ns max	ADC Channel to Channel Sampling Skew

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_1 and t_2 are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[3]t_3 and t_4 are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the times, t_3 and t_4, quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitance.

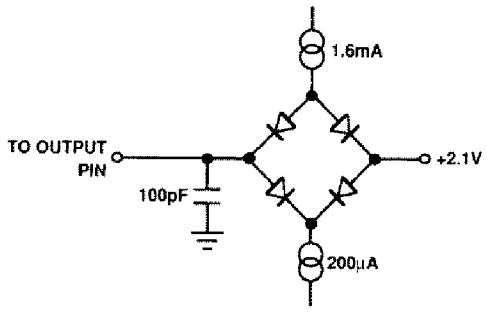


Figure 1. Load Circuits for Timing Measurements

AD7774 ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option*	Price 100s
AD7774KN	0°C to +70°C	±1 LSB	N-28	$35.00
AD7774KP	0°C to +70°C	±1 LSB	P-28A	$36.00

*N = Plastic DIP Pacakge; P = Plastic Leaded Chip Carrier (PLCC) Package.

ABSOLUTE MAXIMUM RATINGS*

T_A = +25°C unless otherwise noted

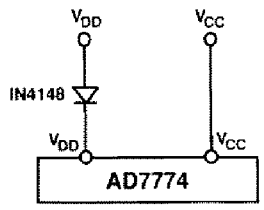
V_{DD} to AGND or DGND . . . . . −0.3 V, +15 V
V_{CC} to DGND . . . . . −0.3 V, V_{DD} + 0.3 V or +7 V (whichever is lower)
AGND to DGND . . . . . −0.3 V, V_{CC} + 0.3 V
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, AD0–AD2 to DGND . . . −0.3 V, V_{DD} + 0.3 V
DB0–DB7, $\overline{BUSY}$ to DGND . . . . . −0.3 V, V_{CC} + 0.3 V
Analog Input Voltage to AGND . . . . . −0.3 V, V_{DD} + 0.3 V
Analog Output Voltage to AGND . . . . −0.3 V, V_{DD} + 0.3 V
Operating Temperature Range
Commercial (K Version) . . . . . 0°C to +70°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 6 mW/°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

Note:
During power supply sequencing some of the absolute maximum rating specifications may be violated. The following specifications are allowed during power-up (for 5 seconds) without causing permanent damage to the device:

1) Digital Input Current, 100 mA.
2) V_{CC} to V_{DD} Current, 3A.

If the V_{CC} supply can provide more than 3A to V_{DD} during power supply sequencing or if V_{CC} can exceed V_{DD} by more than 0.3 V at any other time, the diode protection scheme shown below is recommended;

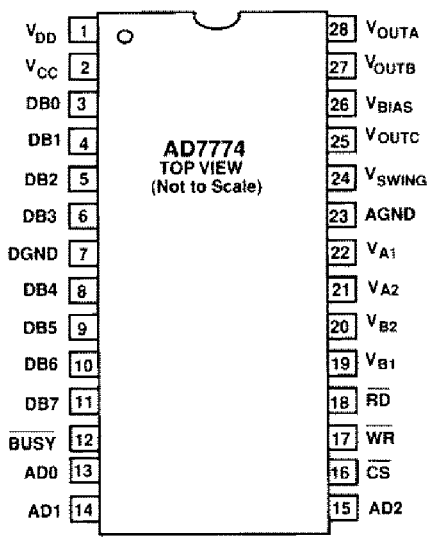


CAUTION

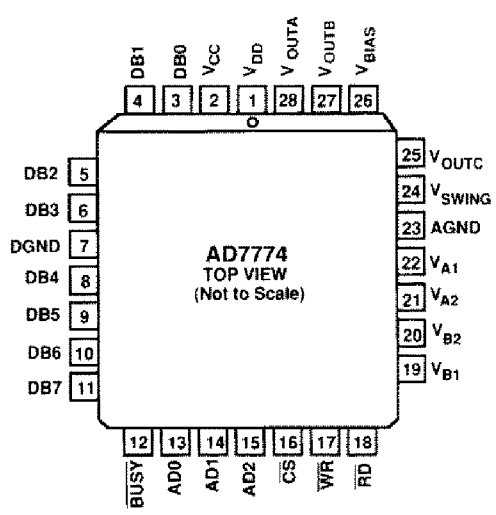
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PIN CONFIGURATIONS

DIP



PLCC



AD7774 PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{DD}	Analog Supply Voltage, +12 V nominal. This is used to power all analog circuitry on the part.
2	V_{CC}	Digital Supply Voltage, +5 V nominal. This is used to power all digital circuitry on the part.
3–6	DB0–DB3	Data Bit 0 to Data Bit 3 of the Input/Output Data Bus. This is a bidirectional data port from which ADC output data may be read and to which DAC input data and ADC Control Register data may be written.
7	DGND	Digital Ground. Ground reference for digital circuitry.
8–11	DB4–DB7	Data Bit 4 to Data Bit 7 of the Input/Output Data Bus. This is a bidirectional data port from which ADC output data may be read and to which DAC input data and ADC Control Register data may be written.
12	$\overline{BUSY}$	BUSY. Active low logic output indicating A/D converter status. The AD7774 is performing an ADC conversion if this output is low.
13–15	AD0–AD2	Address Inputs. These select the internal latches and registers and also the analog input channel to be converted (see TIMING AND CONTROL section).
16	$\overline{CS}$	Chip Select Input. The device is selected when this input is active.
17	$\overline{WR}$	Write Input. Edge-triggered logic input. It is used in conjunction with $\overline{CS}$ and AD0–AD2 to write data to the DAC registers and the ADC Control Register. Data is written to the registers on the rising edge of this $\overline{WR}$ input. The 11 bits of data for DAC A are written from the 8-bit data bus in two write operations. The rising edge of $\overline{WR}$ also starts conversion when AD0–AD2 are set to appropriate values (see ADC Control Register section).
18	$\overline{RD}$	Read Input. Active low logic input. It is used in conjunction with $\overline{CS}$ to enable the data outputs from the ADC latches.
19	V_{B1}	Analog Input B1. This input shares Track/Hold Amplifier B with Analog Input B2. The analog input range is $V_{BIAS} \pm V_{SWING}$ or $V_{BIAS} \pm V_{SWING}/2$. The input voltage on this input and the V_{A1} input are simultaneously sampled.
20	V_{B2}	Analog Input B2. This input shares Track/Hold Amplifier B with Analog Input B1. The analog input range is $V_{BIAS} \pm V_{SWING}$ or $V_{BIAS} \pm V_{SWING}/2$. The input voltage on this input and the V_{A2} input are simultaneously sampled.
21	V_{A2}	Analog Input A2. This input shares Track/Hold Amplifier A with Analog Input A1. The analog input range is $V_{BIAS} \pm V_{SWING}$ or $V_{BIAS} \pm V_{SWING}/2$. The input voltage on this input and the V_{B2} input are simultaneous sampled.
22	V_{A1}	Analog Input A1. This input shares Track/Hold Amplifier A with Analog Input A2. The analog input range is $V_{BIAS} \pm V_{SWING}$ or $V_{BIAS} \pm V_{SWING}/2$. The input voltage on this input and the V_{B1} input are simultaneous sampled.
23	AGND	Analog Ground. Ground reference for analog circuitry.
24	V_{SWING}	Analog Input/Output. The internal voltage reference, which is nominally 2.5 V and provides the span voltage for the input and output channels, is provided at this pin. The output span voltage is 2 V_{SWING} while the input span voltage can be 2 V_{SWING} or V_{SWING}. This pin can also be driven from an external voltage source to allow the span voltage for the input channels to be adjusted. The input voltage range is +2 V to +3 V with respect to AGND. Adjusting this voltage externally does not change the DAC output span which is determined by the internal reference and remains at 5 V nominal.
25	V_{OUTC}	Analog Output Voltage for DAC C. Eight-bit buffered output with an output range of $V_{OUTC} = V_{BIAS} \pm V_{SWING}$; 1 LSB = 2 $V_{SWING}/256$ = 5 V/256 = 19.5 mV nominal.
26	V_{BIAS}	Input Bias Voltage. The voltage applied to this input (with respect to AGND) sets the midpoint of the transfer function for all input and output channels. The bias voltage range is +3 V to +6.8 V.
27	V_{OUTB}	Analog Output Voltage for DAC B. Eight-bit buffered output with an output range of $V_{OUTB} = V_{BIAS} \pm V_{SWING}$; 1 LSB = 2 $V_{SWING}/256$ = 5 V/256 = 19.5 mV nominal.
28	V_{OUTA}	Analog Output Voltage for DAC A. Eleven-bit buffered output with an output range of $V_{OUTA} = V_{BIAS} \pm V_{SWING}$; 1 LSB = 2 $V_{SWING}/2048$ = 5 V/2048 = 2.44 mV nominal.

TERMINOLOGY

Relative Accuracy
For the AD7774 ADC, Relative Accuracy or endpoint nonlinearity is the maximum deviation, in LSBs, of the ADC's actual code transition points from a straight line drawn between the endpoints of the ADC transfer function.

For the DACs, Relative Accuracy or endpoint nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity
Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max ensures monotonicity (DAC) or no missed codes (ADC).

Bias Offset Error
For an ideal 8-bit ADC, the output code for an input voltage equal to V_{BIAS} should be 00 Hex. The ADC Bias Offset Error is the difference between the actual midpoint voltage for code 00 Hex and the input bias voltage, expressed in LSBs.

For an ideal DAC, the output voltage for code 000 Hex (DAC A) or code 00 Hex (DAC B, DAC C) should be equal to V_{BIAS}. The DAC Bias Offset Error is the difference between the actual output voltage and V_{BIAS}, expressed in LSBs.

Relative Offset Error
Relative Offset Error is the difference between the result of an internal bias conversion and the result of a conversion carried out with each of the analog inputs connected to V_{BIAS}.

Full-Scale Error (DAC)
The DACs in the AD7774 can be considered as having a bipolar (positive and negative) output range, but referred to the input bias voltage instead of AGND. Positive Full-Scale Error for the DACs is the difference, expressed in LSBs, between the actual output voltage for input code 3FF Hex (for DAC A) or 7F Hex (DAC B, DAC C) and the ideal voltage (V_{BIAS} + V_{SWING} − 1 LSB). Negative Full-Scale Error for the DAC is similarly specified for code 400 (DAC A) or code 80 (DAC B, DAC C), relative to the ideal output voltage (V_{SWING} − V_{BIAS}). Note that the full-scale errors for the DACs are measured after the bias offset errors have been adjusted out.

Full-Scale Error (ADC)
The input channels of the ADC can also be considered as having bipolar (positive and negative) input ranges, but referred to the input bias voltage instead of AGND. Positive Full-Scale Error for the ADC is the difference between the actual input voltage at the 7E to 7F code transition and the ideal input voltage (V_{BIAS} + V_{SWING} −1.5 LSB), expressed in LSBs. Negative Full-Scale Error is similarly specified for the 81 to 80 code transition, relative to the ideal input voltage for this transition (V_{BIAS} − V_{SWING} +0.5 LSB). Note that the full-scale errors for the ADC input channels are measured after their respective Bias Offset errors have been adjusted out.

Digital-to-Analog Glitch Impulse
Digital-to-Analog Glitch Impulse is the impulse injected into the analog output when the digital inputs change state with the DAC selected. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed from all 1s to all 0s.

Digital Feedthrough
Digital Feedthrough is also a measure of the impulse injected into the analog outputs from the digital inputs but is measured when the DAC is not selected. It is essentially feedthrough across the die and package. It is important in the AD7774 since it is a measure of the glitch impulse transferred to the analog output when data is read from the ADC latches. It is specified in nV secs and is measured with $\overline{WR}$ high and a digital code change from all 0s to all 1s.

TIMING AND CONTROL

The AD7774 contains two ADC data latches, an ADC control register and three DAC registers. Each of the ADC data latches contains a conversion result from the held voltage on its respective track/hold, i.e., ADC Latch A contains the result of a conversion performed on the held voltage on Track/Hold A, while ADC Latch B contains the results of a conversion done on the held voltage on Track/Hold B. The ADC control register determines whether a single or double conversion takes place and also determines the conversion sequence . In addition, it controls the analog input range for each channel.

Reading from the AD7774 accesses the contents of the ADC data latches. The $\overline{RD}$ input is a level-triggered input. Writing to the device either initiates conversion on the channel(s) determined by the ADC control register or loads data to the DAC registers. The $\overline{WR}$ input is an edge-triggered input. The following sections describe read, write and control register operations for the AD7774.

Read Operation

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	AD2	AD1	AD0	Function
1	X	X	X	X	X	No Read Operation.
X	1	X	X	X	X	No Read Operation.
0	0	X	X	X	0	The contents of ADC Latch A are output to the databus. This will contain the results of a conversion on either V_{A1} or V_{A2} (see ADC Control Register section).
0	0	X	X	X	1	The contents of ADC Latch B are output to the databus. This will contain the results of a conversion on either V_{B1} or V_{B2} (see ADC Control Register section).

Write Operation

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	AD2	AD1	AD0	Function
1	X	X	X	X	X	No Write Operation.
X	X	1	X	X	X	No Write Operation.
0	1	↓	0	0	0	DB0–DB7 are written to the upper 8 bits of the DAC A Register.
0	1	↓	0	0	1	DB5–DB7 are written to the lower 3 bits of the DAC A Register, and all 11 bits of the DAC A register are loaded to DAC A.
0	1	↓	0	1	0	DB0–DB7 are written into the DAC B Register and are loaded to DAC B.
0	1	↓	0	1	1	DB0–DB7 are written into the DAC C Register and are loaded to DAC C.
0	1	↓	1	0	0	Start conversion on either V_{A1} or V_{B1} or both (DB4 and DB5 of the ADC Control Register determine operation – see ADC Control Register section).
0	1	↓	1	0	1	Start conversion on either V_{A2} or V_{B2} or both (DB4 and DB5 of the ADC Control Register determine operation – see ADC Control Register section).
0	1	↓	1	1	0	Start conversion on either Track/Hold A bias voltage or Track/Hold B bias voltage or both (DB4 and DB5 of the ADC Control Register determine operation—see ADC Control Register section). See Bias Conversions section for explanation.
0	1	↓	1	1	1	DB0–DB5 is written to the ADC Control Register.

X = Don't Care.
A read during an ADC conversion may corrupt the data from the conversion in progress.

ADC Control Register

The ADC Control Register determines whether a single or double conversion takes place and also which track/hold output is converted when a write operation to start conversion takes place. The single/double conversion is determined by DB4 (see below). A double conversion means that both track/holds go into hold mode simultaneously, and the ADC converts both held voltages in sequence. The ADC status line, $\overline{BUSY}$, does not indicate that the conversion sequence has ended until both conversions are complete. In the single conversion mode, both track/holds again are simultaneously held but only one of these "held" voltages is converted—the other is ignored. The ADC status line, $\overline{BUSY}$, indicates that the conversion sequence has ended after one track/hold voltage has been converted. DB5 determines which track/hold voltage is converted in the single conversion mode. The ADC Control Register also determines the analog input voltage range for all four inputs (see DB0–DB3 below).

ADC Control Register Bit	Function
DB0	V_{A1} Input Voltage Range
0	Input Range is $V_{BIAS} \pm V_{SWING}$
1	Input Range is $V_{BIAS} \pm V_{SWING}/2$
DB1	V_{A2} Input Voltage Range
0	Input Range is $V_{BIAS} \pm V_{SWING}$
1	Input Range is $V_{BIAS} \pm V_{SWING}/2$
DB2	V_{B1} Input Voltage Range
0	Input Range is $V_{BIAS} \pm V_{SWING}$
1	Input Range is $V_{BIAS} \pm V_{SWING}/2$
DB3	V_{B2} Input Voltage Range
0	Input Range is $V_{BIAS} \pm V_{SWING}$
1	Input Range is $V_{BIAS} \pm V_{SWING}/2$
DB4	Single/Double Conversion
0	Double Conversion
1	Single Conversion
DB5	Conversion Sequence
0	First Conversion in the sequence is a V_A conversion[1, 2]
1	First Conversion in the sequence is a V_B conversion[1, 2]

NOTES

[1]A V_A conversion is a conversion on either V_{A1}, V_{A2}, or the bias voltage for Track/Hold A. Address inputs AD0, AD1 and AD2 determine which one of these signals is converted. A V_B conversion is a conversion on either V_{B1}, V_{B2}, or the bias voltage for Track/Hold B. Address inputs AD0, AD1 and AD2 determine which one of these signals is converted. (See previous page.)

[2]In the single conversion mode DB5 determines whether a V_A conversion or a V_B conversion takes place. In the double conversion mode, DB5 simply determines the order in which the two track/hold voltages are converted.

ADC Read Cycle

Figure 2 shows the timing diagram for a read operation for the AD7774. It consists of bringing both $\overline{CS}$ and $\overline{RD}$ low with data being accessed from one of the two on-chip ADC latches. Address line AD0 determines from which latch the data is accessed. With AD0 low, the contents of ADC Latch A are placed on the databus during a read operation; with AD0 high, a read operation will access the contents of ADC Latch B. ADC Latch A will contain the results of a conversion on either V_{A1} or V_{A2} or the results of a conversion on the bias voltage for Track/Hold A. ADC Latch B will contain the results of a conversion on V_{B1} or V_{B2} or the results of a conversion on the bias voltage for Track/Hold B.

Both the $\overline{CS}$ and $\overline{RD}$ inputs are level-triggered. If both are hardwired low, the data access time for a read cycle is determined from AD0.

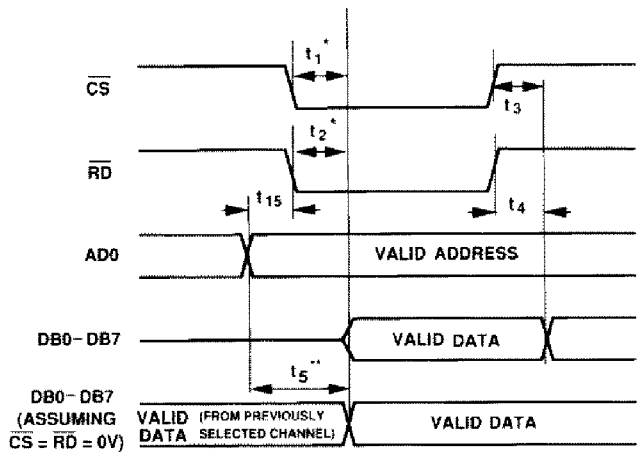


Figure 2. AD7774 Read Cycle

DAC/Control Register Write Cycle

A write operation to the AD7774 consists of writing data to the DAC registers or to the ADC Control Register. A write to the AD7774 can also initiate conversion on the ADC (see ADC Conversion Sequence section). The function of the write operation is determined by address bits AD0–AD2.

The $\overline{WR}$ input is an edge-triggered input, and data is only written to the on-chip registers on the rising edge of $\overline{WR}$. Data written to the DAC registers must be left justified to load correct data. For the 11-bit DAC A, this means that the upper 8 bits are loaded with the 11-bit MSB occupying the DB7 position on the databus. The lower three bits of the 11-bit word are loaded in a separate write cycle with DB0 of the 11-bit word occupying the DB5 position on the databus. Figure 3 shows the timing diagram for a write operation to the AD7774.

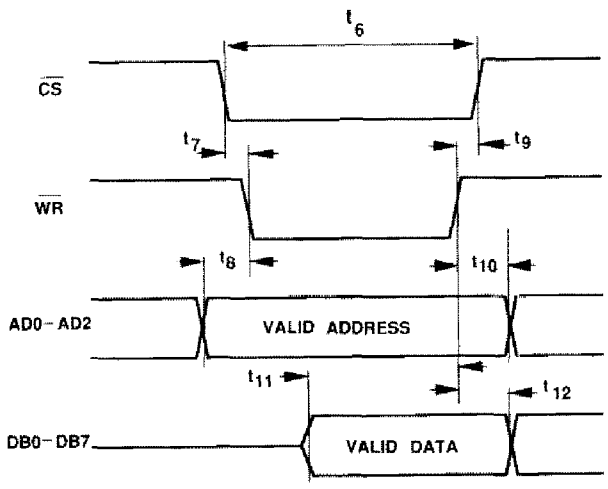


Figure 3. AD7774 Write Cycle

ADC Conversion Sequence

The AD7774 contains two track/hold amplifiers and one A/D converter. A conversion sequence can either consist of a single conversion or double conversion. In the double conversion mode, the track/holds go into hold mode simultaneously, and the held voltages are converted sequentially by the A/D converter. In the single conversion option, the track/holds again go into hold mode simultaneously, but only one voltage is converted—either the held voltage on Track/Hold A or Track/Hold B.

Figure 4 shows the timing diagram for the AD7774 conversion sequence. Conversion is initiated on the rising edge of $\overline{WR}$. Address lines AD0–AD2 determine which channel is to be converted. On the rising edge of $\overline{WR}$, the internal clock oscillator is activated, and the channel acquisition time begins. The $\overline{BUSY}$ output goes low to indicate that the conversion sequence has begun. The channel acquisition time takes approximately 1.5 μs, at which time the track/holds go into hold mode. The A/D converter then converts the held voltage on either Track/Hold A or Track/Hold B depending on the status of DB5 of the control register.

This first conversion takes a total of 3.6 μs maximum. In the single conversion mode, the conversion sequence is now complete, and the AD7774 indicates this by taking its $\overline{BUSY}$ status line high. In the double conversion mode, the conversion on the voltage held on the second track/hold starts at this time and runs for another 2.4 μs maximum. In this double conversion mode, the $\overline{BUSY}$ line does not return high until the second conversion is complete. At the end of conversion, either single or double, the internal clock oscillator is shut down.

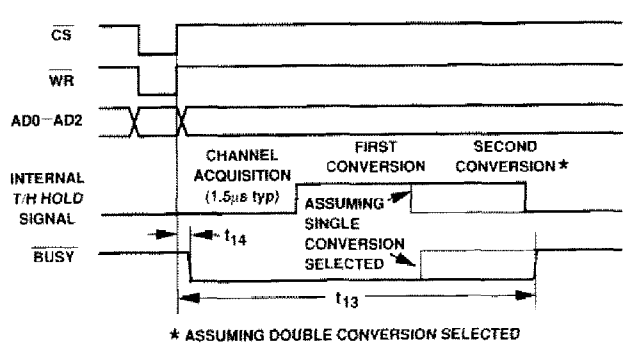


Figure 4. AD7774 Conversion Cycle

CIRCUIT DESCRIPTION

Analog Inputs and Outputs

The AD7774 provides the analog-to-digital and digital-to-analog conversion functions required between the microcontroller and the servo power amplifier in digital servo systems. It is intended primarily for closed-loop head positioning in dedicated-only and combined dedicated/embedded disk drives or other closed-loop digital servo applications. The ability to refer input and output signals to some voltage other than ground is of particular importance in disk drive applications. Typically, only +5 V digital and +12 V analog supply voltages are available, and the analog signals are often referred to a voltage around half the analog supply.

The AD7774 contains two track/hold amplifiers which feed a high speed, 8-bit, sampling ADC, each track/hold having two input channels. The part also contains three DACs with output amplifiers—one 11-bit DAC and two 8-bit DACs. A unique feature of the AD7774 is the input and output signal conditioning circuitry, which allows the analog input and output voltages to be referred to a point other than analog ground. The offset of the input channels and output channels is achieved by applying a ground-referenced, positive control voltage to the V_{BIAS} input of the AD7774. The voltage span of the input channels is set by applying a ground-referenced, positive control voltage to the V_{SWING} input of the part. The output voltage span from the DACs is set by the internal reference voltage.

Figure 5 shows the input voltage to output code relationship for the four input channels. The midpoint code of the input channels, 00 Hex (0000 0000 Binary), occurs at an input voltage equal to V_{BIAS}. Output coding from the ADC is 2s complement biased around this V_{BIAS} voltage.

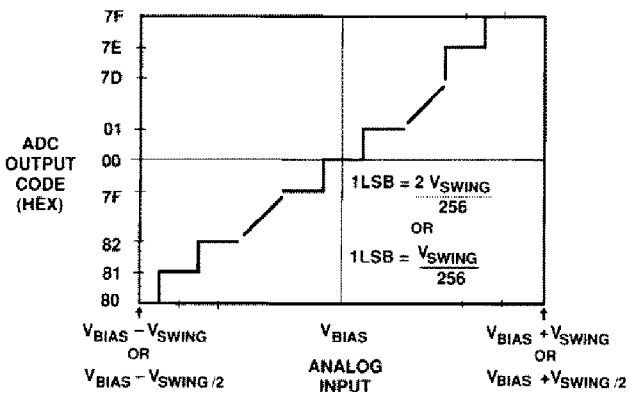


Figure 5. ADC Transfer Function

The input voltage range for the channels depends upon the status of bits DB0 to DB3 of the ADC control register. Each these bits controls the gain on one of the input channels (see ADC Control Register section). The input gain on each one of the input channels can either be a gain of 1 or a gain of 1/2. This results in an input voltage range which can be either $V_{BIAS} \pm V_{SWING}$ or $V_{BIAS} \pm V_{SWING}/2$.

For the first case, the full scale range (FSR) is 2 V_{SWING} and 1 LSB = 2 V_{SWING}/256. With the nominal V_{SWING} of +2.5 V, 1 LSB = 5 V/256 = 19.5 mV. The ideal first code transition (80 to 81 Hex) occurs at an analog input voltage equal to $V_{BIAS} - V_{SWING}$ + 0.5 LSB (negative full scale) and the ideal last code transition (7E to 7F Hex) occurs at an input voltage equal to $V_{BIAS} + V_{SWING}$ −1.5 LSBs (positive full scale).

For the second case, the full scale range (FSR) is V_{SWING} and 1 LSB = V_{SWING}/256. With the nominal V_{SWING} of +2.5 V, 1 LSB = 2.5 V/256 = 9.76 mV. The ideal first code transition (80 to 81 Hex) occurs at an analog input voltage equal to $V_{BIAS} - V_{SWING}/2$ + 0.5 LSB (negative full scale) and the ideal last code transition (7E to 7F Hex) occurs at an input voltage equal to $V_{BIAS} + V_{SWING}/2$ − 1.5 LSBs (positive full scale).

The input code to output voltage relationship for DAC A is shown in Figure 6. The DAC output voltage for an input code of 000 Hex is ideally equal to V_{BIAS}. Input coding to the DAC is 2s complement with the output voltage range biased around this V_{BIAS} voltage. The output voltage range is $V_{BIAS} \pm V_{SWING}$.

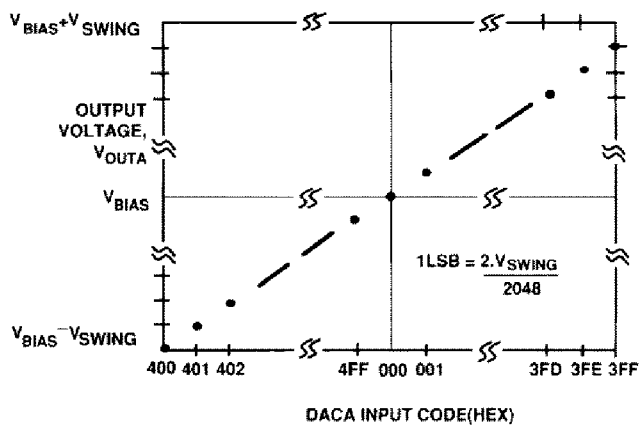


Figure 6. Transfer Function

The output range is 2 V_{SWING} where V_{SWING} is set by the internal reference voltage. The nominal DAC output swing is, therefore, 5 V and 1 LSB = 5 V/2048 = 2.44 mV. The bottom end of the transfer function occurs at an input code of 400 Hex and is ideally equal to $V_{BIAS} - V_{SWING}$. The top end of the transfer function occurs at an input code of 3FF Hex and is ideally equal to $V_{BIAS} + V_{SWING}$ −1 LSB.

The transfer function for both DAC B and DAC C is very similar to that outlined for DAC A. Once again, the output voltage range is $V_{BIAS} \pm V_{SWING}$. The V_{SWING} voltage is again set by the internal reference voltage. Therefore, the nominal output swing is 5 V and 1 LSB = 5 V/256 = 19.5 mV.

The DAC output voltage for an input code of 00 Hex is ideally equal to V_{BIAS}. Input coding to the DACs is 2s complement with the output voltage range biased around this V_{BIAS} voltage. The bottom end of the transfer function (negative full scale) occurs at an input code of 80 Hex and is ideally equal to $V_{BIAS} - V_{SWING}$. The top end of the transfer function (positive full scale) occurs at an input code of 7F Hex and is ideally equal to $V_{BIAS} + V_{SWING} - 1$ LSB. The input code to output voltage relationship for both DAC B and DAC C is shown in Figure 7.

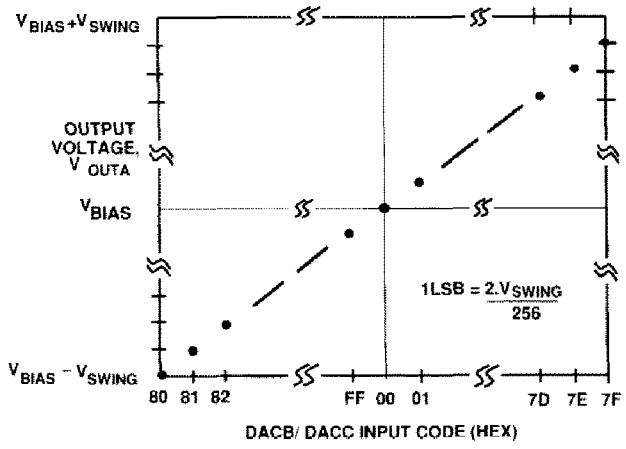


Figure 7. DAC B/DAC C Transfer Function

Bias Voltage Conversions

The voltage applied to the V_{BIAS} pin of the AD7774 is applied internally to both track/holds. Each track/hold introduces some bias offset error on this input V_{BIAS} voltage, and these errors may differ slightly from each other (typically less than 2 LSBs). The AD7774 provides the option to convert the bias voltage to estimate the bias offset error. Since both track/holds introduce different errors, the AD7774 allows the user to perform a conversion on the bias voltage at each track/hold. If this is done during a calibration routine, the bias offset error in each channel can be stored and compensated for in software. After a bias offset conversion for Track/Hold A, the results are stored in ADC Latch A and for a bias offset conversion for Track/Hold B, the results are stored in ADC Latch B.

Driving the Analog Inputs and Reference Inputs

The analog inputs, V_{A1}, V_{A2}, V_{B1} and V_{B2} require up to 1 mA of input current and as such must be driven from low output impedance sources. In addition, the V_{BIAS} and V_{SWING} inputs must also be driven from low impedance sources. The V_{SWING} pin provides the internally generated swing voltage, but this can be overdriven by an externally applied voltage. This externally applied voltage will generate the V_{SWING} voltage for the ADC but the V_{SWING} for the DACs is always generated from the internal swing voltage.

MICROPROCESSOR/MICROCOMPUTER INTERFACING

The AD7774 is designed for easy interfacing to microprocessors and microcomputers as a memory mapped peripheral or an I/O device. In addition, the AD7774 high speed bus timing allows direct interfacing to most microprocessors including the DSP processors.

AD7774–ADSP-2101/ADSP-2105 Interface

Figure 8 shows a typical interface to the DSP microcomputer, the ADSP-2101/ADSP-2105. The ADSP-2101/ADSP-2105 is optimized for high speed numeric processing tasks.

Because the instruction cycle of the ADSP-2101/ADSP-2105 is very fast, the $\overline{WR}$ and $\overline{RD}$ pulses must be stretched out to suit the AD7774. This is easily achieved as the ADSP-2101/ADSP-2105 memory interface supports slower memories and memory-mapped peripherals with a programmable wait state generation capability. A number of wait states, from 0 to 7, can be specified for each memory interface. One wait state is sufficient for the interface to the AD7774.

Conversion is initiated on the required ADC channel using a <DM(CST) = MR0> where CST is the relevant channel address. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of a <DM(DAC) = MR0> instruction where DAC is the relevant DAC address or the address of the ADC control register. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction <MR0 = DM(ADC)> where ADC is the address of the relevant ADC Latch.

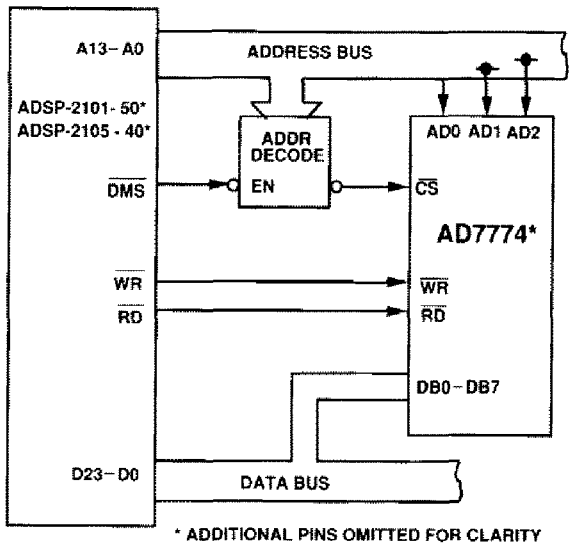


Figure 8. AD7774 to ADSP-2101/ADSP-2105 Interface

AD7774–TMS320C10/TMS320C14 Interface

A typical interface to the TMS320C10/TMS320C14 is shown in Figure 9. The AD7774 is mapped at a port address, and the interface is designed for the maximum TMS320C10 clock frequency of 20 MHz and the maximum clock frequency of 25 MHz for the TMS320C14.

Conversion is initiated on the selected AD7774 ADC channel using a single I/O instruction, <OUT CST,A> where CST is the relevant address for the selected channel. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of an <OUT DAC,A> instruction where DAC is the relevant DAC address or the address of the ADC control regis-

ter. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction <IN A,ADC> where ADC is the address of the relevant ADC Latch.

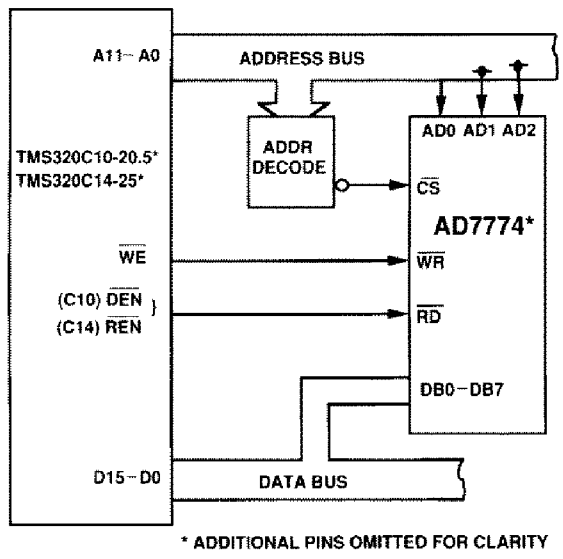


Figure 9. AD7774 to TMS320C10/TMS320C14 Interface

AD7774–TMS320C25 Interface

Figure 10 shows an interface between the TMS320C25 and the AD7774. The TMS320C25 does not have separate $\overline{RD}$ and $\overline{WR}$ signals to drive the AD7774 $\overline{RD}$ and $\overline{WR}$ inputs directly. These have to be generated from the processor $\overline{STRB}$ and R/$\overline{W}$ outputs with the addition of some logic gates.

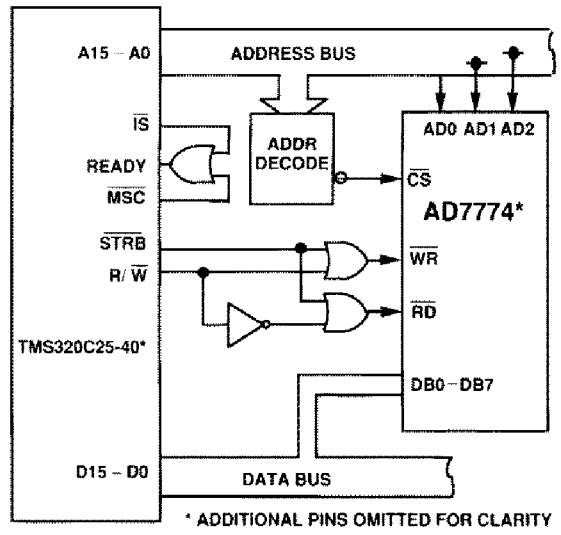


Figure 10. AD7774 to TMS320C25 Interface

Once again, because the processor cycle time is so fast a wait state has to be inserted during read and write cycles to the AD7774. This is achieved by OR-gating the $\overline{IS}$ signal with the $\overline{MSC}$ signal to drive the READY input and, thereby, generate one wait state during every read and write operation to the AD7774.

Conversion is initiated on the selected AD7774 ADC channel using a single I/O instruction, <OUT CST,A> where CST is the relevant address for the selected channel. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of an <OUT DAC,A> instruction where DAC is the relevant DAC address or the address of the ADC control register. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction < IN A,ADC > where ADC is the address of the relevant ADC Latch.

AD7774–80C196 Interface

Figure 11 shows a typical interface between the AD7774 and the 80C196 microcomputer. The microcomputer is configured in its 8-bit bus cycle mode and in the address valid strobe mode. In this mode, the high order 8 bits of the address bus appear on Port 4, while Port 3 contains the multiplexed data bus and lower order address bus.

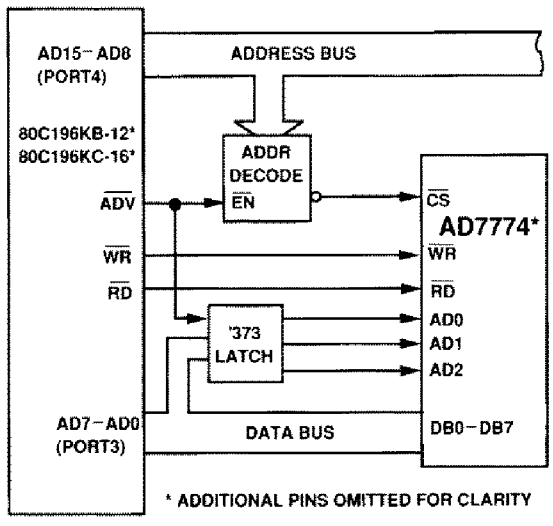


Figure 11. AD7774 to 80C196 Interface

Conversion is initiated on the selected AD7774 ADC channel using a single I/O instruction, <STB CST,D> where CST is the relevant address for the selected channel and D is a location in the 80C196 register file or is immediate data. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of an <STB DAC,D> instruction where DAC is the relevant DAC address or the address of the ADC control register and D is a location in the 80C196 register file or is immediate data. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction <LDB D,ADC> where ADC is the address of the relevant ADC latch and D is a location in the 80C196 register file.

AD7774–80C51 Interface

A typical interface between the AD7774 and the 80C51 is shown in Figure 12. In this interface, Port 0 provides the multiplexed low order address and data bus, and Port 2 provides the high order address bus. The ALE signal from the 80C51 is used to demultiplex the address/data bus.

Conversion is initiated on the selected AD7774 ADC channel using a single instruction, <MOV CST,A> where CST is the relevant address for the selected channel and A is the 80C51 accumulator. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of an <MOV DAC,A> instruction where DAC is the relevant DAC address or the address of the ADC control register, and A is the 80C51 accumulator. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction <MOV A,ADC> where ADC is the address of the relevant ADC Latch and A is the 80C51 accumulator.

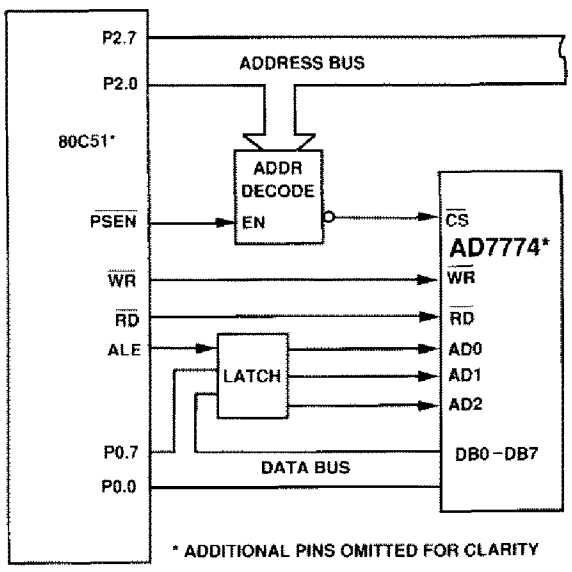


Figure 12. AD7774 to 80C51 Interface

AD7774–68HC11 Interface

Figure 13 shows an interface between the AD7774 and the 68HC11. In this interface, Port C provides the multiplexed low order address and data bus, and Port B provides the high order address bus. The AS signal from the 68HC11 is used to demultiplex the address/data bus. The 68HC11 does not have separate $\overline{RD}$ and $\overline{WR}$ signals to drive the AD7774 $\overline{RD}$ and $\overline{WR}$ inputs directly. These have to be generated from the processor E and R/$\overline{W}$ outputs with the addition of some logic gates.

Conversion is initiated on the selected AD7774 ADC channel using a single instruction, <STAA CST> where CST is the relevant address for the selected channel. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of an <STAA DAC> instruction where DAC is the relevant DAC address or the address of the ADC control register, and the data is loaded to the relevant register from the 68HC11 accumulator. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction <LDAA ADC> where ADC is the address of the relevant ADC latch, and the conversion result is loaded to the 68HC11 accumulator.

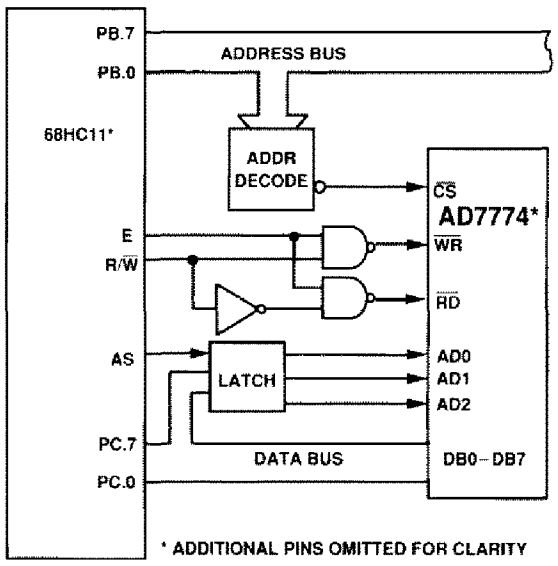


Figure 13. AD7774 to 68HC11 Interface

APPLICATIONS

The AD7774 servo I/O port is used to convert servo-related signals between the analog and digital domains. The input structure of the ADC makes it very easy to convert the typical output signals provided by a servo demodulator.

In a magnetic disk drive employing a dedicated servo surface or a combined embedded/dedicated servo surface, the servo demodulator produces two, positive-only, quadrature signals, generally sinusoidal or triangular, from the di-bit patterns read from the servo surface. The quadrature signals have the form of $V_{BIAS} \pm V_{SWING}$. The simultaneous sampling of the AD7774 input channels allows conversion of these quadrature signals without introducing significant phase delay errors. These converted signals provide the servo microcontroller with position and track crossing information from which velocity information can be derived. In optical disk drives, analogous servo signals can be derived from the quad photodiode detector to provide position and focus information for the microcontroller.

In dedicated servo drives and combined embedded/dedicated servo drives, the servo demodulator converts the servo information bit patterns from the disk into the standard N and Q (normal and quadrature) servo signals. The relative phase relationship between these signals is important so the simultaneous sampling feature of the AD7774 is used to maintain the relative phase between the N and Q signals. The four channels of the AD7774 can be used to process information from two demodulators. Alternatively, two channels can be used for the N and Q signals with the other ADC channels used for current measurement, temperature measurement, calibration routines or other housekeeping functions.

In magnetic disk drives, a single voice coil motor is used to position the head assembly and one DAC is usually sufficient to drive the motor in both the seek and track modes. In the seek mode the DAC can be used to generate directly the desired analog velocity trajectory which the head must travel in order to achieve minimum access times. Alternatively the DAC can generate a servo error value (computed by the microcontroller) between the actual head velocity and the desired head velocity. In

the track mode, the DAC can be used to provide a position error signal to keep the head over the track or to detect the head off-track, for such purposes as thermal compensation and soft-error retries. The DACs provide positive-only output signals of the form $V_{BIAS} \pm V_{SWING}$, which are ideal for driving voice coil motors. In general, up to 11 bits of resolution are required for a DAC to control the motor in both the seek and track modes. As a result, DAC A would generally be used to drive the voice coil motor. The other DAC channels can be used for programmable control of the loop filter or for AGC or programmable gain control.

A typical servo control loop using the AD7774 is shown in Figure 14. In this dedicated servo example, the servo demodulator outputs (the N and Q signals) are applied to the V_{A1} and V_{B1} inputs of the AD7774. The voice coil motor current, I_L, is bidirectional and is supplied by the power transconductance amplifier. One input to this amplifier is held at V_{BIAS} while the other input is driven from the DAC A output, V_{OUTA}. Typical input voltages for this power stage are shown in Figure 15. The transconductance, G_O, of the power stage is determined by external sense resistors.

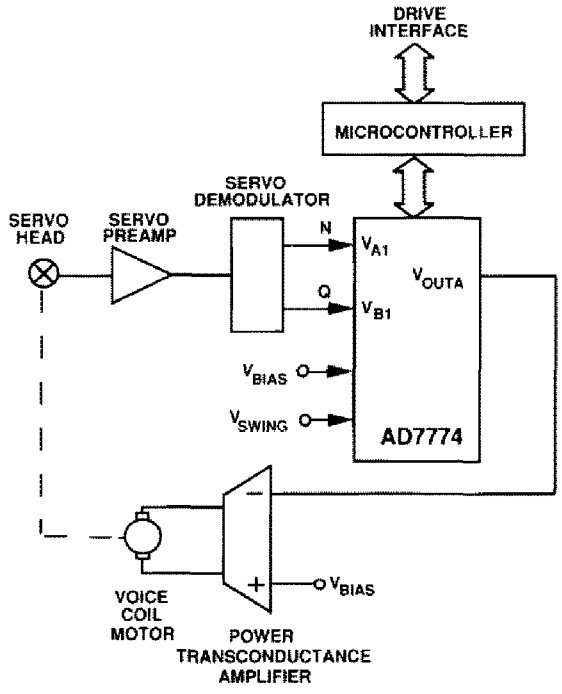


Figure 14. Typical Dedicated Servo Control Loop Using the AD7774

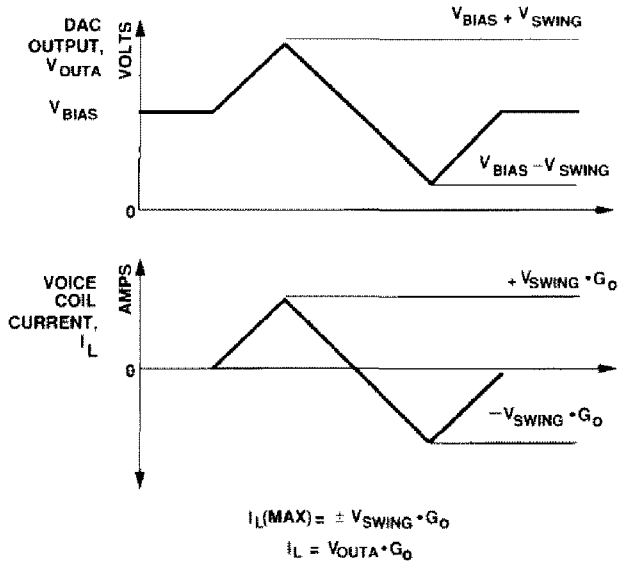


Figure 15. Typical Relationship Between Input Voltage and Output Current for Transconductance Amplifier

Multichannel Expansion

The AD7774 with its four input channels has the capability of monitoring the N and Q signals from two servo demodulators. With the addition of a multiplexer and a dual op amp, the system can be expanded so that the AD7774 handles the outputs from a number of servo demodulators. Using a differential multiplexer as shown in Figure 16, the N and Q signals for each servo demodulator can still be simultaneously sampled. The ADG527A multiplexer is ideally suited since it is specified for single supply operation (12 V ± 10%).

The $\overline{CS}$ and $\overline{WR}$ inputs to the AD7774 are gated to provide the $\overline{WR}$ input to the ADG527A. The multiplexer input is selected on the falling edge of $\overline{WR}$ while the signal is latched on the rising edge. The AD7774 starts conversion also on the rising edge of $\overline{WR}$. Therefore, the output signal of the multiplexer must have settled to within 8 bits over the duration of the $\overline{WR}$ pulse. The t_{ON} ($\overline{WR}$) and settling time of the ADG527A determine the width of the $\overline{WR}$ pulse.

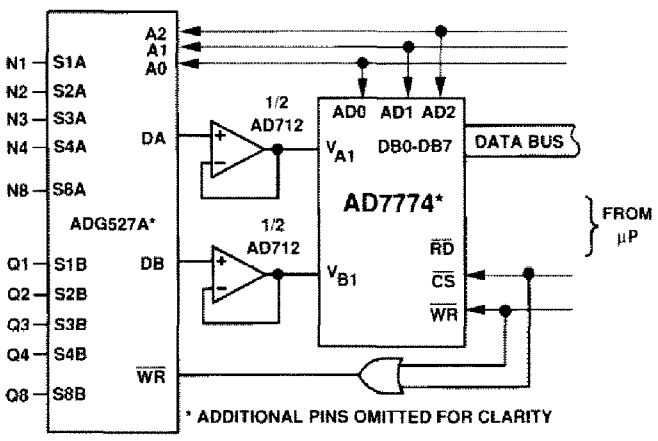


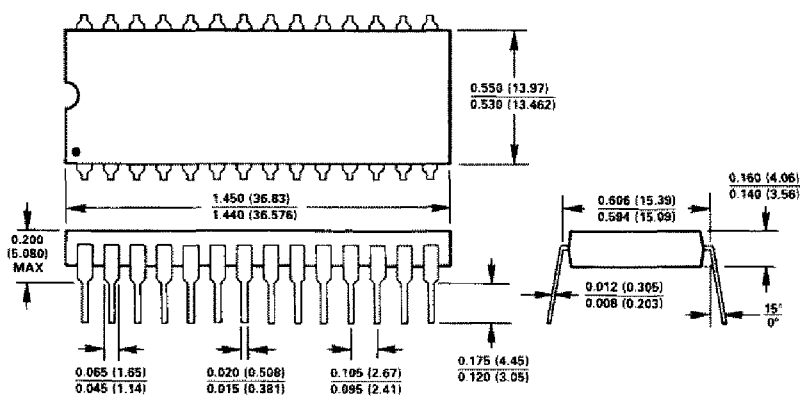
Figure 16. Multichannel System

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

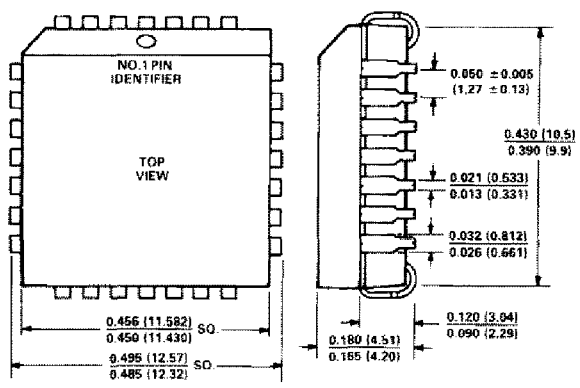
Dimensions shown in inches and (mm).

28-Pin Plastic DIP (N-28)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
LEADS ARE SOLDER DIPPED OR TIN-PLATED ALLOY 42 OR COPPER

28-Pin PLCC (P-28A)



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