ANALOG DEVICES

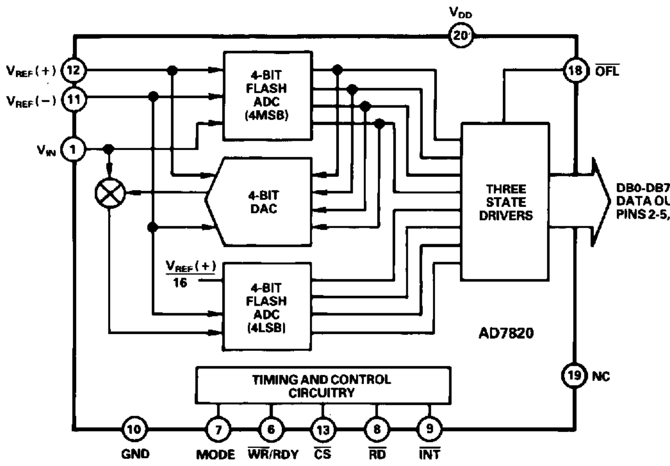
LC²MOS High Speed μP-Compatible 8-Bit ADC with Track/Hold Function

AD7820

FEATURES

Fast Conversion Time: 1.36μs max
Built-In Track-and-Hold Function
No Missed Codes
No User Trims Required
Single +5V Supply
Ratiometric Operation
No External Clock
Extended Temperature Range Operation
Skinny 20-Pin DIP, SOIC and 20-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7820 is a high speed, microprocessor-compatible 8-bit analog-to-digital converter which uses a half-flash conversion technique to achieve a conversion time of 1.36μs. The converter has a 0V to +5V analog input voltage range with a single +5V supply.

The half-flash technique consists of 31 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC. The input to the AD7820 is tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold for signals with slew rates less than 100mV/μs.

The part is designed for ease of microprocessor interface with the AD7820 appearing as a memory location or I/O port without the need for external interfacing logic. All digital outputs use latched, three-state output buffer circuitry to allow direct connection to a microprocessor data bus or system input port. A non-three state overflow output is also provided to allow cascading of devices to give higher resolution.

The AD7820 is fabricated in an advanced, all ion-implanted, high speed, Linear Compatible CMOS (LC²MOS) process and features a low maximum power dissipation of 75mW. It is available in 20-pin DIPs, SOICs and in 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The half-flash conversion technique, coupled with fabrication on Analog Devices' LC²MOS process, enables very fast conversion times. The maximum conversion time for the WR-RD mode is 1.36μs, with 1.6μs the maximum for the RD mode.
2. Total Unadjusted Error
   The AD7820 features an excellent total unadjusted error figure of less than 1/2LSB over the full operating temperature range. The part is also guaranteed to have no missing codes over the entire temperature range.
3. Built-In Track-and-Hold
   The analog input circuitry uses sampled-data comparators, which by nature have a built-in track-and-hold function. As a result, input signals with slew rates up to 100mV/μs can be converted to 8-bits without external sample-and-hold. This corresponds to a 5V peak-to-peak, 7kHz sine-wave signal.
4. Single Supply
   Operation from a single +5V supply with a positive voltage reference allows operation of the AD7820 in microprocessor systems without any additional power supplies.

REV. A

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AD7820—SPECIFICATIONS

($V_{DD} = +5V$; $V_{REF}(+) = +5V$; $V_{REF}(-) = GND = 0V$ unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise specified. Specifications apply for RD Mode (Pin 7 = 0V)

Parameter	K Version[1]	L Version	B, T Versions	C, U Versions	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[2]	±1	±1/2	±1	±1/2	LSB max	
Minimum Resolution for which No Missing Codes are guaranteed	8	8	8	8	Bits	
REFERENCE INPUT						
Input Resistance	1.0/4.0	1.0/4.0	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
$V_{REF}(+)$ Input Voltage Range	$V_{REF}(-)/V_{DD}$	$V_{REF}(-)/V_{DD}$	$V_{REF}(-)/V_{DD}$	$V_{REF}(-)/V_{DD}$	V min/V max	
$V_{REF}(-)$ Input Voltage Range	GND/$V_{REF}(+)$	GND/$V_{REF}(+)$	GND/$V_{REF}(+)$	GND/$V_{REF}(+)$	V min/V max	
ANALOG INPUT						
Input Voltage Range	$V_{REF}(-)/V_{REF}(+)$	$V_{REF}(-)/V_{REF}(+)$	$V_{REF}(-)/V_{REF}(+)$	$V_{REF}(-)/V_{REF}(+)$	V min/V max	
Input Leakage Current	±3	±3	±3	±3	μA max	
Input Capacitance[3]	45	45	45	45	pF typ	
LOGIC INPUTS						
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$						
V_{INH}	2.4	2.4	2.4	2.4	V min	
V_{INL}	0.8	0.8	0.8	0.8	V max	
I_{INH} ($\overline{CS}$, $\overline{RD}$)	1	1	1	1	μA max	
I_{INH} ($\overline{WR}$)	3	3	3	3	μA max	
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
MODE						
V_{INH}	3.5	3.5	3.5	3.5	V min	
V_{INL}	1.5	1.5	1.5	1.5	V max	
I_{INH}	200	200	200	200	μA max	50 μA typ
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
LOGIC OUTPUTS						
DB0-DB7, $\overline{OFL}$, $\overline{INT}$						
V_{OH}	4.0	4.0	4.0	4.0	V min	$I_{SOURCE} = 360\mu A$
V_{OL}	0.4	0.4	0.4	0.4	V max	$I_{SINK} = 1.6mA$
I_{OUT} (DB0–DB7)	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5pF
RDY						
V_{OL}	0.4	0.4	0.4	0.4	V max	$I_{SINK} = 2.6mA$
I_{OUT}	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5pF
SLEW RATE, TRACKING[3]	0.2	0.2	0.2	0.2	V/μs typ	
	0.1	0.1	0.1	0.1	V/μs max	
POWER SUPPLY						
V_{DD}	5	5	5	5	Volts	±5% for Specified Performance
I_{DD}[4]	15	15	20	20	mA max	$\overline{CS} = \overline{RD} = 0V$
Power Dissipation	40	40	40	40	mW typ	
Power Supply Sensitivity	±1/4	±1/4	±1/4	±1/4	LSB max	±1/16LSB typ $V_{DD} = 5V \pm 5\%$

NOTES

[1] Temperature Ranges are as follows:
- K, L Versions: −40°C to +85°C
- B, C Versions: −40°C to +85°C
- T, U Versions: −55°C to +125°C

[2] Total Unadjusted Error includes offset, full-scale and linearity errors.

[3] Sample tested at 25°C by Product Assurance to ensure compliance.

[4] See Typical Performance Characteristics.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V; $V_{REF}(+)$ = +5V; $V_{REF}(-)$ = GND = 0V unless otherwise stated.)

Parameter	Limit at 25°C (All Versions)	Limit at T_{min}, T_{max} (K, L, B, C Versions)	Limit at T_{min}, T_{max} (T, U Versions)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ TO $\overline{RD}/\overline{WR}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ TO $\overline{RD}/\overline{WR}$ Hold Time
t_{RDY}[2]	70	90	100	ns max	$\overline{CS}$ to Delay. Pull-Up Resistor 5kΩ.
t_{CRD}	1.6	2.0	2.5	μs max	Conversion Time (RD Mode)
t_{ACC0}[3]	t_{CRD} + 20	t_{CRD} + 35	t_{CRD} + 50	ns max	Data Access Time (RD Mode)
t_{INTH}[2]	125	–	–	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)
	175	225	225	ns max	
t_{DH}[4]	60	80	100	ns max	Data Hold Time
t_P	500	600	600	ns min	Delay Time between Conversions
t_{WR}	600	600	600	ns min	Write Pulse Width
	50	50	50	μs max	
t_{RD}	600	700	700	ns min	Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses
t_{ACC1}[3]	160	225	250	ns max	Data Access Time (WR–RD Mode, see Fig. 5b)
t_{RI}	140	200	225	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{INTL}[2]	700	–	–	ns typ	$\overline{WR}$ to $\overline{INT}$ Delay
	1000	1400	1700	ns max	
t_{ACC2}[3]	70	90	110	ns max	Data Access Time (WR–RD Mode, see Fig. 5a)
t_{IHWR}[2]	100	130	150	ns max	$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)
t_{ID}	50	65	75	ns max	Data Access Time after $\overline{INT}$ (Stand-Alone Operation)

NOTES
[1]Sample tested at 25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]C_L = 50pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

Test Circuits

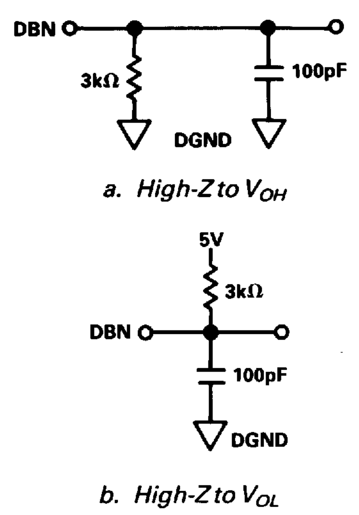


Figure 1. Load Circuits for Data Access Time Test

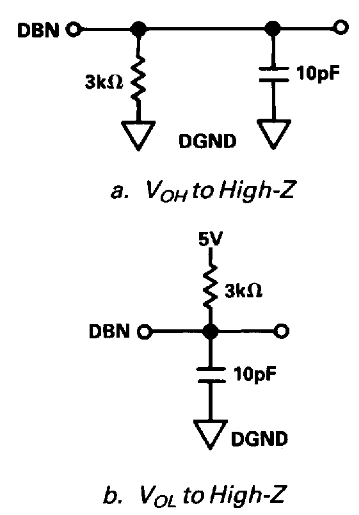


Figure 2. Load Circuits for Data Hold Time Test

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . 0V, +7V
Digital Input Voltage to GND
(Pins 6-8, 13) . . . . −0.3V, V_{DD} +0.3V
Digital Output Voltage to GND
(Pins 2-5, 9, 14-18) . . . . −0.3V, V_{DD} +0.3V
V_{REF} (+) to GND . . . . V_{REF} (−), V_{DD} +0.3V
V_{REF} (−) to GND . . . . 0V, V_{REF} (+)
V_{IN} to GND . . . . −0.3V, V_{DD} +0.3V
Operating Temperature Range
Commercial (K, L Versions) . . . . −40°C to +85°C
Industrial (B, C Versions) . . . . −40°C to +85°C
Extended (T, U Versions) . . . . −55°C to +125°C
Storage Temperature Range . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . +300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by . . . . 6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

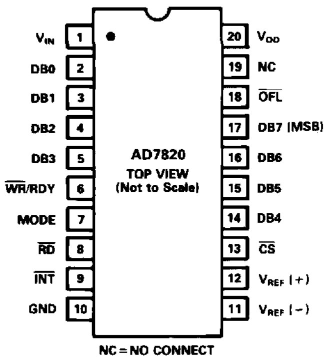
ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (Max)	Package Option[2]
AD7820KN	−40°C to +85°C	±1LSB	N-20
AD7820LN	−40°C to +85°C	±1/2LSB	N-20
AD7820KP	−40°C to +85°C	±1LSB	P-20A
AD7820LP	−40°C to +85°C	±1/2LSB	P-20A
AD7820KR	−40°C to +85°C	±1LSB	R-20
AD7820LR	−40°C to +85°C	±1/2LSB	R-20
AD7820BQ	−40°C to +85°C	±1LSB	Q-20
AD7820CQ	−40°C to +85°C	±1/2LSB	Q-20
AD7820TQ	−55°C to +125°C	±1LSB	Q-20
AD7820UQ	−55°C to +125°C	±1/2LSB	Q-20
AD7820TE	−55°C to +125°C	±1LSB	E-20A
AD7820UE	−55°C to +125°C	±1/2LSB	E-20A

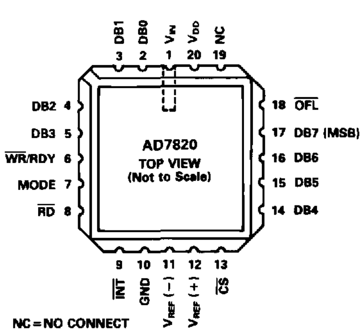
NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-88650.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

PIN CONFIGURATIONS

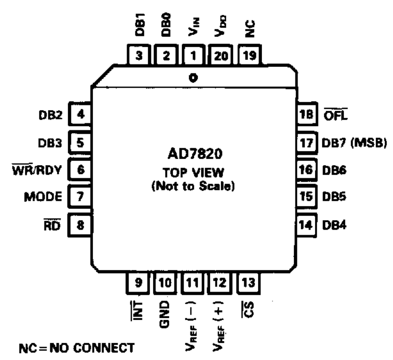
DIP, SOIC



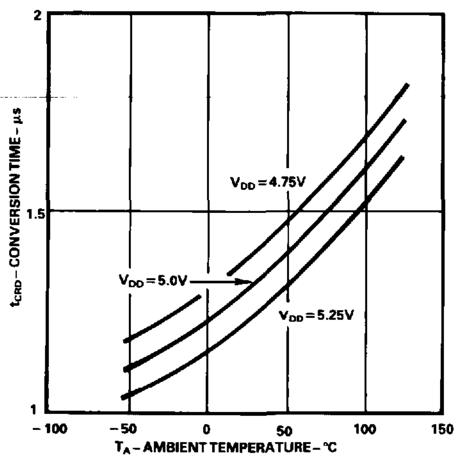
LCCC



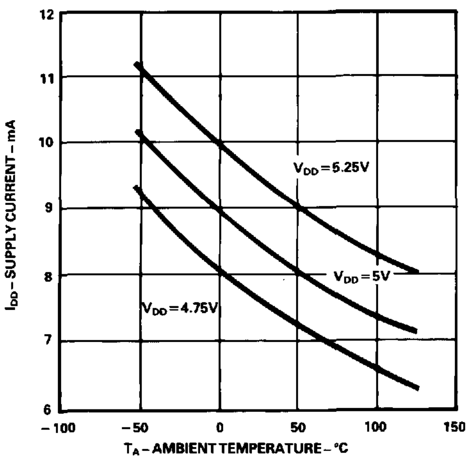
PLCC



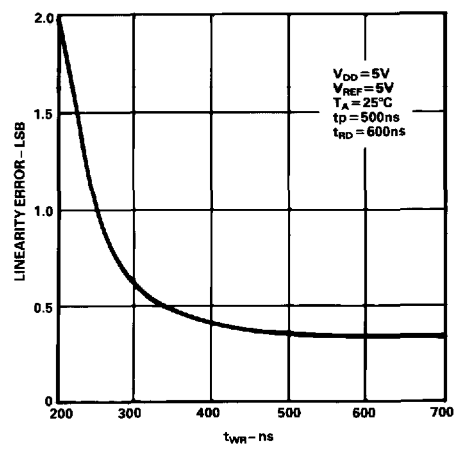
Typical Performance Characteristics—AD7820



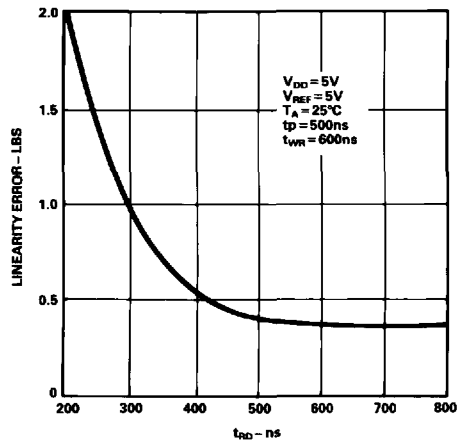
Conversion Time (RD Model) vs. Temperature



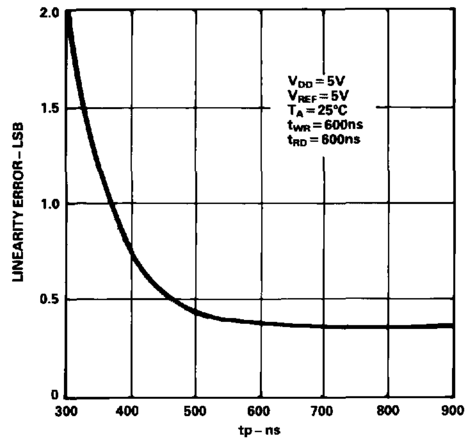
Power Supply Current vs. Temperature (not including reference ladder)



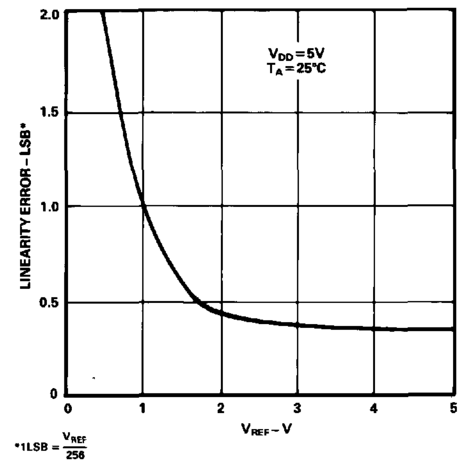
Accuracy vs. t_{WR}



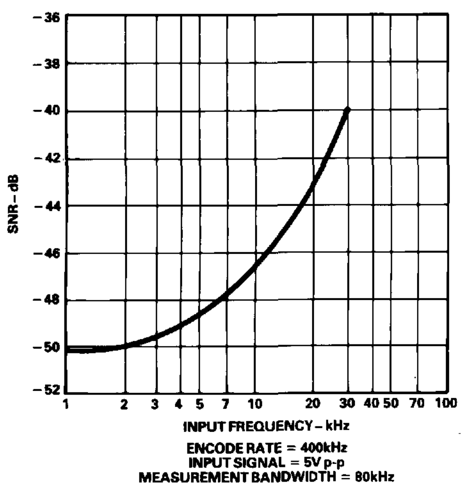
Accuracy vs. t_{RD}



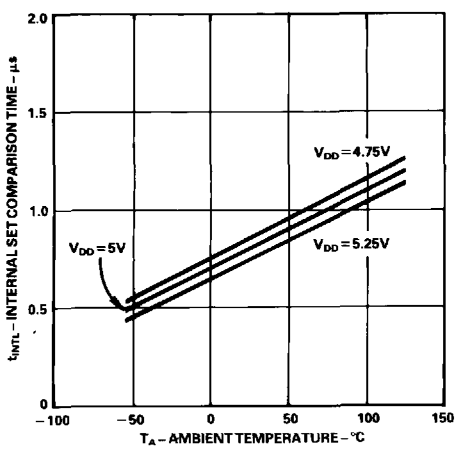
Accuracy vs. tp



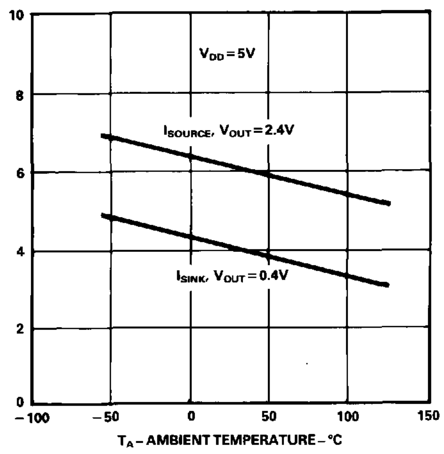
Accuracy vs V_{REF}
[V_{REF} = $V_{REF}(+)$ – $V_{REF}(-)$]



Signal-Noise Ratio vs. Input Frequency



t_{INTL}, Internal Time Delay vs. Temperature



Output Current vs. Temperature

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{IN}	Analog Input. Range: $V_{REF}(-)$ to $V_{REF}(+)$.
2	DB0	Data Output. Three State Output, bit 0 (LSB)
3	DB1	Data Output. Three State Output, bit 1
4	DB2	Data Output. Three State Output, bit 2
5	DB3	Data Output. Three State Output, bit 3
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	Mode	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. It is internally tied to GND through a 50μA current source. See Digital Interface section.
8	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data from the part. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{RD}$ or $\overline{CS}$. See Digital Interface section.
10	GND	Ground
11	$V_{REF}(-)$	Lower limit of reference span. Range: $GND \leq V_{REF}(-) \leq V_{REF}(+)$
12	$V_{REF}(+)$	Upper limit of reference span. Range: $V_{REF}(-) \leq V_{REF}(+) \leq V_{DD}$
13	$\overline{CS}$	Chip Select Input. $\overline{CS}$, the decoded device address, must be low for $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	Data Output. Three State Output, bit 4
15	DB5	Data Output. Three State Output, bit 5
16	DB6	Data Output. Three State Output, bit 6
17	DB7	Data Output. Three State Output, bit 7 (MSB)
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than $(V_{REF}(+) - 1/2LSB)$, $\overline{OFL}$ will be low at the end of conversion. It is a non three state output which can be used to cascade 2 or more devices to increase resolution.
19	NC	No connection.
20	V_{DD}	Power supply voltage, +5V

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7820 uses a half-flash conversion technique whereby two 4-bit flash A/D converters are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. For a full 8-bit reading to be realized, the upper 4-bit flash, the most significant (MS) flash, performs a conversion to provide the 4 most significant data bits. An internal DAC, driven by the 4 MSBs, then recreates an analog approximation of the input voltage. This analog result is subtracted from the input, and the difference is converted by the lower flash ADC, the least significant (LS) flash, to provide the 4 least significant bits of the output data. The MS flash ADC also has one additional comparator to detect input overrange.

OPERATING SEQUENCE

The operating sequence for the AD7820 in the WR-RD mode is shown in Figure 3. A set-up time of 500ns is required prior to the falling edge of $\overline{WR}$. (This 500ns is required between reading data from the AD7820 and starting another conversion). When $\overline{WR}$ is low the input comparators track the analog input signal, V_{IN}. On the rising edge of $\overline{WR}$, the input signal is sampled and the result for the four most significant bits is latched. $\overline{INT}$ goes low approximately 700ns after the rising edge of $\overline{WR}$. This indicates that conversion is complete and the data result is already in the output latch. $\overline{RD}$ going low then accesses the output data. If a faster conversion time is required, the $\overline{RD}$ line can be brought low 600ns after $\overline{WR}$ goes high. This latches the lower 4 bits of data and accesses the output data on DB0–DB7.

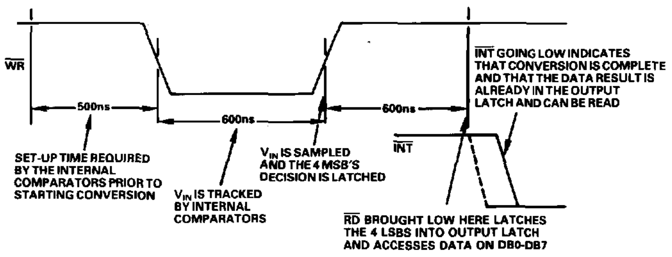


Figure 3. Operating Sequence (WR-RD Mode)

DIGITAL INTERFACE

The AD7820 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low the converter is in the RD mode, with this pin high the AD7820 is set up for the WR-RD mode.

RD Mode

The timing diagram for the RD mode is shown in Figure 4. In the RD mode configuration, conversion is initiated by taking $\overline{RD}$ low. The $\overline{RD}$ line is then kept low until output data appears. It is very useful with microprocessors which can be forced into a WAIT state, with the microprocessor starting a conversion, waiting, and then reading data with a single READ instruction. In this mode, pin 6 of the AD7820 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open drain output (no internal pull-up device) which goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion. An $\overline{INT}$ line is also provided which goes low at the completion of conversion. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

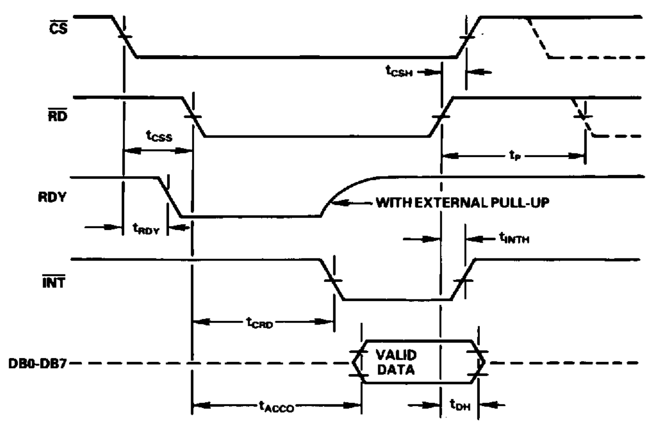


Figure 4. RD Mode

WR-RD Mode

In the WR-RD mode, pin 6 is configured as the WRITE input for the AD7820. With $\overline{CS}$ low, conversion is initiated on the falling edge of $\overline{WR}$. Two options exist for reading data from the converter.

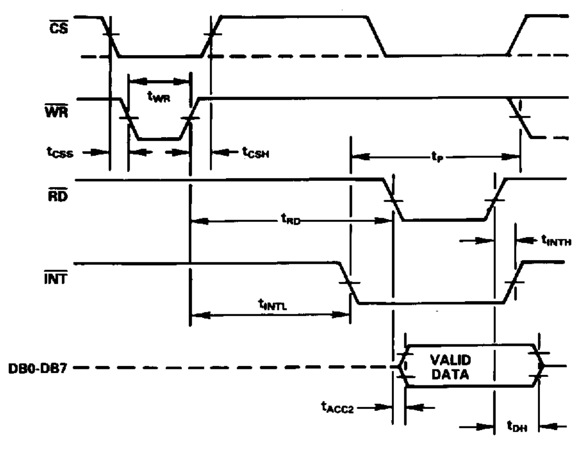


Figure 5a. WR-RD Mode ($t_{RD}>t_{INTL}$)

In the first of these options the processor waits for the $\overline{INT}$ status line to go low before reading the data (see Figure 5a). $\overline{INT}$ typically goes low 700ns after the rising edge of $\overline{WR}$. It indicates that conversion is complete and that the data result is in the output latch. With $\overline{CS}$ low, the data outputs (DB0-DB7) are activated when $\overline{RD}$ goes low. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$.

The alternative option can be used to shorten the conversion time. To achieve this, the status of the $\overline{INT}$ line is ignored and $\overline{RD}$ can be brought low 600ns after the rising edge of $\overline{WR}$. In this case $\overline{RD}$ going low transfers the data result into the output latch and activates the data outputs (DB0-DB7). $\overline{INT}$ also goes low on the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The timing for this interface is shown in Figure 5b.

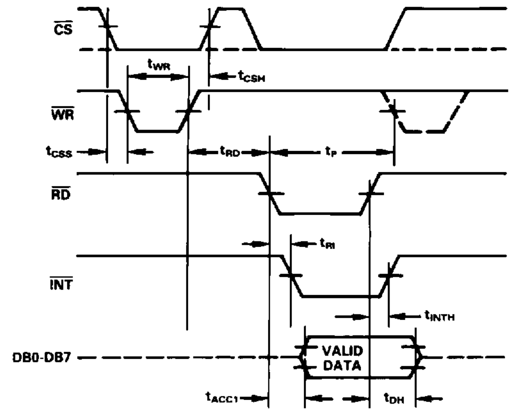


Figure 5b. WR-RD Mode ($t_{RD}<t_{INTL}$)

The AD7820 can also be used in stand-alone operation in the WR-RD mode. $\overline{CS}$ and $\overline{RD}$ are tied low and a conversion is initiated by bringing $\overline{WR}$ low. Output data is valid typically 700ns after the rising edge of $\overline{WR}$. The timing diagram for this mode is shown in Figure 6.

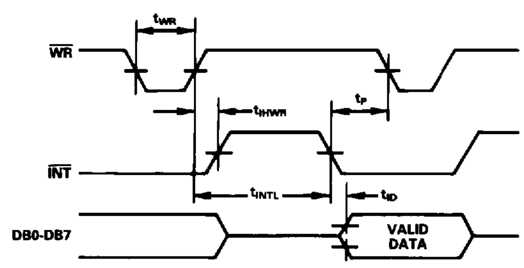


Figure 6. WR-RD Mode Stand-Alone Operation, $\overline{CS}=\overline{RD}=0$

APPLYING THE AD7820

REFERENCE AND INPUT

The two reference inputs on the AD7820 are fully differential and define the zero to full-scale input range of the A/D converter. As a result, the span of the analog input can easily be varied since this range is equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing the reference span, $V_{REF}(+)$–$V_{REF}(-)$, to less than 5V the sensivity of the converter can be increased (i.e., if $V_{REF} = 2V$ then $1LSB = 7.8mV$). The input/reference arrangement also facilitates ratiometric operation.

This reference flexibility also allows the input span to be offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Therefore, although V_{IN} is not itself differential, it will have nearly differential-input capability in most measurement applications because of the reference design. Figure 7 shows some of the configurations that are possible.

INPUT CURRENT

Due to the novel conversion techniques employed by the AD7820, the analog input behaves somewhat differently than in conventional devices. The ADC's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the AD7820 is shown in Figure 8a. When a conversion starts ($\overline{WR}$ low, WR-RD mode), all input switches close, and V_{IN} is connected to the most significant and least significant comparators. Therefore, V_{IN} is connected to thirty one 1pF input capacitors at the same time.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 2kΩ to 5kΩ). In addition, about 12pF of input stray capacitance must be charged. For large source resistances, the analog input can be modelled as an RC network as shown in Figure 8b. As R_S increases, it takes longer for the input capacitance to charge.

In the RD mode, the time for which the input comparators track the analog input is 600ns at the start of conversion. In the WR-RD mode the input comparators track V_{IN} for the duration of the $\overline{WR}$ pulse. Since other factors cause this time to be at least 600ns, input time constants of 100ns can be accommodated without special consideration. Typical total input capacitance values of 45pF allow R_S to be 1.5kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

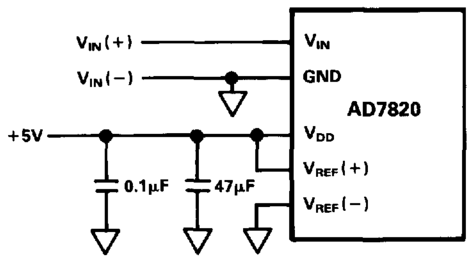


Figure 7a. Power Supply as Reference

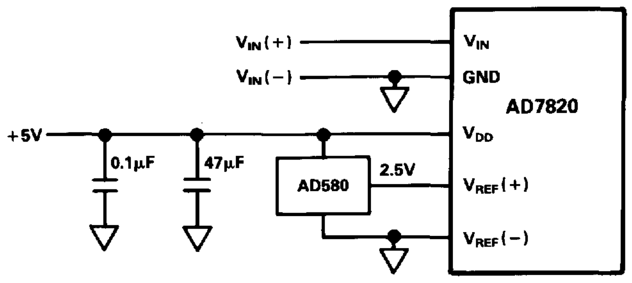


Figure 7b. External Reference 2.5V Full-Scale

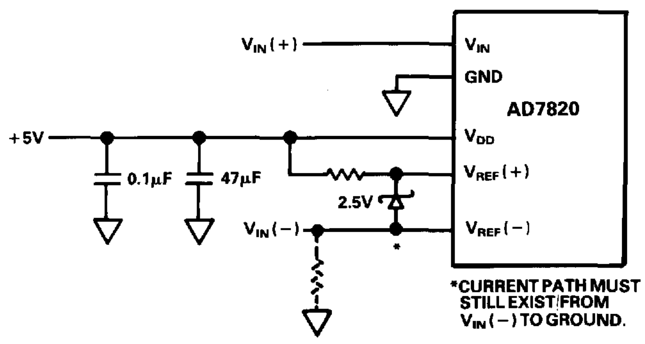


Figure 7c. Input Not Referenced to GND

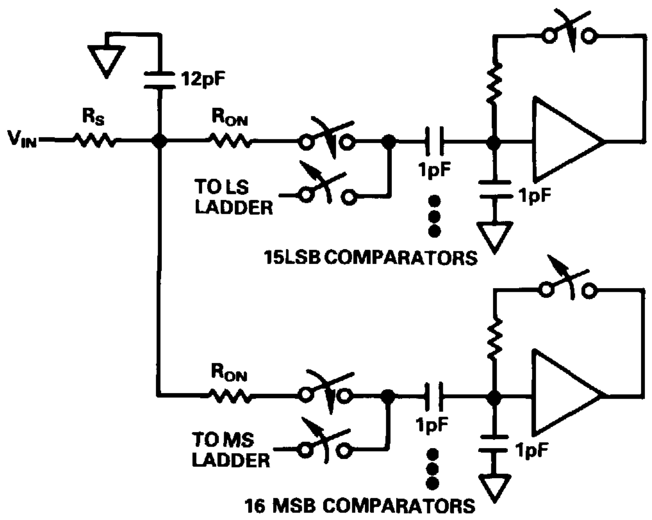


Figure 8a. AD7820 Equivalent Input Circuit

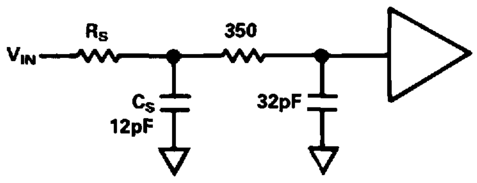


Figure 8b. RC Network Model

INPUT FILTERING

It should be made clear that transients on the analog input signal, caused by charging current flowing into V_{IN} will not normally degrade the ADC's performance. In effect, the AD7820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is low, so at least 600ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients with an external capacitor at the V_{IN} terminal.

INHERENT SAMPLE-HOLD

A major benefit of the AD7820's input structure is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain stable to at least ½LSB throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled and held stationary during the conversion. The AD7820 input comparators, by nature of their input switching inherently accomplish this sample-and-hold function. Although the conversion time for the AD7820 is 1.36μs, the time through which V_{IN} must be ½LSB stable is much smaller. The AD7820 "samples" V_{IN} only when $\overline{WR}$ is low. The value of V_{IN} approximately 100ns (internal propogation delay) after the rising edge of $\overline{WR}$ is the measured value. This value is then used in the least significant flash to generate the lower 4-bits of data.

Input signals with slew rates typically below 200mV/μs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the AD7820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. A SAR type converter with a conversion time as fast as 1μs would still not be able to measure a 5V, 1kHz sine wave without the aid of an external sample-and-hold. The AD7820 with no such help, can typically measure 5V, 10kHz waveforms.

Applications

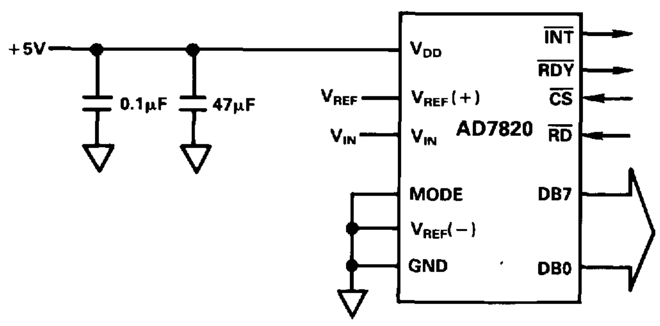


Figure 9a. 8-Bit Resolution

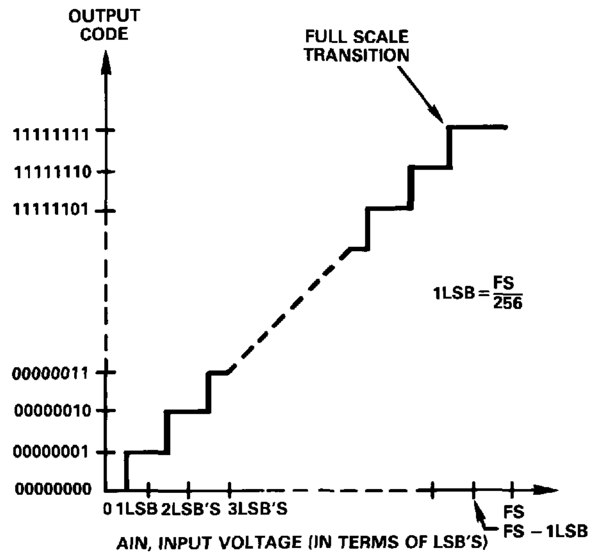


Figure 9b. Nominal Transfer Characteristic for 8-Bit Resolution Circuit

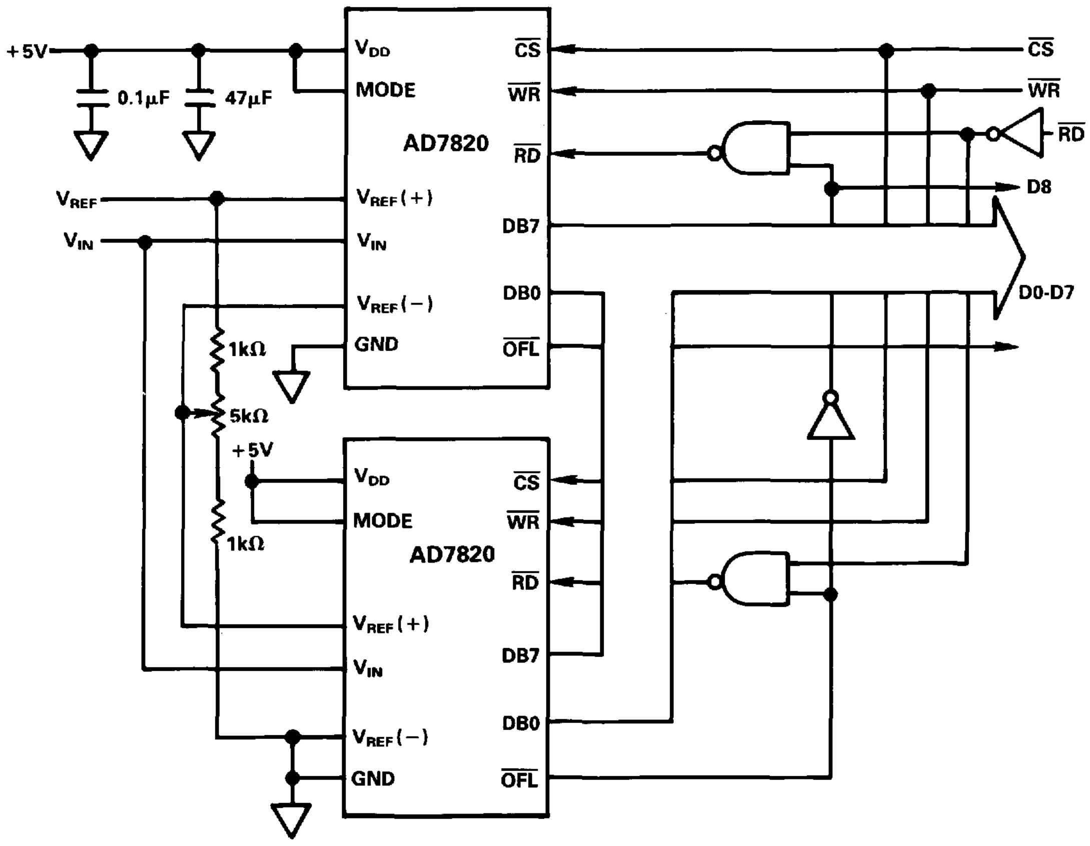


Figure 10. 9-Bit Resolution

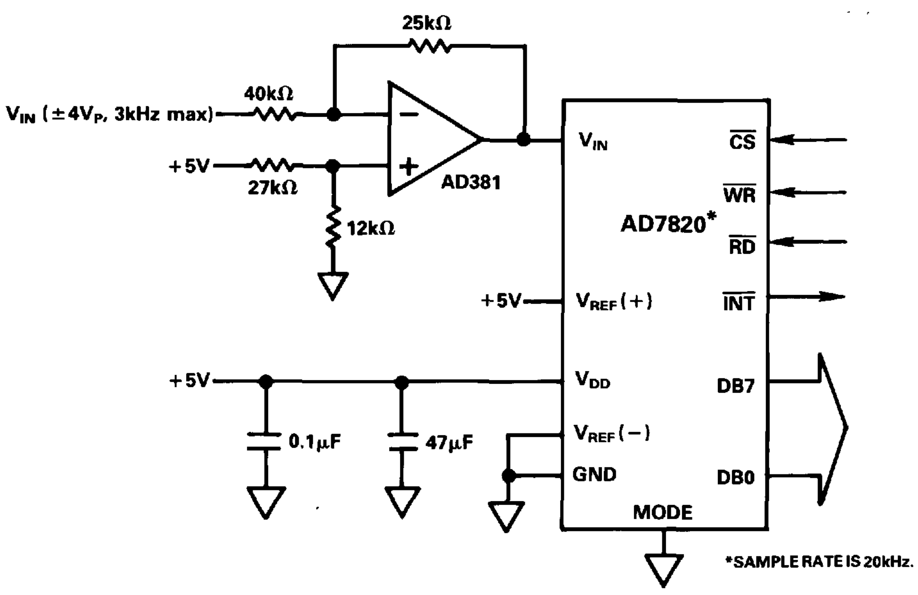


Figure 11. Telcom A/D Converter

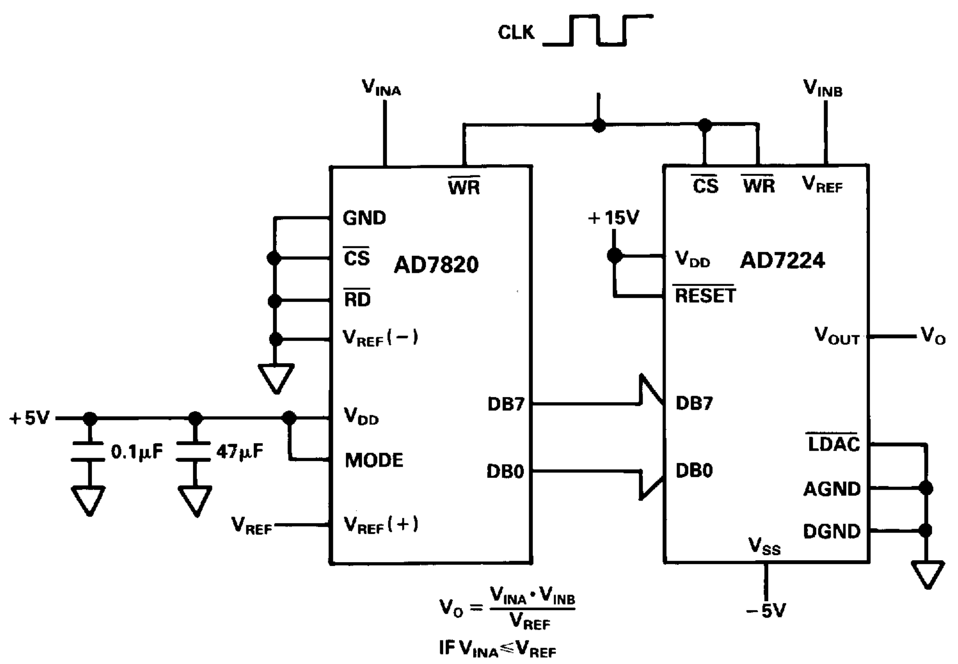


Figure 12. 8-Bit Analog Multiplier

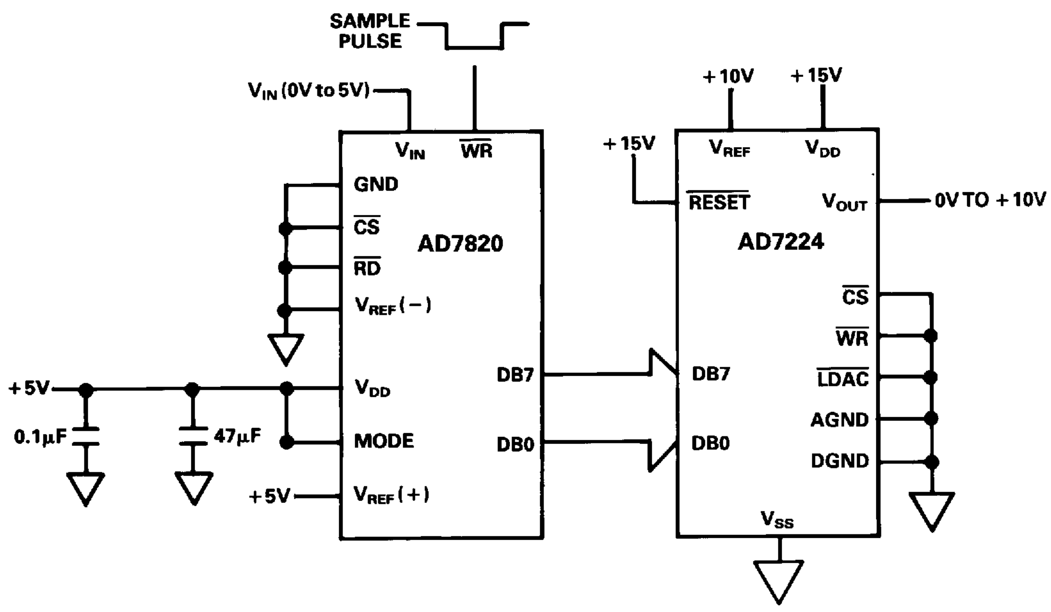
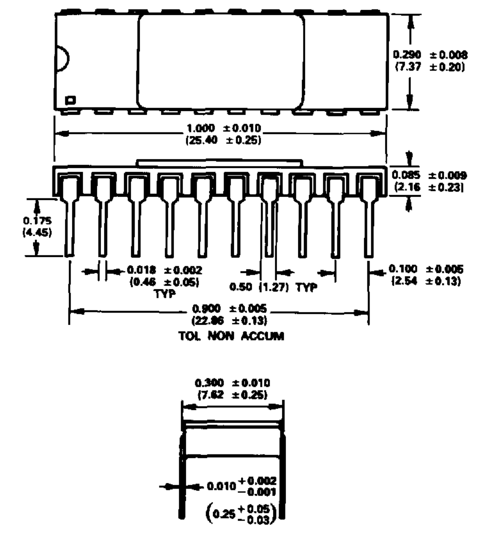


Figure 13. Fast Infinite Sample-and-Hold

MECHANICAL INFORMATION
OUTLINE DIMENSIONS

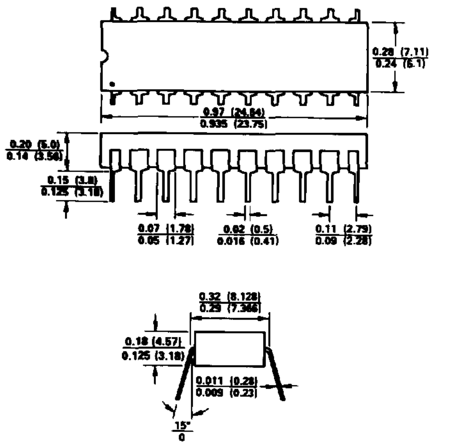
Dimensions shown in inches and (mm).

20-PIN CERAMIC[1]

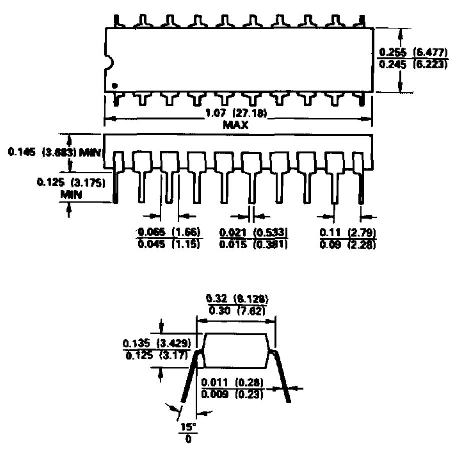


NOTES:
1. LEAD NUMBER 1 IDENTIFIED BY DOT OR NOTCH.
2. LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

20-PIN CERDIP (SUFFIX Q)



20-PIN PLASTIC DIP (SUFFIX N)



NOTE

[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

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