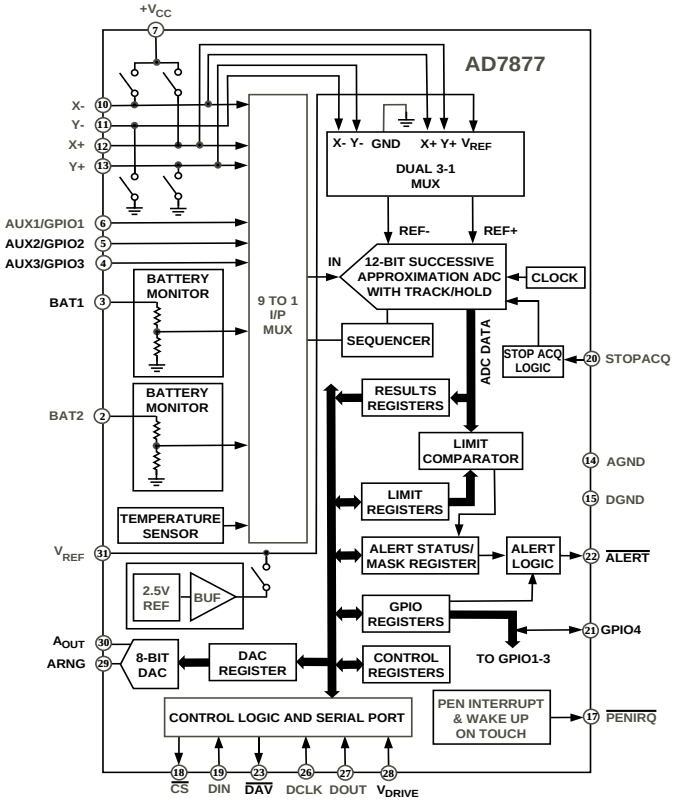
TOUCH SCREEN DIGITIZER

Preliminary Technical Data — AD7877

FEATURES
- 4-Wire Touch Screen Interface
- LCD noise reduction feature (STOPACQ pin)
- On-Chip Temperature Sensor: -40°C to +85°C
- On-Chip 2.5 V Reference
- On-Chip 8-Bit DAC
- 3 Auxiliary Analog Inputs
- One Dedicated & 3 Optional GPIOs
- 2 Direct Battery Measurement Channels (0.5V to 5V)
- 3 Interrupt outputs
- Automatic Conversion Sequencer & Timer
- Touch-Pressure Measurement
- Wake up on Touch Function
- Specified Throughput Rate of 125 ksps
- Single Supply, V_{CC} of 2.7 V to 5.25 V
- ESD Protection on all analogue pins
- Shutdown Mode: 1 µA max

APPLICATIONS
- Personal Digital Assistants
- Smart Hand-held Devices
- Touch-screen Monitors
- Point-of-Sales Terminals
- Pagers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7877 is a 12-bit successive-approximation ADC with a synchronous serial interface and low on-resistance switches for driving touch screens. The AD7877 operates from a single 2.7 V to 5.25 V power supply (functional operation to 2.2V), and features throughput rates of 125 ksps.

The AD7877 features direct battery measurement on two inputs, temperature measurement and touch-pressure measurement. The AD7877 also has an on-board reference of 2.5 V. When not in use, it can be shutdown to conserve power. An external reference can also be applied and can be varied from 1 V to $+V_{CC}$, while the analog input range is from 0 V to V_{REF}. The device includes a shutdown mode which reduces the current consumption to less than 1µA.

To reduce the effects of noise from LCDs, the acquisition phase of the on-board ADC may be controlled via the STOPACQ pin. There is also an on-board DAC, for LCD backlight or contrast control. The AD7877 can run in either a slave or master mode, using a conversion sequencer and timer. It is ideal for battery powered systems such as personal digital assistants with resistive touch screens and other portable equipment. The part is available in a 32 pin Lead Frame Chip Scale Package (LFCSP).

PRODUCT HIGHLIGHTS

1. Functional Mode that reduces effects of noise from LCD, by monitoring a signal via STOPACQ pin
2. Ratiometric conversion mode available eliminating errors due to on board switch resistances.
3. Two Battery Monitor Inputs.
4. Touch-Pressure Measurement capability.
5. Programmable Acquisition Time
6. Low power consumption of 1.37mW at 125 ksps.
7. V_{DRIVE} function allowing serial interface to connect directly to 1.8V processors independently of V_{CC}.
8. Wake up on Touch.
9. Analog input range from 0V to V_{REF}.
10. Sequencer and Timer functions.
11. Programmable First Conversion delay to allow for screen settling time.

REV. PrF 05/12/03

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AD7877-SPECIFICATIONS at $+V_{CC}$ = +2.7 V to 3.6V, V_{REF} = 2.5V internal or external, f_{DCLK} = 2 MHz unless otherwise noted; T_A = -40°C to +85°C , unless otherwise noted.)

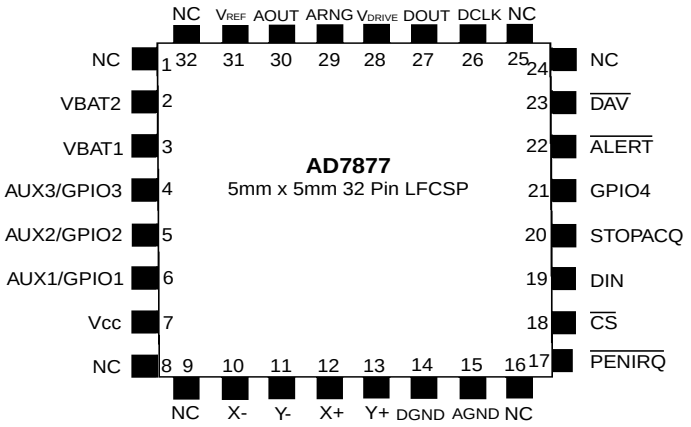
Parameter	Min	Typ	Max	Units	Test Conditions/Comments
A/D CONVERTER :					
DC ACCURACY					
Resolution	12			Bits	
No Missing Codes	12			Bits	
Integral Nonlinearity[1]			±2	LSB	
Differential Nonlinearity[1]			-0.9/+1.5	LSB	
Offset Error[1]			±6	LSB	V_{CC} = 2.7 V
Gain Error[1]			±4	LSB	External reference
Noise		70		µVrms	
Power Supply Rejection		70		dB	
SWITCH DRIVERS					
On-Resistance[1]					
Y+, X+		10		Ω	
Y-, X-		10		Ω	
ANALOG INPUTS					
Input Voltage Ranges	0		V_{REF}	Volts	
DC Leakage Current		±0.1		µA	
Input Capacitance		30		pF	
Accuracy			TBD	%	Worse case channel
REFERENCE INPUT/OUTPUT					
Internal Reference Voltage	2.45		2.55	V	
Internal Reference Tempco		±50		ppm/°C	
V_{REF} Input Voltage Range	+1		$+V_{CC}$	V	
DC Leakage Current			±1	µA	
V_{REF} Input Impedance		1		GΩ	$\overline{CS}$ = GND or $+V_{CC}$; Typically 25Ω when on-board reference enabled.
TEMPERATURE MEASUREMENT					
Temperature Range	-40		+85	°C	
Resolution					
Differential Method[2]		1.6		°C	
Single Conversion Method[3]		0.3		°C	
Accuracy					
Differential Method[2]		±2		°C	
Single Conversion Method[3]		±3		°C	
BATTERY MONITOR					
Input Voltage Range	0.5		+5	V	@V_{REF}=2.5V
Input Impedance		10		kΩ	Sampling; 1GΩ when Battery Monitor OFF
Accuracy			±2	%	External or Internal reference
D/A CONVERTER					
Resolution	8			Bits	
Integral NonLinearity		TBD			Bits
Differential NonLinearity					Guaranteed Monotonic by design.
(VOLTAGE MODE)					
Output Voltage Range	0		$V_{CC}/2$	V	DAC Register Bit 2 = 0, Bit 0 = 0
	0		V_{CC}	V	DAC Register Bit 2 = 0, Bit 0 = 1
Slew Rate		-0.4,+0.5		V/ms	
Output Settling Time		5	TBD	ms	1/4 Scale to 3/4 Scale, R_{LOAD}=TBDkΩ , C_{LOAD} = TBDpF.
Capacitive Load Stability		50		pF	R_{LOAD} = 10kΩ
Output Impedance		75		kΩ	Power down mode.
Short Circuit Current		TBD		mA	

AD7877-SPECIFICATIONS at $+V_{CC}$ = +2.7 V to 3.6V, V_{REF} = 2.5V internal or external, f_{DCLK} = 2 MHz unless otherwise noted; T_A = -40°C to +85°C , unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
D/A CONVERTER:					
(CURRENT MODE)					
Output Current Range	0		1000	µA	DAC Register Bit 2 = 1 Full-scale current is set by R_{RNG}
Output Impedance			Open		Power down mode.
Output Capacitance			TBD	pF	
LOGIC INPUTS					
Input High Voltage, V_{INH}	$0.7V_{DRIVE}$			V	
Input Low Voltage, V_{INL}			$0.3V_{DRIVE}$	V	
Input Current, I_{IN}			±1	µA	Typically 10 nA, V_{IN} = 0 V or $+V_{CC}$
Input Capacitance, C_{IN}[4]			10	pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} -0.2			V	I_{SOURCE} = 250 µA; V_{CC} / V_{DRIVE} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} =250 µA
Floating-State Leakage Current			±10	µA	
Floating-State Output Capacitance[4]			10	pF	
Output Coding					Straight (Natural) Binary
CONVERSION RATE					
Conversion Time		8		µs	$\overline{CS}$ high to $\overline{DAV}$ low.
Throughput Rate			125	ksps	
POWER REQUIREMENTS					
$+V_{CC}$ (Specified Performance)	+2.7		+3.6	V	Functional from 2.2 V to 5.25 V.
V_{DRIVE}	1.65		V_{CC}	V	
I_{CC}[5]					Digital I/Ps = 0 V or V_{CC}.
(f_{SAMPLE} = 125 ksps)		240	380	µA	ADC On,Internal Ref Off, V_{CC}=3.6V
		670		µA	ADC On,Internal Ref ON, V_{CC}=3.6V
		880		µA	ADC On,Internal Ref ON,DAC ON
Normal Mode (f_{SAMPLE} = 12.5 ksps)		170		µA	Internal Reference OFF. V_{CC} =2.7 V, f_{DCLK} =200 kHz
Normal Mode(Static)		150		µA	Internal Reference OFF. V_{CC} = 3.6 V
		580		µA	Internal Reference ON. V_{CC} = 3.6 V
Shutdown Mode (Static)			1	µA	
Power Dissipation[5]					
Normal Mode (F_{SAMPLE}=125 ksps)			1.368	mW	V_{CC}=3.6V. Internal Ref OFF.
			2.412	mW	V_{CC}=3.6 V. Internal Ref ON.
			2.7	mW	V_{CC}=3.6V. Internal Ref On. DAC On.
Shutdown			3.6	µW	V_{CC} = 3.6 V.

NOTES
[1]See Terminology.
[2]Difference between Temp0 and Temp1 measurement. No Calibration necessary.
[3]Temperature Drift is -2.1mV/°C.
[4]Sample tested @ +25°C to ensure compliance.
[5]See POWER VERSUS THROUGHPUT RATE section.
Specifications subject to change without notice.

AD7877 PIN CONFIGURATION



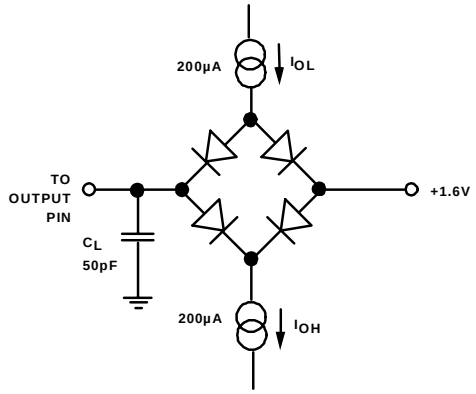


Figure 1. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

$+V_{CC}$ to GND.....–0.3V to 7V
Analog Input Voltage to GND.....–0.3V to V_{CC}+0.3V
Digital Input Voltage to GND.....–0.3V to V_{CC}+0.3V
Digital Output Voltage to GND.....–0.3V to V_{CC}+0.3V
V_{REF} to GND.....–0.3V to V_{CC}+0.3V
Input Current to Any Pin Except Supplies[2].....±10 mA
ESD Rating (analog input pins).....15kV
ESD Rating (other pins).....2kV
Operating Temperature Range..... 40°C to +85°C
Storage Temperature Range.....–65°C to +150°C
Junction Temperature.....+150°C
LFCSP Package:
Power Dissipation.....450mW
q_{JA} Thermal Impedance.....135.7°C/W
Lead Temperature, Soldering:
Vapor Phase (60 secs).....+215°C
Infrared (15 secs).....+220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

ORDERING GUIDE

Model	Operating Range	Package Option[1]	Branding
AD7877CB	-40°C to +85°C	CP-32	AD7877CP
AD7877CB-REEL	-40°C to +85°C	CP-32	AD7877CP
AD7877CB-REEL7	-40°C to +85°C	CP-32	AD7877CP
EVAL-AD7877EB	Evaluation Board		

NOTES
[1]CP = LFCSP.

Timing Specifications[1] at T_A = T_{MIN} to T_{MAX}, unless otherwise noted; V_{CC} = +2.7 V to +5.25 V , V_{REF} = +2.5 V.

Parameter	Limit at T_{MIN}, T_{MAX} AD7877	Units	Description
f_{DCLK} [2]	TBD	kHz min	
	20	MHz max	
t_{ACQ}	1.5	µs min	Acquisition time.
t_1	TBD	ns min	$\overline{CS}$ falling edge to first DCLK rising edge.
t_2	200	ns min	DCLK High Pulse Width.
t_3	200	ns min	DCLK Low Pulse Width.
t_4	TBD	ns min	DIN setup time.
t_5	TBD	ns min	DIN hold time.
t_6	TBD	ns max	$\overline{CS}$ falling edge to DOUT Tri-State Disabled.
t_7 [3]	TBD	ns max	DOUT setup time.
t_8 [4]	TBD	ns max	$\overline{CS}$ Rising edge to DOUT High Impedance.
t_9	0	ns min	$\overline{CS}$ Rising edge to DCLK Ignored

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.6 Volts.

[2]Mark/Space ratio for the DCLK input is 40/60 to 60/40.

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.4 V or 2.0 V.

[4]t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8 quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

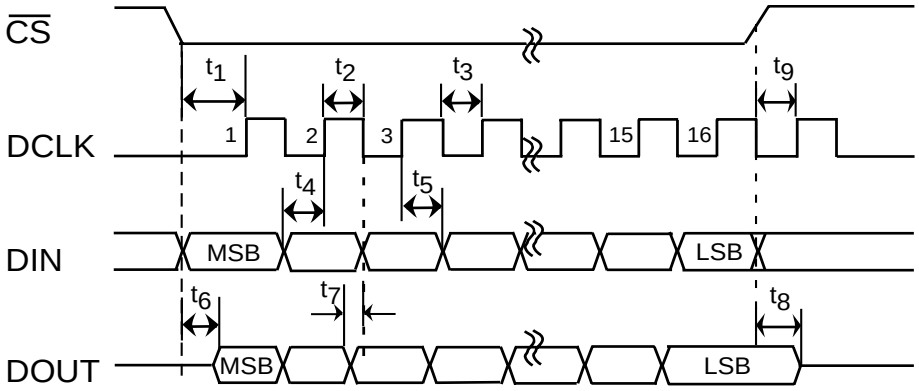


Figure 2. Detailed Timing Diagram

TERMINOLOGY

Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e. AGND + 1LSB

Gain Error

This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1 LSB) after the offset error has been adjusted out.

On-Resistance

This is a measure of the ohmic resistance between the drain and source of the switch drivers.

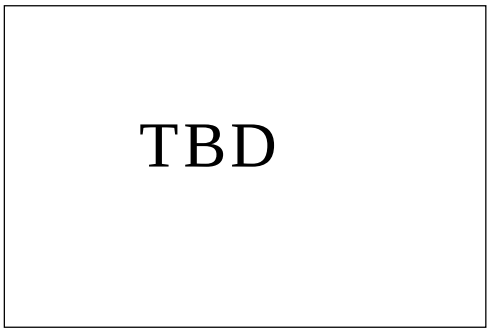
PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Function
1	NC	No Connect.
2	BAT2	Battery Monitor Input. ADC input Channel 7.
3	BAT1	Battery Monitor Input. ADC input Channel 6.
4	AUX3/GPIO3	Auxiliary Input. ADC input Channel 5. Can be reconfigured as GPIO pin.
5	AUX2/GPIO2	Auxiliary Input. ADC input Channel 4. Can be reconfigured as GPIO pin.
6	AUX1/GPIO1	Auxiliary Input. ADC input Channel 3. Can be reconfigured as GPIO pin.
7	$+V_{CC}$	Power Supply Input. The $+V_{CC}$ range for the AD7877 is from +2.2 V to +5.25 V.
8-9	NC	No Connect.
10	X-	Touchscreen Position Input.
11	Y-	Touchscreen Position Input. ADC input Channel 2.
12	X+	Touchscreen Position Input. ADC input Channel 0.
13	Y+	Touchscreen Position Input. ADC input Channel 1.
14	DGND	Digital Ground. Ground reference for all digital circuitry on the AD7877. All digital input signals should be referred to this voltage.
15	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7877. All analog input signals and any external reference signal should be referred to this voltage.
16	NC	No Connect.
17	$\overline{PENIRQ}$	Pen Interrupt. Digital Active Low output (has 50 kΩ internal pull-up resistor).
18	$\overline{CS}$	Chip Select Input. Active low logic input. This input provides the dual function of initiating conversions on the AD7877 and also enables the serial input/output register.
19	DIN	SPI Serial Data Input. Data to be written to the AD7877's Control Register is provided on this input and is clocked into the register on the rising edge of DCLK.
20	STOPACQ	Stop Acquisition pin. A signal applied to this pin can be monitored, so that acquisition of new measurements by the ADC is halted while the signal is active. Used to reduce the effect of noise from an LCD screen on the touchscreen measurements.
21	GPIO4	Dedicated general-purpose logic input/output pin.
22	$\overline{ALERT}$	Digital Active Low Output. Interrupt output, which goes low if a GPIO data bit is set or if AUX1, TEMP1, BAT1 or BAT2 measurement is out of range.
23	$\overline{DAV}$	Data Available Output. Active Low Logic output. Asserts Low when new data is available in the AD7877 result registers. This output is high impedance when $\overline{CS}$ is high.
24-25	NC	No Connect.
26	DCLK	External Clock Input. Logic input. DCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7877's conversion process.
27	DOUT	Serial Data Output. Logic Output. The conversion result from the AD7877 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the DCLK input. This output is high impedance when $\overline{CS}$ is high.
28	V_{DRIVE}	Logic Power Supply input. The voltage supplied at this pin determines what voltage the serial interface of the AD7877 will operate at.
29	ARNG	When DAC is in current output mode, a resistor from ARNG to GND sets the output range.
30	AOUT	Analog Output Voltage or Current from D/A Converter.

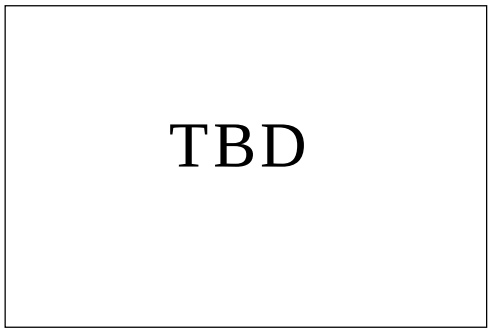
Pin Function Description

Pin No.	Pin Mnemonic	Function
31	VREF	Reference output for the AD7877. Alternatively an external reference can be applied to this input. The voltage range for the external reference is +1.0V to +VCC. For specified performance it is +2.5 V on the AD7877. The internal 2.5 V reference is available on this pin for use external to the device. The reference output must be buffered before it is applied elsewhere in a system. TBD: (A capacitor of 0.1µF is strongly recommended between the VREF pin and GND to reduce system noise effects.)
32	NC	No Connect.

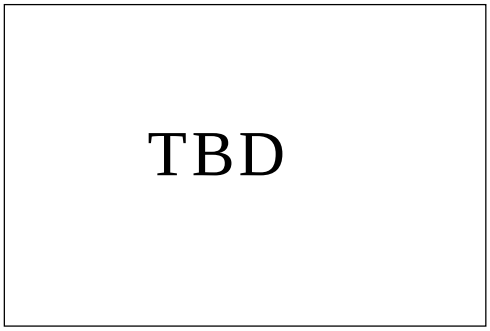
Typical Performance Characteristics at T_A = +25°C, $+V_{CC}$ = +2.7 V, V_{REF} = +2.5 V, f_{SAMPLE} =125 kHz, f_{DCLK} = 16 x f_{SAMPLE} = 2 MHz,unless otherwise noted.



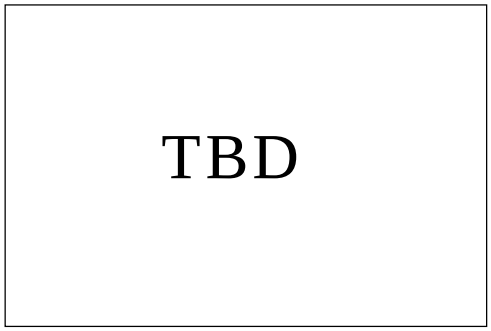
TPC 1. Supply Current vs Temperature



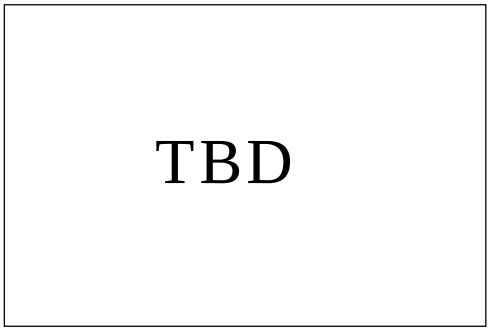
TPC 4. Shutdown Supply Current vs Temperature



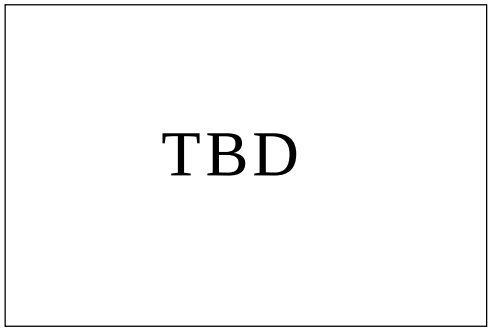
TPC 2. Supply Current vs $+V_{CC}$



TPC 5. Change in Offset vs Temperature

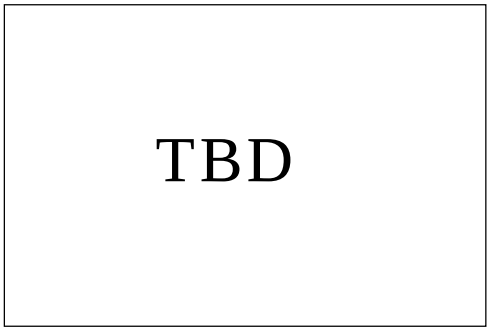


TPC 3. Change in Gain vs Temperature

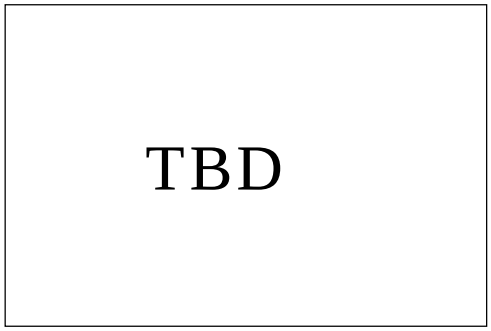


TPC 6. External Reference Current vs Sample Rate

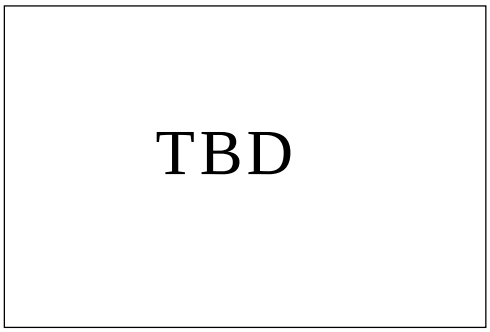
Typical Performance Characteristics at T_A = +25°C, $+V_{CC}$ = +2.7 V, V_{REF} = +2.5 V, f_{SAMPLE} =125 kHz, f_{DCLK} = 16 x f_{SAMPLE} = 2 MHz,unless otherwise noted.



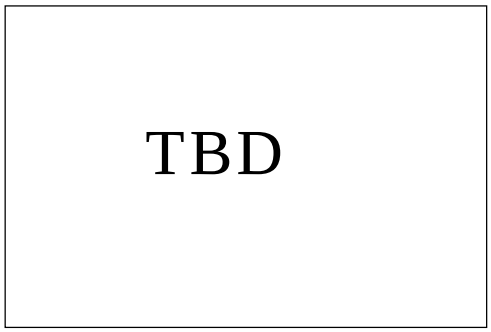
TPC 7. Switch On Resistance vs $+V_{CC}$ ($X+, Y+$: $+V_{CC}$ to Pin; $X-, Y-$: Pin to GND)



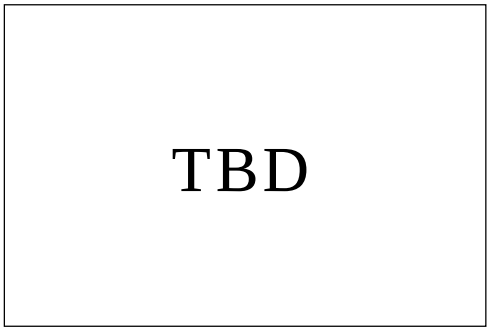
TPC 10. Switch On Resistance vs Temperature ($X+, Y+$: $+V_{CC}$ to Pin; $X-, Y-$: Pin to GND)



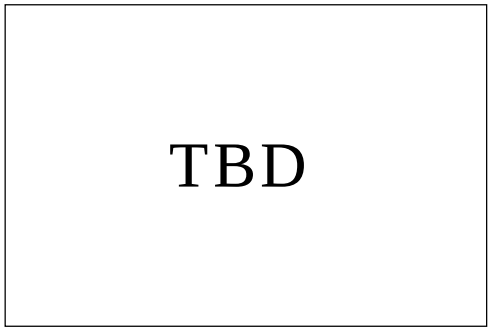
TPC 8. Maximum Sampling Rate vs R_{IN}



TPC 11. Internal V_{REF} vs Temperature

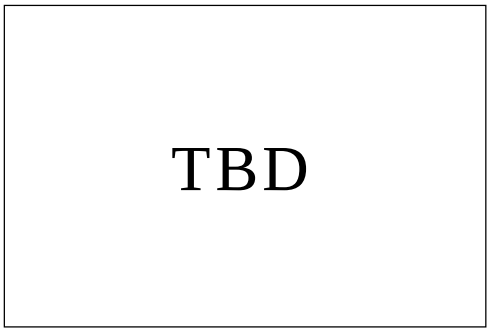


TPC 9. External Reference Current vs Temperature

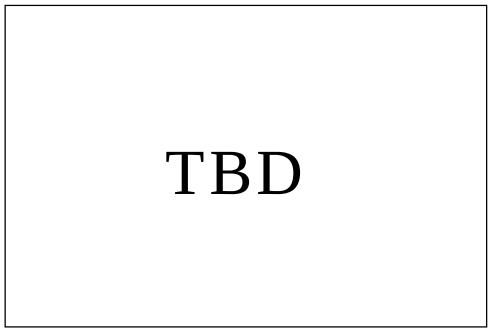


TPC 12. Internal V_{REF} vs $+V_{CC}$

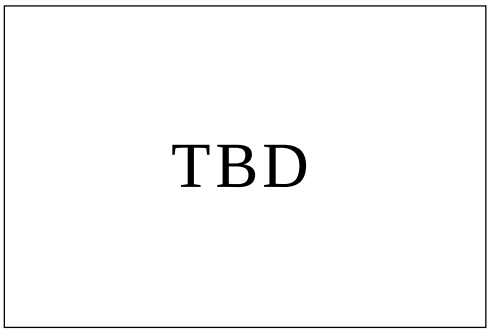
Typical Performance Characteristics at T_A = +25°C, $+V_{CC}$ = +2.7 V, V_{REF} = +2.5 V, f_{SAMPLE} =125 kHz, f_{DCLK} = 16 x f_{SAMPLE} = 2 MHz,unless otherwise noted.



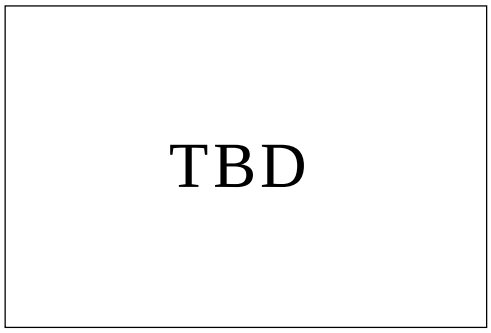
TPC 13 . ADC Code vs Temperature (2.7V Supply)



TPC 16. Temp0 ADC Code vs V_{SUPPLY} (25°C)

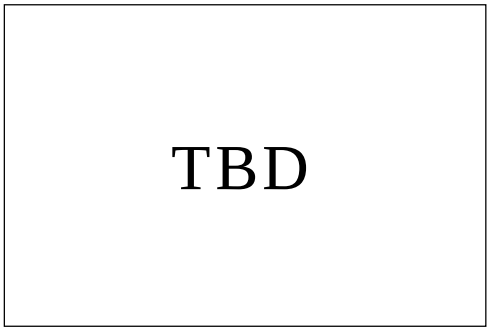


TPC 14 . Temp1 ADC Code vs V_{SUPPLY} (25°C)

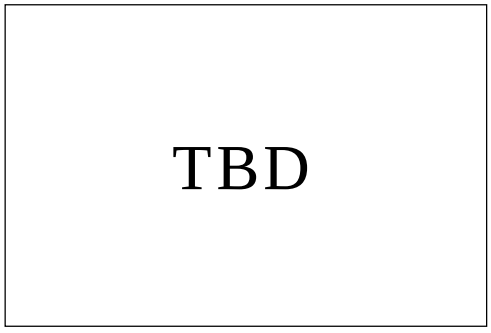


TPC 17. Auxiliary Channel Dynamic Performance

TPC 17. shows a typical FFT plot for the auxiliary channels of the AD7877 at 125 kHz sample rate and 10 kHz input frequency.



TPC 15 Internal V_{REF} vs Turn-on Time



TPC 18. DAC Source & Sink Current Capability

Typical Performance Characteristics at T_A = +25°C, $+V_{CC}$ = +2.7 V, V_{REF} = +2.5 V, f_{SAMPLE} =125 kHz, f_{DCLK} = 16 x f_{SAMPLE} = 2 MHz,unless otherwise noted.

TBD

TPC 19.DAC Half-Scale Settling (1/4 to 3/4 Scale Code Change)

TBD

TPC 20.Output Current vs DAC Input Code, (Voltage Mode)

CIRCUIT INFORMATION

The AD7877 is a complete, 12-bit data acquisition system for digitizing positional inputs from a touchscreen in PDAs and other devices. In addition it can monitor two battery voltages, ambient temperature and three auxiliary analog voltages, with high and low limit comparisons on three of the inputs, and has up to four general-purpose logic I/O pins.

The core of the AD7877 is a high-speed, low-power, 12-bit A to D converter with input multiplexer, on-chip track/hold and on-chip clock. The results of conversions are stored in 11 results registers, and the results from one auxiliary input and two battery inputs can be compared with high and low limits stored in limit registers to generate an out of limit $\overline{\text{ALERT}}$. The AD7877 also contains low-resistance analog switches to switch the X and Y excitation voltages to the touchscreen, a STOPACQ pin to control the ADC acquisition period, 2.5 V reference, on-chip temperature sensor and 8-bit DAC to control LCD contrast. Control of, and communication with, the device is achieved via a high-speed SPI serial bus.

Operating from a single supply from +2.2 V to +5 V, the AD7877 offers throughput rates up to 125 kHz.

The device is available in a 5mm by 5mm 32 pin Lead-Frame chip scale package.

TOUCH SCREEN PRINCIPLES

A four-wire touch screen consists of two flexible, transparent, resistive coated layers that are normally separated by a small air gap. The X layer has conductive electrodes running down the left and right edges, allowing an excitation voltage to be applied across the X layer from left to right.

The Y layer has conductive electrodes running along the top and bottom edges, allowing an excitation voltage to be applied down the layer from top to bottom.

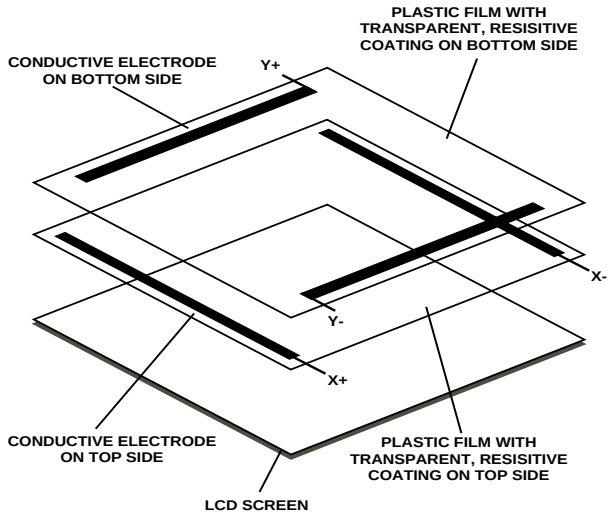


Figure 3. Basic Construction of a Touch Screen

Provided the layers are of uniform resistivity, the voltage at any point between the two electrodes will be proportional to the horizontal position in the case of the X layer and the vertical position in the case of the Y layer.

When the screen is touched, the two layers will make contact. If only the X layer is excited, the voltage at the point of contact, and hence the horizontal position, can be sensed at one of the Y-layer electrodes. Similarly, if only the Y layer is excited, the voltage, and hence the vertical position, can be sensed at one of the X electrodes. By switching alternately between X and Y excitation and measuring the voltages, the X and Y co-ordinates of the contact point can be found.

As well as measuring the X and Y co-ordinates, it is also possible to estimate the touch pressure by measuring the contact resistance between the X and Y layers. The AD7877 is designed to facilitate this measurement.

Figure 2 shows an equivalent circuit of the analog input structure of the AD7877, showing the touch screen switches, the main analog multiplexer, the ADC with analog and differential reference inputs, and the dual 3 to 1 multiplexer that selects the reference source for the ADC.

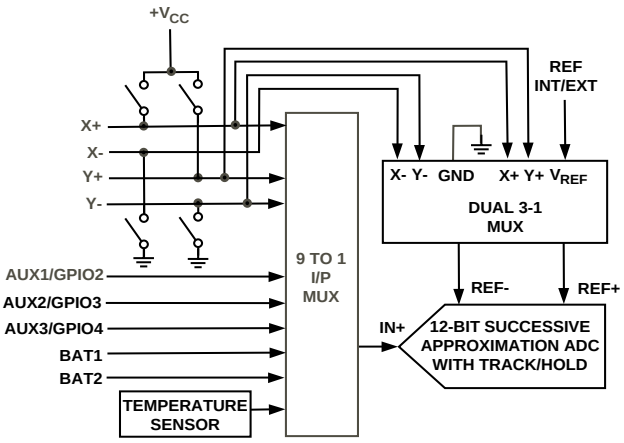


Figure 4. Analog Input Structure

The AD7877 can be set up to convert specific input channels, or a sequence of channels can be converted automatically. The results of ADC conversions are stored in the results registers. This is described in the section on the Serial Interface and Control Logic.

When measuring the ancillary analog inputs (AUX1 to AUX3, BAT1 and BAT2), the ADC uses the internal reference, or an external reference applied to the V_{REF} pin, and the measurement is referred to GND.

When measuring the touchscreen inputs, it is possible to measure using the internal (or external) reference, or to use the touchscreen excitation voltage as the reference and perform a ratiometric, differential measurement. The differential method is the default and is selected by clearing the SER/DFR bit (bit 11) in Control Register 1. The single-end method is selected by setting this bit.

The single-ended method is illustrated for the Y position in Figure 5. For the X-position, the excitation voltage would be applied to X+ and X- and the voltage measured at Y+ .

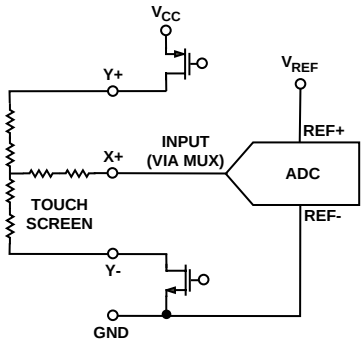


Figure 5. Single-Ended Conversion of Touch Screen Inputs

The ratiometric method is illustrated in Figure 6. Here, the negative input of the ADC reference is tied to Y- and the positive input is connected to Y+, so the screen excitation voltage provides the reference for the ADC.

The input of the ADC is connected to X+, to determine the Y position.

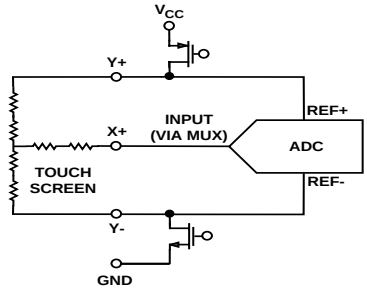


Figure 6. Ratiometric Conversion of Touch Screen Inputs

Both methods have advantages and disadvantages.

The disadvantages of the single-ended method are:

1. It can only be used if V_{CC} is close to V_{REF}. If V_{CC} is greater than V_{REF}, some positions on the screen will be outside the range of the ADC. If V_{CC} is less than V_{REF}, the full range of the ADC will not be utilized.
2. The ratio of V_{CC} to V_{REF} must be known. If V_{REF} and/or V_{CC} vary relative to one another, this will introduce errors.
3. Voltage drops across the switches can introduce errors. Touch screens may have a total end-to-end resistance between 200 Ω and 900 Ω. Taking the lowest screen resistance of 200 Ω and a typical switch resistance of 10Ω, this could reduce the apparent excitation voltage to 200/220 × 100 = 90% of its actual value. In addition, the voltage drop across the low-side switch adds to the ADC input voltage. This introduces an offset into the input voltage that means it can never reach zero.

The advantage of the single-ended method is that the touchscreen excitation voltage can be switched off once the signal has been acquired. As a screen can draw over 1mA, this is a significant consideration for a battery-powered system.

The single-ended method is adequate for applications where the input device is a fairly blunt and imprecise in-

strument such a finger. For greater accuracy, the ratiometric method has two significant advantages.

1. Since the reference to the ADC is provided from the actual voltage across the screen, voltage drops across the switches have no effect.
2. Since the measurement is ratiometric, it does not matter if the voltage across the screen varies in the long term. (it must not change after the signal has been acquired).

The disadvantage of the ratiometric method is that the screen must be powered up all the time, because it provides the reference voltage for the ADC.

TOUCH PRESSURE MEASUREMENT

The pressure applied to the touchscreen via a pen or finger may also be measured with the AD7877 with some simple calculations. The contact resistance between the X and Y plates is measured. This provides a good indication of the size of the depressed area and hence the applied pressure. The area of the spot touched is proportional to the size of the object touching it. The size of this resistance (R_{TOUCH}) can be calculated using two different methods.

The first method requires the user to know the total resistance of the X-plate tablet (R_X). Three touchscreen conversions are required:

1. Measurement of the X position, $X_{Position}$. (Y+ input).

2. Measurement of the Y- input with the excitation voltage applied to Y+ and X- (Z1 measurement).

3. Measurement of the X+ input with the excitation voltage applied to Y+ and X- (Z2 measurement).

These three measurements are illustrated in Figure 7.

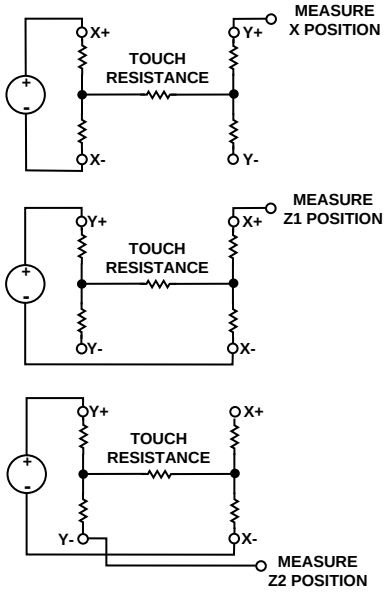


Figure 7. Three Measurements Required for Touch Pressure

The AD7877 has two special ADC channel settings that configure the X and Y switches for Z1 and Z2 measurement and store the results in the Z1 and Z2 results registers. The Z1 measurement is ADC channel 1010b and the result is stored in the register with read address 11010b. The Z2 measurement is ADC channel 0010b and the result is stored in the register with read address 10010b.

The touch resistance may then be calculated using the following equation:

$$R_{TOUCH} = (R_{XPlate}) \times (X_{Position}/4096) \times [(Z_2/Z_1)-1]$$

The second method requires that the resistance of both the X-plate and Y-plate tablets are known. Three touchscreen conversions again are required, a measurement of the X-Position ($X_{Position}$), Y-Position ($Y_{Position}$), and Z_1 position.

The following equation will also calculate the touch resistance:

$$R_{TOUCH} = R_{XPlate} \times (X_{Position}/4096) \times [(4096/Z_1)-1] - R_{YPlate} \times [1 - (Y_{Position})/4096)]$$

STOPACQ PIN

As explained previously, touchscreens are composed of two resistive layers, placed over an LCD screen. Because these layers are in close proximity to the LCD screen, noise can be coupled from the screen onto these resistive layers, causing errors in the touch screen positional measurements. For instance, a jitter may be noticeable in the cursor on-screen. In most LCD touch screen systems, there is a signal such as an LCD 'invert' signal, or other control signal, present, and noise is mainly coupled onto the touchscreen during this signal's active period, as shown in the figure below.

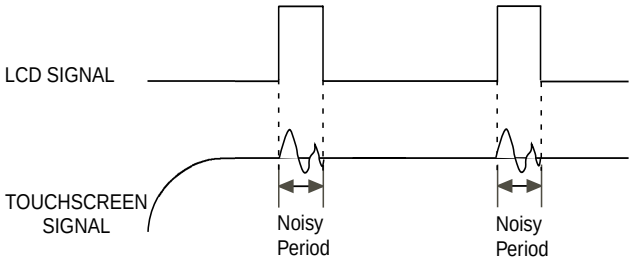


Figure 8. LCD Noise effects Touchscreen Measurements

It is only during the sample, or acquisition phase, of the AD7877's ADC's operation, that noise from the LCD screen has an effect on the ADC's measurements. During the hold, or conversion phase, the noise has no effect, as the voltage at the input of the ADC has already been acquired. So, no acquisitions should take place during the LCD control signal active period.

To minimize the effect of noise on the touch screen measurements, the LCD control signal should be applied to the STOPACQ pin. To ensure that acquisition never takes place during the noisy period where the LCD signal is active, the AD7877 monitors this signal. No acquisitions take place when the control signal is active. Any acquisition that is in progress when the signal becomes active will be aborted, and will restart when the signal becomes inactive again.

To cater for signals of different polarities on the STOP-ACQ pin, there is a user-programmable register bit to indicate if the signal is active high or low. POL bit is bit 3 in Control Register 2, address 02h. Setting POL to 1 indicates the signal on STOPACQ is active high, setting POL to 0 indicates it is active low. POL defaults to 0 on power-up. To disable monitoring of STOPACQ, the pin should be tied low if POL=1, or tied high if POL=0.

The signal on STOPACQ will have no effect while the ADC is in conversion mode, or during the first conversion delay time. (See Control Register section for more information on first conversion delay.)

When enabled, the STOPACQ monitoring function is implemented on all input channels to the ADC ; AUX1, AUX2, BAT1, BAT2, TEMP1, TEMP2, as well as the touchscreen input channels, X+, X-, Y+, Y-.

TEMPERATURE MEASUREMENT

There are two temperature measurement options available on the AD7877, the Single Conversion Method and the Differential Conversion Method. Single conversion requires only a single measurement on ADC channel 1000b. Differential conversion requires two measurements, one on ADC channel 1000b and a second on ADC channel 1001b. The results are stored in results registers, addresses 11000b (TEMP1) and 11001b (TEMP2). It should be noted that the AD7877 does not provide an explicit output of the temperature reading. Some external calculations must be performed by the system.
Both methods are based on an on-chip diode measurement. The Single Conversion Method makes use of the fact that temperature coefficient of a silicon diode is approximately -2.1 mV/°C. However, this small change is superimposed on the diode forward voltage, which can have a wide tolerance. It is therefore necessary to calibrate by measuring the diode voltage at a known temperature to provide a baseline from which the change in forward voltage with temperature can be measured. This method provides a resolution of approximately 0.3°C and a predicted accuracy of +/- 3°C.

It should be noted that temperature limit comparison is performed on the result in the TEMP1 result register, which is simply the measurement of the diode forward voltage. This means that programming high and low temperature limits is not simply a matter of putting known values in the limit registers. In order to make accurate limit comparisons it will be necessary to calibrate the system to factor out the variability of this voltage, and program in high and low limits that take account of this calibration. This is not as difficult as it might sound. It is not necessary to calibrate at a fixed temperature, only at a known temperature. This can be measured without calibration using the Differential Conversion Method, so it is quite feasible to design an automatic software calibration routine.

The Differential Conversion Method is a two point measurement. The first measurement is performed with a fixed bias current into a diode (when TEMP1 channel is selected) and the second measurement is performed with a fixed multiple of the bias current into the same diode (when TEMP2 channel is selected). The voltage difference in the diode readings is proportional to absolute temperature and is given by the following formula:

$$\Delta V_{BE} = (kT/q)x(\ln N)$$

where V_{BE} represents the diode voltage, N is the bias current multiple, k is Boltzmann's constant and q is the electron charge. This method provides more accurate absolute temperature measurement of +/- 2°C, however the resolution is reduced to approximately 1.6°C.

Assuming a current multiple of 105, (which is a typical value for the AD7877), taking Boltzmann's constant, k = $1.38054x10^{-23}$ electrons volts/degrees Kelvin, the electron charge q = $1.602189x10^{-19}$, then T the ambient temperature in Kelvin would be calculated as follows:

$$\Delta V_{BE} = (kT/q)x(\ln N)$$

$$T\ (^{o}\ \text{Kelvin}) = (\Delta V_{BE} * q)/(k * \ln N)$$

$$= (\Delta V_{BE} \times 1.602189 \times 10^{-19})/(1.38054 \times 10^{-23} \times 4.65)$$

$$T°C = 2.49x10^{3} \times \Delta V_{BE} - 273$$

ΔV_{BE} is calculated from the difference in readings from the first conversion and second conversion. The user must perform the calculations to get $\Delta V_{BE,}$ and then calculate the temperature value in degrees.

Figure 9 shows a block diagram of the Temperature measurement Mode.

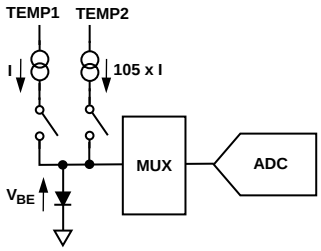


Figure 9. Block Diagram of Temperature Measurement Circuit

TEMPERATURE CALCULATION

If an explicit temperature reading in degrees Celsius is required, then this can be calculated as follows for the Single Measurement method:

1. Calculate the scale factor of the ADC in degrees per LSB.

   Degrees per LSB = ADC LSB size / -2.1mV.

   = (V_{REF}/4096) / -2.1mV

2. Save the ADC output D_{CAL} at the calibration temperature T_{CAL}.
3. Take ADC reading D_{AMB} at temperature to be measured T_{AMB}.
4. Calculate difference in degrees between T_{CAL} and T_{AMB} using:

   $\Delta T = (D_{AMB} - D_{CAL}) \times$ degrees per LSB.

5. Add ΔT to T_{CAL}.

Example:

The internal 2.5 V reference is used.

1. Degrees per LSB = (2.5/4096) / -2.1×10^{-3} = -0.291
2. The ADC output is 983 decimal at 25°C, equivalent to a diode forward voltage of 0.6V.
3. The ADC output at T_{AMB} is 880.
4. ΔT = (880 - 983) × -0.291 = 30 degrees.
5. T_{AMB} = 25 + 30 = 55°C.

To calculate the temperature explicitly using the Differential method:

1. Calculate the LSB size of the ADC in volts.
   LSB = V_{REF}/4096
2. Subtract TEMP1 from TEMP2 and multiply by LSB size to get ΔV_{BE}.
3. Multiply by 2490 and subtract 273 to get the temperature in degrees Celsius.

Example:

The internal 2.5 V reference is used.

1. LSB size = 2.5 V/4096 = 6.1×10^{-4} V (610µV).
2. TEMP1 = 880 and TEMP2 = 1103.
   ΔV_{BE} = (1103 - 880) × 6.1×10^{-4} = 0.136 V
3. T = 0.136 × 2490 - 273 = 65°C.

BATTERY MEASUREMENT

The AD7877 can monitor battery voltages from 0.5V to +5 V on two inputs, BAT1 and BAT2. Figure 8 shows a block diagram of a battery voltage monitored through the BAT1 pin. The BAT2 input circuitry is identical. The voltage to the $+V_{CC}$ of the AD7877 is maintained at the desired supply voltage via the DC/DC regulator while the input to the regulator is monitored. This voltage on BAT1 is divided down by 2 internally, so that a +5 V battery voltage is presented to the ADC as 2.5 V. In order to conserve power, the divider circuit is only on during the sampling of a voltage on BAT1.

The BAT1 input is ADC channel 0110b and the result is stored in register 10110b. The BAT2 input is ADC channel 0111b and the result is stored in register 10111b.

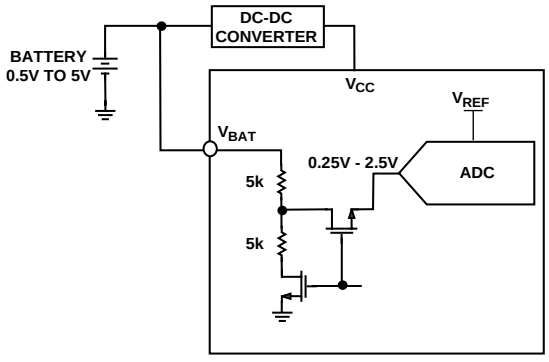


Figure 10. Block Diagram of Battery Measurement Circuit

Figure 10 shows the ADC using the internal reference of 2.5V. If a different reference voltage is used, then the maximum battery voltage the AD7877 can measure will change. The maximum voltage measurable is V_{REF} x2, as this voltage will give a full scale output from the ADC. If a smaller reference is used, say 2V, then the maximum battery voltage measurable is 4V. If a larger reference is used, say 3.5V, then the maximum battery voltage measurable is 7V. The internal reference is particularly suited for use when measuring Li-Ion batteries, where the minimum voltage is circa 2.7V, and the maximum is circa 4.2V. A proper choice of external reference will ensure that other voltage ranges can be well catered for.

AUXILIARY INPUTS

The AD7877 has three auxiliary analog inputs, AUX1 to AUX3. These channels have a full-scale input range from zero volts to V_{REF}. The ADC channel addresses for AUX1 to AUX3 are 0011b, 0100b and 0101b, and the results are stored in registers 10011b, 10100b and 10101b. These pins may also be reconfigured as general purpose logic input/outputs, as described later in the GPIO section.

LIMIT COMPARISON

The AUX1 measurement, the two battery measurements and TEMP1 measurement can all be compared with high and low limits, and an out-of limit result made to generate an alarm output at the $\overline{\text{ALERT}}$ pin. The limits are stored in registers with addresses from 00100b to 01011b. After each of these four channels is converted, it is compared with the corresponding high and low limits. An out-of-limit result will set one of the status bits in the Alert Status/Enable Register.

For more details on these and other registers, refer to the Register Map and Detailed Register Descriptions. For more information on writing and read data, refer to the section on the Serial Interface .

As mentioned previously, the temperature comparison is made using the result of the TEMP1 measurement, which is basically just the diode forward voltage. Since the temperature coefficient of the diode is known, but the actual forward voltage can have a wide tolerance, it is not possible to program the high and low limit registers with predetermined values. Instead, it is necessary to calibrate the temperature measurement, calculate what the TEMP1 reading will be at the high and low limit temperatures, then program those values into the limit registers, as follows:

1. Calculate LSB per degree, = -2.1mV/(V_{REF}/4096)
2. Save the calibration reading D_{CAL} at calibration temperature T_{CAL}.
3. Subtract T_{CAL} from limit temperatures T_{HIGH} and T_{LOW} to get difference in degrees between limit temperatures and calibration temperature.
4. Multiply this values by LSB per degree to get value in LSB.
5. Add these values to digital value at calibration temperature to get digital high and low limit values.

Example:

The internal 2.5V reference is used.

T_{HIGH} = +65°C and T_{LOW} = -10°C.

LSB per degree = $-2.1 \times 10^{-3}/(2.5/4096) = -3.44$.

D_{CAL} = 983 decimal at 25°C.

$D_{HIGH} = (65 - 25) \times -3.44 + 983 = 845$

$D_{LOW} = (-10 - 25) \times -3.44 + 983 = 1103$

DATA ACQUISITION SYSTEM ADVANCED FEATURES

The data acquisition system of the AD7877 has a number of advanced features.

1. Input channel sequenced automatically or selected by CPU.
2. Averaging of from 1 to 16 conversions for noise reduction.
3. Programmable acquisition time.
4. Power management.
5. Programmable ADC power-up delay before first conversion.
6. Choice of internal or external reference.
7. Conversion at pre-programmed intervals.

The data acquisition system is controlled by four registers, Control Registers 1 and 2, and Sequencer Registers 0 and 1.

CONTROL REGISTERS

Control Register 1 contains the ADC channel address, the SER/DFR bit (to choose single or differential methods of touch screen measurement), the read address for reading registers, and two bits to set the ADC mode. See also Detailed Register Descriptions section. Control Register 1 should always be the last register to be programmed prior to starting conversions.

11											0
SER/DFR	CHNL ADD 3	CHNL ADD 2	CHNL ADD 1	CHNL ADD 0	RD ADD 4	RD ADD 3	RD ADD 2	RD ADD 1	RD ADD 0	ADC MODE 1	ADC MODE 0

Figure 11. Control Register 1

Control Register 2 sets the timer, reference, polarity, first conversion delay, averaging and acquisition time. See also Detailed Register Descriptions section.

11											0
AVG 1	AVG 0	ACQ 1	ACQ 0	PM 1	PM 0	FCD 1	FCD 0	POL	REF	TMR 1	TMR 0

Figure 12. Control Register 2.

ADC MODE (CONTROL REGISTER 1 BITS <1:0>)
These bits select the operating mode of the ADC.

MODE1	MODE0	Function
0	0	Do not convert
0	1	Single channel conversion (AD7877 in slave mode)
1	0	Software sequence (Sequence 0 AD7877 in slave mode)
1	1	Hardware sequence (Sequence 1 AD7877 in master mode)

The AD7877 has three operating modes. These are selected by writing to the mode bits in Control register 1, as shown in the previous table.

If the mode bits are 00, no conversion is performed.

If the mode bits are 01, a single conversion is performed on the channel selected by writing to the channel bits of Control Register 1. (Bits 7 to 10) At the end of the conversion, if the TMR bits in Control Register 2 are set to 00, the mode bits will revert to 00 and the ADC will return to no convert mode until a new conversion is initiated by the Host. Setting the TMR bits to a value other than 00 causes the conversion to be repeated, as described in the TIMER section. Figure 13 is a flowchart, showing how the AD7877 operates in mode 01.

The AD7877 can also be programmed to convert a sequence of selected channels automatically. There are two modes for this, known as software or slave mode and hardware or master mode.

For slave mode operation, the channels to be digitized are selected by setting the corresponding bits in Sequencer Register 0. Conversion is initiated by writing 10 to the mode bits of Control Register 1. The ADC will then digitize the selected channels and store the results in the corresponding results registers. At the end of the conversion, if the TMR bits in Control Register 2 are set to 00, the mode bits will revert to 00 and the ADC will return to no convert mode until a new conversion is initiated by the CPU. Setting the TMR bits to a code other than 00 causes the conversion to be repeated. Figure 14 is a flowchart, showing how the AD7877 operates in mode 10.

For master mode operation, the channels to be digitized are written to Sequencer Register 1. Master mode is then selected by writing 11 to the mode bits in Control Register 1. Conversion does not begin immediately, the AD7877 waits until the screen is touched before beginning the sequence of conversions. The ADC will then digitize the selected channels, and the results are written to the results registers. The AD7877 waits for the screen to be touched again, or for a timer event, before beginning another sequence of conversions. Figure 15 is a flowchart, showing how the AD7877 operates in mode 11.

ADC CHANNEL (CTRL REGISTER 1 BITS <10:7>)
The ADC channel is selected by bits 10:7 of Control Register 1 (CHADD3 - CHADD0). In addition, the SER/DFR bit, bit 11, selects between single ended and differential conversion. A complete list of channel addresses is given in Table 1, overleaf.

TIMER (CTRL REGISTER 2 BITS <1:0>)

The TMR bits in Control Register 2 allows the ADC to be programmed to perform a single conversion sequence, or to convert repetitively at intervals of 512 µs, 1.024 ms or 8.19 ms.

In slave mode the timer starts as soon as the conversion sequence is finished. In master mode, the timer starts at the end of a conversion sequence only if the screen remains touched. If the touch is released at any stage, then the timer stops, and the next time the screen is touched, a conversion sequence begins immediately.

TABLE 1. CODES FOR SELECTING INPUT CHANNEL AND NORMAL OR RATIOMETRIC CONVERSION

CHAN.	SER/DFR	CHADD(3:0)	ANALOG INPUT	X SWITCHES	Y SWITCHES	+REF	-REF
0	0	0 0 0 0	X+ (Y Position)	OFF	ON	Y+	Y-
1	0	0 0 0 1	Y+ (X Position)	ON	OFF	X+	X-
2	0	0 0 1 0	Y- (Z2)	X+ OFF, X- ON	Y+ ON, Y- OFF	Y+	X-
3	0	0 0 1 1	AUX1	OFF	OFF	VREF	GND
4	0	0 1 0 0	AUX2	OFF	OFF	VREF	GND
5	0	0 1 0 1	AUX3	OFF	OFF	VREF	GND
6	0	0 1 1 0	BAT1	OFF	OFF	VREF	GND
7	0	0 1 1 1	BAT2	OFF	OFF	VREF	GND
8	0	1 0 0 0	TEMP1	OFF	OFF	VREF	GND
9	0	1 0 0 1	TEMP2	OFF	OFF	VREF	GND
10	0	1 0 1 0	X+ (Z1)	X+ OFF, X- ON	Y+ ON, Y- OFF	Y+	X-
-	0	1 0 1 1	INVALID ADDRESS				
-	0	1 1 0 0	INVALID ADDRESS				
-	0	1 1 0 1	INVALID ADDRESS				
-	0	1 1 1 0	INVALID ADDRESS				
-	0	1 1 1 1	INVALID ADDRESS				
0	1	0 0 0 0	X+ (Y Position)	OFF	ON	VREF	GND
1	1	0 0 0 1	Y+ (X Position)	ON	OFF	VREF	GND
2	1	0 0 1 0	Y- (Z2)	X+ OFF, X- ON	Y+ ON, Y- OFF	VREF	GND
3	1	0 0 1 1	AUX1	OFF	OFF	VREF	GND
4	1	0 1 0 0	AUX2	OFF	OFF	VREF	GND
5	1	0 1 0 1	AUX3	OFF	OFF	VREF	GND
6	1	0 1 1 0	BAT1	OFF	OFF	VREF	GND
7	1	0 1 1 1	BAT2	OFF	OFF	VREF	GND
8	1	1 0 0 0	TEMP1	OFF	OFF	VREF	GND
9	1	1 0 0 1	TEMP2	OFF	OFF	VREF	GND
10	1	1 0 1 0	X+ (Z1)	X+ OFF, X- ON	Y+ ON, Y- OFF	VREF	GND
-	1	1 0 1 1	INVALID ADDRESS				
-	1	1 1 0 0	INVALID ADDRESS				
-	1	1 1 0 1	INVALID ADDRESS				
-	1	1 1 1 0	INVALID ADDRESS				
-	1	1 1 1 1	INVALID ADDRESS				

Notes

[1]For Mode 0 (single-channel) conversion, channel is selected by writing appropriate CHADD3-CHADD0 code to Control Register 1.

[2]For sequential channel conversion, channels to be converted are selected by setting bits corresponding to channel number in Sequencer Register 1 for slave mode sequencing or Sequencer Register 2 for master mode sequencing.

[3]For both single channel and sequential conversion, normal (single-ended) conversion is selected by clearing the SER/DFR bit in Control Register 1. Ratiometric (differential) conversion is selected by setting the SER/DFR bit.

TMR1	TMR0	Function
0	0	Convert only once
0	1	Every 1024 clocks (512 µs)
1	0	Every 2048 clocks (1.024ms)
1	1	Every 16384 clocks (8.19ms)

INT/EXT REFERENCE (CTRL REGISTER 2 BIT <2>)
If the REF bit in Control Register 2 is 0 (default value), the internal reference is selected. If any connection is made to V_{REF} while the internal reference is selected, for example to supply a reference to other circuits, it should be buffered. Note that, since the internal reference is 2.5V, it will only operate with supply voltages down to 2.7V. Below this an external reference should be used. If the REF bit is 1, the V_{REF} pin becomes an input and the internal reference is powered down. This overrides any setting of the PM bits with regard to the reference. An external reference may then be applied to the REF pin.

STOPACQ POLARITY (CTRL REGISTER 2 BIT <3>)
This bit should be set according to the polarity of the signal applied to the STOPACQ pin. If that signal is active high, i.e. no acquisitions should occur during the signal's high period, then the POL bit should be set to 1. If the signal is active low, then the POL bit should be 0. The default value for POL is 0.

FIRST CONVERSION DELAY (CTRL REG 2 BITS <5:4>)
The First Conversion Delay (FCD) bits in Control Register 2 program a delay of 500 ns, 128 µs, 1.024 ms or 8.19 ms before the first conversion, to allow the ADC time to power up. This delay also occurs before conversion of the X and Y co-ordinate channels, to allow extra time for screen settling, and after the last conversion in a sequence, to pre-charge $\overline{\text{PENIRQ}}$.

If the signal at STOP_ACQ is being monitored, and goes active during the FCD, it is ignored until after the FCD period.

FCD1	FCD0	Function
0	0	1 clock delay (500 ns)
0	1	256 clocks delay (128 µs)
1	0	2048 clocks delay (1.024 ms)
1	1	16384 clocks delay (8.19 ms)

POWER MANAGEMENT (CTRL REGISTER 2 BITS <7:6>)

The Power Management (PM) bits in Control Register 2 allow the power management features of the ADC to be programmed.

If the PM bits are 00, the ADC is powered down permanently. This overrides any setting of the mode bits in Control Register 1.

If the PM bits are 01, the ADC and the reference both power down when the ADC is not converting.

If the PM bits are 10, the ADC and reference are powered up continuously.

If the PM bits are 11, the ADC, but not the reference, powers down when the ADC is not converting.

PM1	PM0	Function
0	0	Power down continuously
0	1	Power down ADC and reference when ADC not converting (powers up with FCD at start of conversion)
1	0	Powered up continuously
1	1	Power down ADC when ADC not converting (powers up with FCD at start ofconversion)

ACQUISITION TIME (CTRL REGISTER 2 BITS <9:8>)
The ACQ bits in Control Register 2 allow the selection of acquisition times for the ADC of 2, 4, 8 or 16 µs.

ACQ1	ACQ0	Function
0	0	4 clock periods (2 µs)
0	1	8 clock periods (4 µs)
1	0	16 clock periods (8 µs)
1	1	32 clock periods (16 µs)

AVERAGING (CTRL REGISTER 2 BITS <11:10>)
Signals from touch screens can be extremely noisy. The AVG bits in Control Register 2 allow multiple conversions to be performed on each input channel and averaged to reduce noise. Either a single conversion may be selected (no averaging), or 4, 8, or 16 conversions may be averaged. Only the averaged result is written into the result register.

AVG1	AVG0	Function
0	0	ADC Performs 1 average per channel
0	1	ADC Performs 4 averages per channel
1	0	ADC Performs 8 averages per channel
1	1	ADC Performs 16 averages per channel

SEQUENCER REGISTERS
There are two sequencer registers on the AD7877. Sequencer Register 0 controls which measurements are performed during a slave mode sequence. Sequencer register 1 controls which measurements are performed during a master mode sequence.

To include a measurement in a slave mode or master mode sequence, the relevant bit must be set in Sequencer Register 0 or Sequencer Register 1. Setting bit 11 includes a measurement on ADC channel 0 in the sequence, which is the Y positional measurement. Setting bit 10 includes a measurement on ADC channel 1, and so on, through to bit 1 for channel 10. Refer to Table 1 overleaf for more details of channel settings. Bit 0 in both sequencer registers in not use. See also Detailed Register Descriptions section.

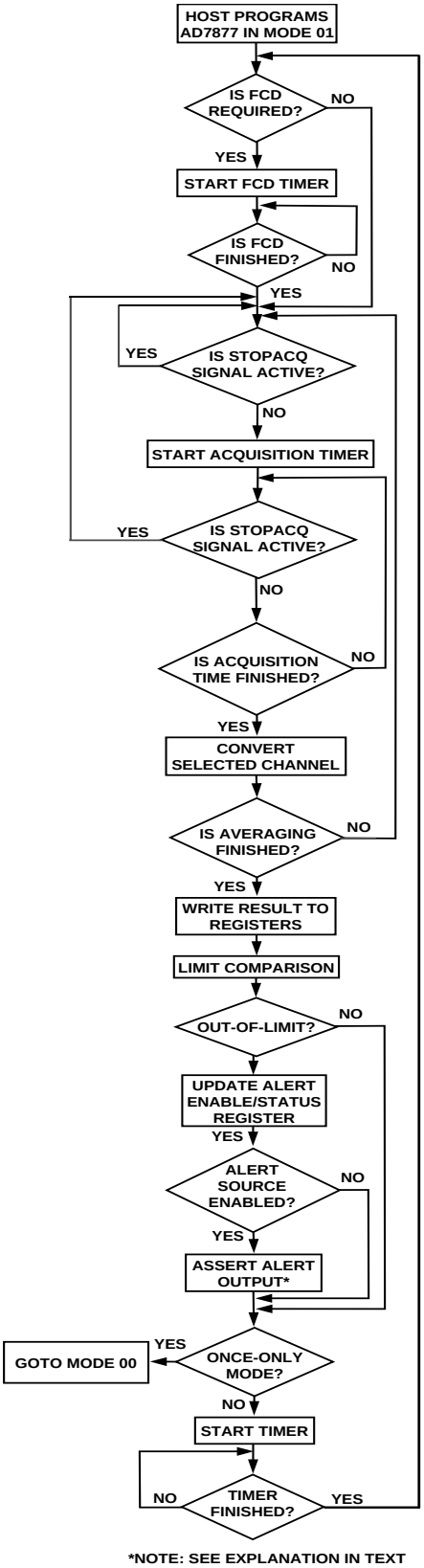


Figure 13. Flowchart for ADC Mode 01

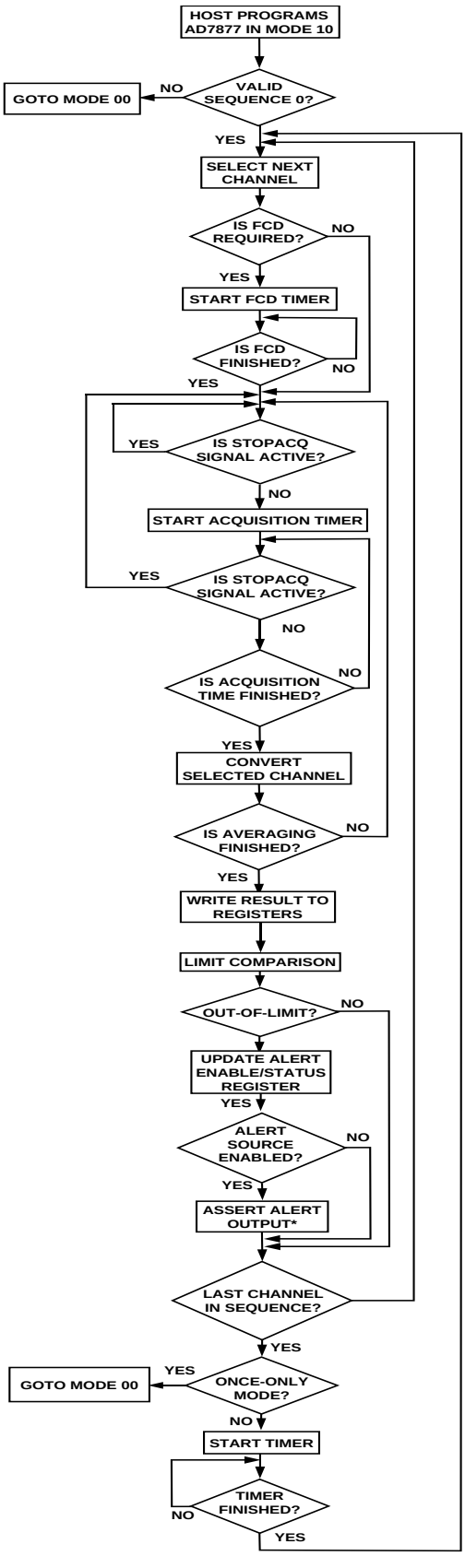


Figure 14. Flowchart for ADC Mode 10

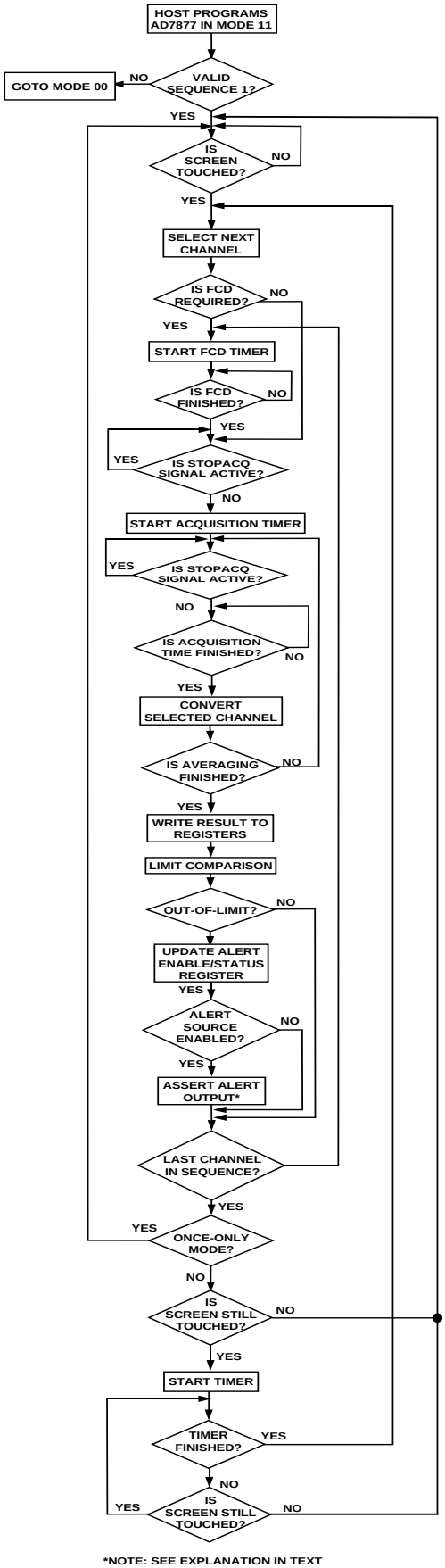


Figure 15. Flowchart for ADC Mode 11

DATA AVAILABLE OUTPUT ($\overline{DAV}$)

The Data Available output ($\overline{DAV}$) indicates that fresh ADC data is available in the results registers. While the ADC is idle, or is converting, $\overline{DAV}$ is high. Once the ADC has finished converting and new data is available in the results registers, $\overline{DAV}$ goes low. Taking $\overline{CS}$ low to read the registers resets $\overline{DAV}$ to a high condition. $\overline{DAV}$ is also reset if a new conversion is started by the AD7877, due to the timer expiring. The host should only attempt to read the results registers while $\overline{DAV}$ is low.

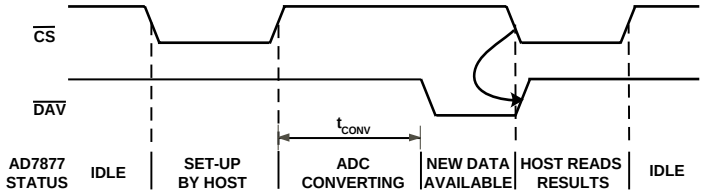


Figure 16. Operation of $\overline{DAV}$ Output

$\overline{DAV}$ is useful as a host interrupt in Master Mode. In this mode, the host can program the AD7877 to automatically perform a sequence of conversions, and can be interrupted by $\overline{DAV}$ at the end of each conversion sequence.

When the on-board timer is programmed to perform automatic conversions, a limited time is available to the host to read the results registers, before another sequence of conversion begins. The $\overline{DAV}$ signal is reset high when the timer expires, and the host should not access the results registers while $\overline{DAV}$ is high.

Figure 17 shows the worst case timings for reading the result registers after $\overline{DAV}$ has gone low. The timer is set at a minimum, and the conversion sequence includes all 11 possible ADC channels. t_1 is the time taken for acquisition and conversion on one ADC channel. t_2 shows the minimum timer delay, which is 1024 clock periods. t_3 is the time taken to read all 11 result registers. If the host wishes to read all 11 registers, then it must do so before the timer expires. t_4 shows the maximum time allowable between $\overline{DAV}$ going low, and the host beginning to read the results registers. If t_4 is exceeded, then all the registers cannot be read before the start of a new conversion, and incorrect data could be read by the host. This error situation should be avoided.

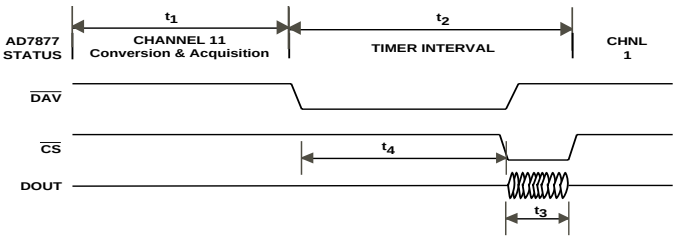


Figure 17. Timing for reads after DAV goes low

If f_{DCLK} = 20MHz (maximum), then t_{DCLK} = 50ns.

t_2= timer interval x t_{DCLK} = (1024 x 50ns) = 51.2µs.

T_{WRITE} = T_{READ} = 16 clk period x t_{DCLK} = 800ns

t_3= max time taken to write read address and read 11 registers = 800ns(write) + [800ns(read) x 11] = 9.6µs

t_{4MAX} = t_2 - t_3 = 51.2µs -9.6µs = 41.6µs

PEN INTERRUPT REQUEST ($\overline{\text{PENIRQ}}$)

The Pen Interrupt Request output ($\overline{\text{PENIRQ}}$) goes low whenever the screen is touched. The pen interrupt equivalent output circuitry is outlined in Figure 18. This is a digital logic output with an internal pullup resistor of 50kΩ, which means it does not need an external pullup. The $\overline{\text{PENIRQ}}$ output will always idle high.

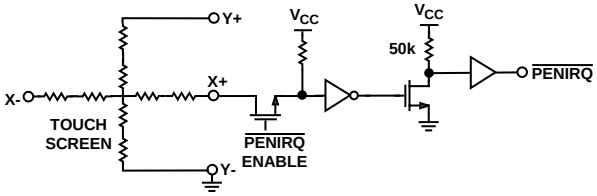


Figure 18. $\overline{\text{PENIRQ}}$ Output Equivalent Circuit

When the screen is touched $\overline{\text{PENIRQ}}$ will go low. This can be used to generate an interrupt request to the CPU.

When the screen touch ends, $\overline{\text{PENIRQ}}$ will go high immediately if the ADC is idle. If the ADC is converting, $\overline{\text{PENIRQ}}$ will go high when the ADC becomes idle. The $\overline{\text{PENIRQ}}$ operation for these two conditions is shown in figure 19.

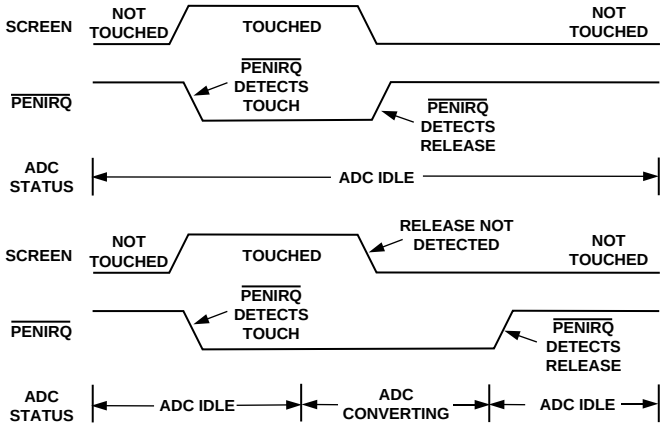


Figure 19. $\overline{\text{PENIRQ}}$ Operation For ADC Idle And ADC Converting

SYNCRONIZING THE AD7877 TO THE HOST CPU

There are two possible methods for syncronizing the AD7877 to its host CPU: Slave mode, where the mode bits may be either 01b or 10b, and Master mode, where the mode bits are 11b.

In slave mode, $\overline{\text{PENIRQ}}$ is used as an interrupt to the host. When $\overline{\text{PENIRQ}}$ goes low to indicate the screen has been touched, the host is woken up. It can then program the AD7877 to begin converting, in either mode 01b or 10b, and read the result registers after the conversions have completed.

In master mode, $\overline{\text{DAV}}$ is used as an interrupt to the host. The host should first initialise the AD7877 in mode 11b. The host can then go into sleep-mode, to conserve power. When the $\overline{\text{DAV}}$ signal goes low, the host can read the data available in the AD7877 result registers, and return to sleep-mode.

8-BIT DAC

The AD7877 features an on-chip 8-bit DAC, which can be used for LCD contrast control. The DAC can be configured for voltage output by clearing bit 2 of the DAC Register (address 1110b), or for current output by setting this bit.

The output voltage range can be set to 0 - $V_{CC}/2$ by clearing bit 0 of the DAC Register, or to 0 - V_{CC} by setting this bit. In current mode the output range is selectable by an external resistor, R_{RNG}, connected between the ARNG pin and GND. This sets the full-scale output current according to the following equation:

$I_{FS} = V_{CC}/(R_{RNG} \times 6)$

so $R_{RNG} = V_{CC}/(I_{FS} \times 6)$

Note that in current mode the DAC sinks current, i.e. positive current flows into ground.

The DAC is updated by writing to the DAC Register, address 1110b. The 8 MSBs of the data word are used for the DAC data.

The most effective way of controlling LCD contrast with the DAC is to use it to control the feedback loop of the DC-DC converter that supplies the LCD bias voltage, as shown in Figure 20. The bias voltage for graphic LCDs is typically in the range 20-25 volts and the DC-DC converter usually has a feedback loop that attenuates the output voltage and compares it with an internal reference voltage.

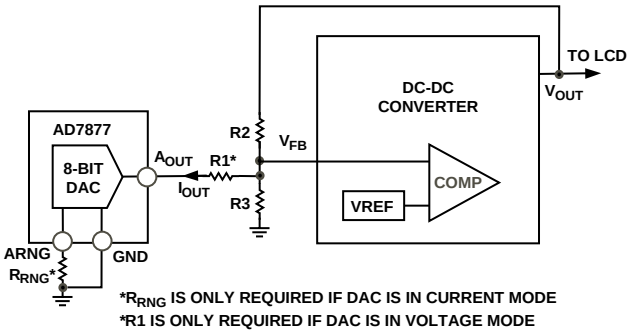


Figure 20. Using the DAC to Adjust LCD Contrast

The circuit operates as follows:

If the DAC is in current mode, when the DAC output is zero it will have no effect on the feedback loop. Irrespective of what the DAC does, the feedback loop maintains the voltage across R4, V_{FB}, equal to V_{REF}, and the output voltage V_{OUT} is: $V_{REF} \times (R2 + R3)/R3$.

As the DAC output is increased it will increase the feedback current, so the voltage across R2, and hence the output voltage, will also increase. (Note that the voltage across R3 does not change. This is important for calculation of the adjustment range).

In current mode it is quite easy to calculate the resistor values to give the required adjustment range in V_{OUT}.

1. Find out the maximum and minimum values of V_{OUT} required from the LCD manufacturer's data.
2. Decide on the current round the feedback loop, which for reasonable accuracy of the output voltage should be

at least 100 times the input bias current of the DC-DC converter's comparator.

3. Calculate R3 using the following:

   $R3 = V_{FB}/I_{FB} = V_{REF}/I_{FB}$

4. Calculate R2 for the minimum value of V_{OUT}, when the DAC has no effect.

   $R2 = R3(V_{OUT(MIN)} - V_{REF})/V_{REF}$.

5. Since the voltage across R3 does not change, subtract V_{REF} from V_{OUTMAX} and V_{OUTMIN} to get the maximum and minimum voltages across R2.

6. Calculate the change in feedback current between minimum and maximum out voltages using:

   $\Delta I = V_{R2(MAX)}/R2 - V_{R2(MIN)}/R2$

   This is the required full-scale current of the DAC

7. Calculate R_{RNG} from the equation given previously.

Example:

1. V_{CC} = 5V. $V_{OUT(MIN)}$ is 20 V and $V_{OUT(MAX)}$ is 25 V. V_{REF} is 1.25 V.
2. Allow 100 µA round the feedback loop.
3. R3 = 1.25 V/100 µA = 12.5 kΩ. Use nearest preferred value of 12 kΩ and recalculate feedback current as:

   I_{FB} = 1.25 V/12 kΩ = 104 µA

4. R2 = (20 V - 1.25 V)/104 µA = 180 kΩ
5. ΔI = 23.75 V/180 kΩ - 18.75 V/180 kΩ = 28 µA
6. R_{RNG} = 5 V/(6 × 28 µA) = 30 kΩ

In voltage mode, the circuit operation depends on whether the maximum output voltage of the DAC exceeds the DC-DC converter V_{REF}.

When the DAC output voltage is zero it will sink the maximum current through R1. The feedback current, and hence $V_{OUT,}$ will be at its maximum. As the DAC output voltage increases, the sink current and hence the feedback current will decrease, and V_{OUT} will fall. If the DAC output exceeds V_{REF}, it will start to source current, and V_{OUT} will have to further decrease to compensate. When the DAC output is at full-scale, V_{OUT} will be at its minimum.

Note that the effect of the DAC on V_{OUT} is opposite in voltage mode to that in current mode. In current mode, increasing DAC code increases the sink current, so V_{OUT} increases with increasing DAC code. In voltage mode, increasing DAC code increases the DAC output voltage, reducing the sink current.

To calculate the resistor values, proceed as follows:

1. Decide on the feedback current as before.
2. Calculate the parallel combination of R1 and R3 when the DAC output is zero.

   $R_P = V_{REF}/I_{FB}$

3. Calculate R2 as before but using R_P and V_{OUTMAX}.

   $R2 = R_P(V_{OUT(MAX)} - V_{REF})/V_{REF}$.

4. Calculate the change in feedback current between minimum and maximum out voltages using:

   $\Delta I = V_{R2(MAX)}/R2 - V_{R2(MIN)}/R2$

   as before.

   This is equal to the change in current through R1 between zero output and full-scale, which is also given by:

   ΔI = current at zero - current at full-scale

   $= V_{REF}/R1 - (V_{REF} - V_{FS})/R1$

   $= V_{FS}/R1$

5. $R1 = V_{FS}/\Delta I$
6. Calculate R3 from R1 and R_P using:

   $R3 = (R1 \times R_P)/(R1 - R_P)$

Example:

1. V_{CC} = 5V and $V_{FS} = V_{CC}$. $V_{OUT(MIN)}$ is 20 V and $V_{OUT(MAX)}$ is 25 V. V_{REF} is 1.25 V. Allow 100µA round the feedback loop, as before.
2. R_P = 1.25 V/100 µA = 12.5 kΩ.
3. R2 = 12.5 kΩ × (25 Ω - 1.25 Ω)/1.25 Ω = 237 kΩ.

   Use nearest preferred value of 240 kΩ.

4. ΔI = 25 V/240 kΩ - 20 V/240 kΩ = 21µA
5. R1 = 5 V/21µA = 238 kΩ

   Use nearest preferred value of 250 kΩ.

6. R3 = (180 kΩ × 12.5 kΩ)/(180 kΩ - 12.5 kΩ) =13.4 kΩ

   Use nearest preferred value of 13 kΩ.

The actual adjustment range using these values is 21V to 26 V.

AD7877 SERIAL INTERFACE

The AD7877 is controlled via a three wire Serial Peripheral Interface (SPI). This has a Data Input pin (DIN) for inputting data to the device, a Data Output pin (DOUT) for reading data back from the device, and a Data Clock pin (DCLK) for clocking data into and out of the device. A Chip Select Pin (CS) enables or disables the serial interface.

WRITING DATA

Data is written to the AD7877 in 16 bit words. The first four bits of the word are a register address, which tells the AD7877 which register to write to. The next 12 bits are data. How the AD7877 handles the data bits depends on the register address.

Register address 0000b is a dummy address which does nothing. Register addresses from 0010b to 1110b are 12-bit registers that perform various functions as described in the register map.

Register address 1111b is not a physical register but enables an extended writing mode that allows writing to the GPIO Configuration Registers.

When the register address is 1111b, the next four bits of the data word are the address of a GPIO configuration register and the 8 LSBs are the GPIO configuration data. Configuration of the GPIO pins is described in the section on General-Purpose I/O Pins.

Register address 0001b is a physical register, Control Register 1, but this is a special register. It contains data for setting up the ADC channel and operating mode, but bits 6 to 2 are the register address for reading. These define which register will be read back during the next read operation. Control Register 1 should be the last register in the AD7877 to be programmed, before starting a conversion.

The three different types of data word used for writing are shown in Figure 21.

WRITE TIMING

No serial interface operations can take place while $\overline{CS}$ is high. In order to write to the AD7877, $\overline{CS}$ must be taken low. To write to the device, a burst of 16 clock pulses is input to DCLK while the write data is input to DIN. Data is clocked in on the rising edge of DCLK. If multiple write operations are to be performed, $\overline{CS}$ must be taken high after the end of each write operation before another write operation can be performed, by taking $\overline{CS}$ low again.

READING DATA

Data is available on the DOUT pin whenever $\overline{CS}$ is low and the device is being clocked. Data is clocked out on the falling edge of DCLK.

After $\overline{CS}$ is taken low and the device is clocked, the AD7877 will output data from the register whose read address is currently stored in Control Register 1. Once this data has been output, the address will automatically increment and data will then be output from the next register, provided that a new read address is not written to Control Register 1. This will continue until $\overline{CS}$ is taken high. When $\overline{CS}$ is taken low again, reading will continue from the register whose read address is in Control Register 1, again provided that the write operation does not change the address. If the register read address reaches 11111b, it will then reset to zero. This feature allows all registers to be read out in sequence without having to explicitly write all their addresses to the device.

Note that since data words are 16-bits long, but the data registers are only 12 bits long, or 8 bits in the case of GPIO registers, the first four bits of a read back data word will be zeroes, or the first 8 bits in the case of a GPIO register.

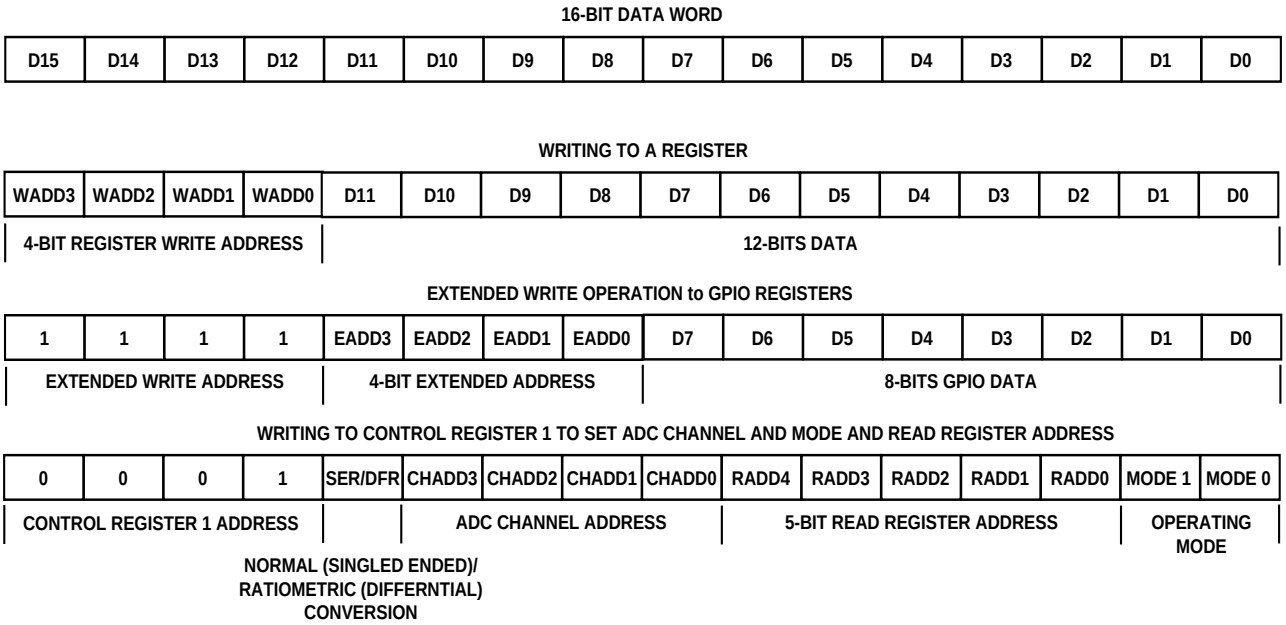
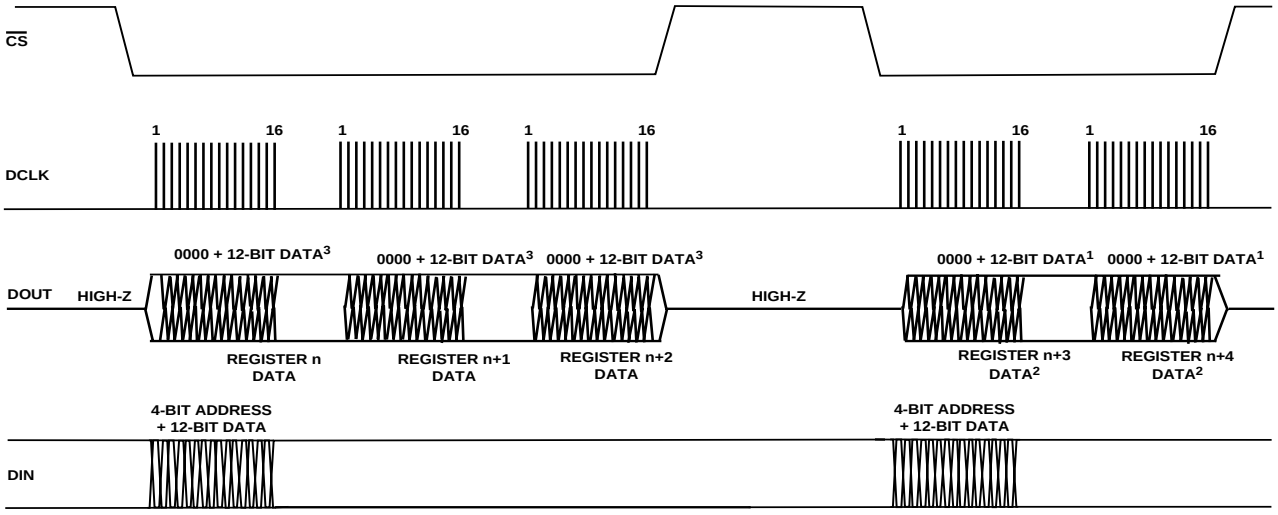


Figure 21. Designation of Data Word Bits in AD7877 Write Operations



NOTES:
1. DATA IS CLOCKED OUT ON THE FALLING EDGE OF DCLK.
2. INPUT DATA IS SAMPLED ON THE RISING EDGE OF DCLK.
3. FOR 8-BIT REGISTERS, 8 LEADING ZEROS PRECEDE 8 BITS OF DATA.
4. REGISTER READ ADDRESS INCREMENTS AUTOMATICALLY, PROVIDED A NEW ADDRESS IS NOT WRITTEN TO CONTROL REGISTER 1.

Figure 22. Overall Read/Write Timing

V_{DRIVE} PIN

The supply voltage to all the pins associated with the serial interface $\overline{DAV}$, DIN, DOUT, DCLK, $\overline{CS}$ $\overline{PENIRQ}$and $\overline{ALERT}$, is separate from the main V_{CC} supply and is connected to the V_{DRIVE} pin. This allows the AD7877 to be connected directly to processors whose supply voltage is less than the minimum operating voltage of the AD7877, in fact as low as 1.7V.

GENERAL-PURPOSE I/O PINS

The AD7877 has one dedicated general-purpose logic input output pin (GPIO 4), and any or all of the three auxiliary analog inputs can also be reconfigured as GPIOs.

Associated with the GPIOs are two 8-bit control registers and one 8-bit data register, which are accessed using the extended write mode.

As mentioned previously, GPIO registers are written to using the extended writing mode. The first four bits of the data word must be 1111b to access the extended writing map and the next four bits are the GPIO register address. This leaves 8 bits for the GPIO register data, so all GPIO registers are 8-bit. The GPIO control registers are located at extended writing map addresses 0000b and 0001b, and the GPIO data register is at address 0010b. GPIO registers are read in the same way as other registers, by writing a 5-bit address to Control Register 1. The GPIO registers are located at read addresses 11011b to 11101b.

GPIO CONFIGURATION

Each GPIO pin is configured by four bits in one of the GPIO control registers and has a data bit in the GPIO data register. See also Detailed Register Descriptions section. The GPIO configuration bits are explained in the next section, and in Table 2.

ENABLE - EN

These bits enable or disable the GPIO pins. When EN = 0, the corresponding GPIO pin is configured as the alternate function (AUX input). The other GPIO configuration bits have no effect if the particular GPIO is not enabled. When EN = 1, the pin is configured as a GPIO pin. GPIO4, which does not have an alternate function, does not have an EN bit; It is always enabled.

DIRECTION - DIR

These bits set the direction of the GPIO pins. When DIR = 0 the pin is an output. Setting or clearing the relevant bit in the GPIO data register will output a value on the corresponding GPIO pin. The output value depends on POL bit.

When DIR = 1 the pin is an input. An input value on the relevant GPIO pin will set or clear the corresponding bit in the GPIO data register, depending on the POL bit. A GPIO data register bit is read-only when DIR =1 for that GPIO.

POLARITY - POL

When POL = 0, the GPIO pin is active low. When POL =1, the GPIO pin is active high. How this bit affects the GPIO operation depends on the DIR bit also.

If POL =1 and DIR =1: A 1 at the input pin will set the corresponding GPIO data bit to 1. A 0 at the input pin will clear the corresponding GPIO data bit to 0.

If POL =1 and DIR =0: A 1 in the GPIO data register bit will put a 1 on the corresponding GPIO output pin. A 0 in the GPIO data register bit will put a 0 on the GPIO output pin.

ALERT ENABLE - ALEN

GPIOs can operate as interrupt sources to trigger the $\overline{\text{ALERT}}$ output. This is controlled by the Alert Enable, or ALEN bits, in the GPIO configuration registers. When ALEN =1, the corresponding GPIO can trigger an $\overline{\text{ALERT}}$. When ALEN =0, the corresponding GPIO cannot cause the $\overline{\text{ALERT}}$ output to assert.

$\overline{\text{ALERT}}$ is asserted low if any GPIO data register bit is set, when the GPIO is configured as an input. The GPIO data bit is set if a 1 appears on the GPIO input pin when POL =1, or if a 0 appears on the GPIO input pin when POL =0. It should be noted that $\overline{\text{ALERT}}$ is only triggered when the GPIO is configured as an input, i.e. when DIR =1. $\overline{\text{ALERT}}$ can never be triggered by a GPIO that is configured as an output, i.e. DIR =0.

$\overline{\text{ALERT}}$ OUTPUT

The ALERT pin is an alarm or interrupt output that will go low if any one of a number of interrupt sources is asserted. The results of limit comparisons on the AUX1, BAT1, BAT2 and TEMP1 channels are interrupt sources. An out-of-limit comparison will set a status bit in the AlertStatus/Mask Register (address 00011b). These interrupt sources can be masked out by clearing the corresponding enable bit in this register. There are separate status and enable bits for high and low limits, so it is possible to have, say, an over-temperature limit without having to program a low limit.

$\overline{\text{ALERT}}$ will also be asserted if an input on a GPIO pin sets a bit in the GPIO data register, as explained in the previous section. GPIO interrupts may be disabled by clearing the corresponding ALEN bit in the GPIO control registers.

The interrupt source may be identified by reading the GPIO data register and the Alert Status/Enable Register. $\overline{\text{ALERT}}$ will remain asserted until the source of the interrupt has been masked out or removed.

If the $\overline{\text{ALERT}}$ source is a GPIO, then masking out the interrupt by clearing the corresponding ALEN bit to 0, or removing the source of the interrupt on the GPIO pin, will cause ALERT to go high again.

If the $\overline{\text{ALERT}}$ source is an out-of-limit measurement, writing a 0 to the corresponding status bit in the Alert Status/Enable Register causes $\overline{\text{ALERT}}$ to go high. However, the status bit will be set to 1 again on the next measurement cycle if the measurement remains out of limit. The $\overline{\text{ALERT}}$ source can also be masked by clearing the relevant bit in the Alert Status/Enable register to 0.

GROUNDING AND LAYOUT

For information on grounding and layout considerations for the AD7877 refer to the 'Layout and Grounding Recommendations for Touch Screen Digitizers' Technical Note.

Table 2. GPIO Configuration

EN	DIR	POL	ALEN		DATA BIT	PIN VOLTAGE	ALERT
0	X	X	0		X	X	X
1	0	0	0		0	1	1
1	0	0	0		1	0	1
1	0	0	1		0	1	1
1	0	0	1		1	0	1
1	0	1	0		0	0	1
1	0	1	0		1	1	1
1	0	1	1		0	0	1
1	0	1	1		1	1	1
1	1	0	0		1	0	1
1	1	0	0		0	1	1
1	1	0	1		1	0	0
1	1	0	1		0	1	1
1	1	1	0		0	0	1
1	1	1	0		1	1	1
1	1	1	1		0	0	1
1	1	1	1		1	1	0

NOTES:
Shaded pin voltage values indicates that change in data register causes change in output voltage on pin.
Shaded data values indicates that change in input voltage on pin causes change in data register bit.

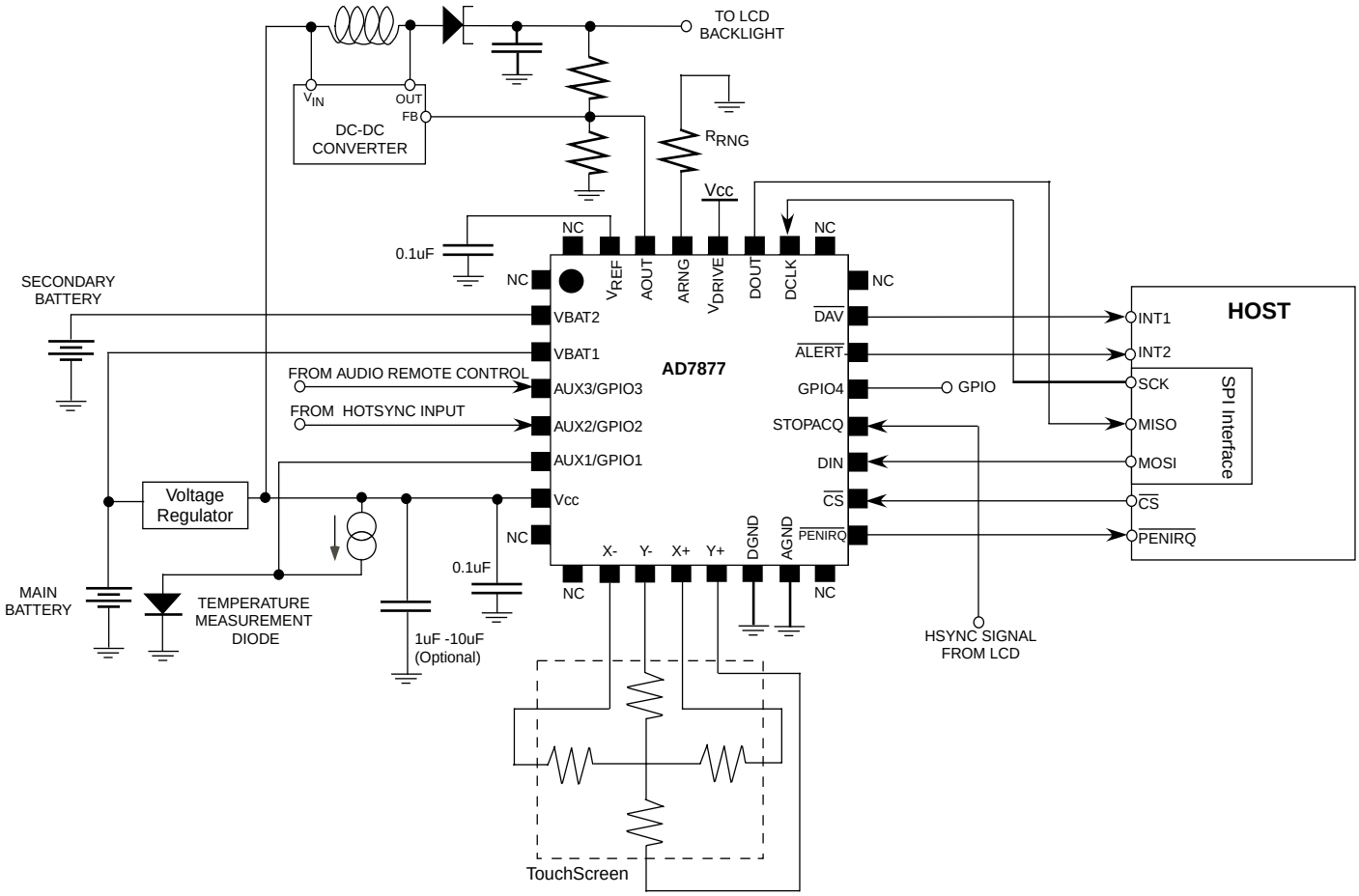


Figure 23. Typical Application Circuit

AD 7877 WRITE REGISTER MAP

REGISTER ADDRESS					REGISTER NAME	DESCRIPTION
(BINARY)				(HEX)		
WADD3	WADD2	WADD1	WADD0			
0	0	0	0	0	None	Unused. writing to this address has no effect.
0	0	0	1	1	Control Register 1	Contains ADC channel address, register read address and ADC mode.
0	0	1	0	2	Control Register 2	Contains ADC averaging, acquisition time, power management, first conversion delay, STOPACQ polarity, reference and timer settings.
0	0	1	1	3	Alert Status/Enable Register	Contains status of high/low limit comparisons for TEMP1, BAT1, BAT2 and AUX1, and enable bits to allow these channels to become interrupt sources.
0	1	0	0	4	AUX1 High Limit	User-programmable AUX1 upper limit.
0	1	0	1	5	AUX1 Low Limit	User-programmable AUX1 lower limit.
0	1	1	0	6	BAT1 High Limit	User-programmable BAT1 upper limit.
0	1	1	1	7	BAT1 Low Limit	User-programmable BAT1 lower limit.
1	0	0	0	8	BAT2 High Limit	User-programmable BAT2 upper limit.
1	0	0	1	9	BAT2 Low Limit	User-programmable BAT2 lower limit.
1	0	1	0	A	TEMP1 High Limit	User-programmable TEMP1 upper limit.
1	0	1	1	B	TEMP1 Low Limit	User-programmable TEMP1 lower limit.
1	1	0	0	C	Sequencer Register 0	Contains channel selection data for slave mode (software) sequencing.
1	1	0	1	D	Sequencer Register 1	Contains channel selection data for master mode (hardware) sequencing.
1	1	1	0	E	DAC Register	Contains DAC data and setup information
1	1	1	1	F	Extended Write	Not a physical register. Enables writing to extended write map.

EXTENDED WRITING MAP

REGISTER ADDRESS					REGISTER NAME	DESCRIPTION
(BINARY)				(HEX)		
EADD3	EADD2	EADD1	EADD0			
0	0	0	0	0	GPIO Control Register 1	Contains polarity, direction, enabling and interrupt enabling settings for GPIO1 and GPIO2.
0	0	0	1	1	GPIO Control Register 2	Contains polarity, direction, enabling and interrupt enabling settings for GPIO3 and GPIO4.
0	0	1	0	2	GPIO Data	Contains GPIO1 to GPIO4 data

AD7877 READ REGISTER MAP

REGISTER ADDRESS (BINARY)					(HEX)	REGISTER NAME	DESCRIPTION
RADD4	RADD3	RADD2	RADD1	RADD0			
0	0	0	0	0	00	None	Reads back all zeroes.
0	0	0	0	1	01	Control Register 1	See previous page.
0	0	0	1	0	02	Control Register 2	See previous page.
0	0	0	1	1	03	Alert Status/Enable Register	See previous page.
0	0	1	0	0	04	AUX1 High Limit	See previous page.
0	0	1	0	1	05	AUX1 Low Limit	See previous page.
0	0	1	1	0	06	BAT1 High Limit	See previous page.
0	0	1	1	1	07	BAT1 Low Limit	See previous page.
0	1	0	0	0	08	BAT2 High Limit	See previous page.
0	1	0	0	1	09	BAT2 Low Limit	See previous page.
0	1	0	1	0	0A	TEMP1 High Limit	See previous page.
0	1	0	1	1	0B	TEMP1 Low Limit	See previous page.
0	1	1	0	0	0C	Sequencer Register 0	See previous page.
0	1	1	0	1	0D	Sequencer Register 1	See previous page.
0	1	1	1	0	0E	DAC Register	See previous page.
0	1	1	1	1	0F	None	Factory use only.
1	0	0	0	0	10	X+	Measurement at X+ input for Y position.
1	0	0	0	1	11	Y+	Measurement at Y+ input for X position.
1	0	0	1	0	12	Y- (Z2)	Measurement at Y- input for touch pressure calculation.
1	0	0	1	1	13	AUX1	Auxiliary Input 1 measurement.
1	0	1	0	0	14	AUX2	Auxiliary Input 2 measurement.
1	0	1	0	1	15	AUX3	Auxiliary Input 3 measurement.
1	0	1	1	0	16	BAT1	Battery Input 1 measurement.
1	0	1	1	1	17	BAT2	Battery Input 1 measurement.
1	1	0	0	0	18	TEMP1	Single-ended temperature measurement.
1	1	0	0	1	19	TEMP2	Differential temperature measurement.
1	1	0	1	0	1A	X+ (Z1)	Measurement at X+ input for touch pressure calculation.
1	1	0	1	1	1B	GPIO Control Register 1	See previous page.
1	1	1	0	0	1C	GPIO Control Register 2	See previous page.
1	1	1	0	1	1D	GPIO Data Register	See previous page.
1	1	1	1	0	1E	None	Factory use only.
1	1	1	1	1	1F	None	Factory use only.

DETAILED REGISTER DESCRIPTIONS

Register Name: Control Register 1

Write Address: 0001 Read Address: 00001 Default Value: 000h Type: Read/Write

Bit	Name	Read/Write	Description
0	MODE0	R/W	LSB of ADC Mode code
1	MODE1	R/W	MSB of ADC Mode code 00 = No conversion 01 = Single conversion 10 = Conversion sequence (slave mode) 11 = Conversion sequence (master mode)
2	RD0	R/W	LSB of register read address. To read a register, its address must first be written to Control Register 1.
3	RD1	R/W	Bit 1 of register read address. To read a register, its address must first be written to Control Register 1.
4	RD2	R/W	Bit 2 of register read address. To read a register, its address must first be written to Control Register 1.
5	RD3	R/W	Bit 3 of register read address. To read a register, its address must first be written to Control Register 1.
6	RD4	R/W	MSB of register read address. To read a register, its address must first be written to Control Register 1.
7	CHADD0	R/W	LSB of ADC channel address.
8	CHADD1	R/W	Bit 1 of ADC channel address
9	CHADD2	R/W	Bit 2 of ADC channel address
10	CHADD3	R/W	MSB of ADC channel address 0000 = X+ input (Y position) 0001 = Y+ input (X position) 0010 = Y- (Z2) input (used for touch pressure calculation) 0011 = Auxiliary Input 1 (AUX1) 0100 = Auxiliary Input 2 (AUX2) 0101 = Auxiliary Input 3 (AUX3) 0110 = Battery Monitor Input 1 (BAT1) 0111 = Battery Monitor Input 2 (BAT2) 1000 = Temperature measurement 1, single conversion 1001 = Temperature measurement 2, for use in differential measurement method. 1010 = X+ (Z1) input (used for touch pressure calculation)
11	SER/DFR	R/W	Selects normal (single-ended) or ratiometric (differential) conversion 0 = ratiometric (differential) 1 = normal (single-ended)

Register Name: Control Register 2

Write Address: 0010 Read Address: 00010 Default Value: 000h

Bit	Name	Read/Write	Description
0	TMR0	R/W	LSB of conversion interval timer.
1	TMR1	R/W	MSB of conversion interval timer.
			00 = only convert once 01 = every 1024 clock periods (512 µs) 10 = every 2048 clock periods (1.024 ms) 11 = every 16384 clock periods (8.19 ms)
2	REF	R/W	Selects internal or external reference. 0 = internal reference 1 = external reference
3	POL	R/W	Indicates polarity of signal on STOPACQ pin. 0 = Active Low, 1 = Active High.
4	FCD0	R/W	LSB of first conversion delay.
5	FCD1	R/W	MSB of first conversion delay. This delay occurs before the first conversion after powering up the ADC, before converting the X and Y co-ordinate channels to allows settling, and after the last conversion to allow $\overline{\text{PENIRQ}}$ pre-charge. 00 = 1 clock period delay (500 ns) 01 = 256 clock periods delay (128 ms) 10 = 2048 clock periods delay (1.024 ms) 11 = 16384 clock periods delay (8.19 ms)
6	PM0	R/W	LSB of ADC power management code.
7	PM1	R/W	MSB of ADC power management code. 00 = ADC and reference powered down continuously 01 = ADC and reference* powered down when not converting 10 = ADC and reference* powered up continuously 11 = ADC powered down when not converting, reference* powered up. *Irrespective of PM bits, reference is always powered down if REF bit is 1.
8	ACQ0	R/W	LSB of ADC acquisition time.
9	ACQ1	R/W	MSB of ADC acquisition time. 00 = 4 clock periods (2 µs) 01 = 8 clock periods (4 µs) 10 = 16 clock periods (8 µs) 11 = 32 clock periods (16 µs)
10	AVG0	R/W	LSB of ADC averaging code.
11	AVG1	R/W	MSB of ADC averaging code. 00 = no averaging (1 conversion per channel) 01 = 4 measurements per channel averaged 10 = 8 measurements per channel averaged 11 = 16 measurements per channel averaged

Register Name: Alert Status/Enable register

Write Address: 0011 Read Address: 00011 Default Value: 000h

Bit	Name	Read/Write	Description
0	AUX1LO	R/W	When this bit is 1, the AUX1 channel is below the low limit
1	BAT1LO	R/W	When this bit is 1, the BAT1 channel is below the low limit
2	BAT2LO	R/W	When this bit is 1, the BAT2 channel is below the low limit
3	TEMP1LO	R/W	When this bit is 1, the TEMP1 channel is below the low limit
4	AUX1HI	R/W	When this bit is 1, the AUX1 channel is above the high limit
5	BAT1HI	R/W	When this bit is 1, the BAT1 channel is above the high limit
6	BAT2HI	R/W	When this bit is 1, the BAT2 channel is above the high limit
7	TEMP1HI	R/W	When this bit is 1, the TEMP1 channel is above the high limit
8	AUX1EN	R/W	Setting this bit enables AUX1 as an interrupt source to the $\overline{\text{ALERT}}$ output
9	BAT1EN	R/W	Setting this bit enables BAT1 as an interrupt source to the $\overline{\text{ALERT}}$ output
10	BAT2EN	R/W	Setting this bit enables BAT2 as an interrupt source to the $\overline{\text{ALERT}}$ output
11	TEMP1EN	R/W	Setting this bit enables TEMP1 as an interrupt source to the $\overline{\text{ALERT}}$ output

Register Name: AUX1 High Limit

Write Address: 0100 Read Address: 00100 Default Value: 000h Type: Read/Write

This register contains the 12-bit high limit for auxiliary input 1.

Register Name: AUX1 Low Limit

Write Address: 0101 Read Address: 00101 Default Value: 000h Type: Read/Write

This register contains the 12-bit low limit for auxiliary input 1.

Register Name: BAT1 High Limit

Write Address: 0110 Read Address: 00110 Default Value: 000h Type: Read/Write

This register contains the 12-bit high limit for battery monitoring input 1.

Register Name: BAT1 Low Limit

Write Address: 0111 Read Address: 00111 Default Value: 000h Type: Read/Write

This register contains the 12-bit low limit for battery monitoring input 1.

Register Name: BAT2 High Limit

Write Address: 1000 Read Address: 01000 Default Value: 000h Type: Read/Write

This register contains the 12-bit high limit for battery monitoring input 2.

Register Name: BAT2 Low Limit

Write Address: 1001 Read Address: 01001 Default Value: 000h Type: Read/Write

This register contains the 12-bit low limit for battery monitoring input 2.

Register Name: TEMP1 High Limit

Write Address: 1010 Read Address: 01010 Default Value: 000h Type: Read/Write

This register contains the 12-bit high limit for temperature measurement.

Register Name: TEMP1 Low Limit

Write Address: 1011 Read Address: 01011 Default Value: 000h Type: Read/Write

This register contains the 12-bit low limit for temperature measurement.

Register Name: Sequencer Register 0

Write Address: 1100 Read Address: 01100 Default Value: 000h

Bit	Name	Read/Write	Description
0	Not Used	R/W	This bit is not used.
1	Z1_SS	R/W	Setting this bit includes a touch pressure measurement (X+ input) in a slave mode sequence.
2	TEMP2_SS	R/W	Setting this bit includes a temperature measurement using differential conversion in a slave mode sequence.
3	TEMP1_SS	R/W	Setting this bit includes a temperature measurement using single-ended conversion in a slave mode sequence.
4	BAT2_SS	R/W	Setting this bit includes measurement of battery monitor input 2 in a slave mode sequence.
5	BAT1_SS	R/W	Setting this bit includes measurement of battery monitor input 1 in a slave mode sequence.
6	AUX3_SS	R/W	Setting this bit includes measurement of auxiliary input 3 in a slave mode sequence.
7	AUX2_SS	R/W	Setting this bit includes measurement of auxiliary input 2 in a slave mode sequence.
8	AUX1_SS	R/W	Setting this bit includes measurement of auxiliary input 1 in a slave mode sequence.
9	Z2_SS	R/W	Setting this bit includes a second touch pressure measurement (Y- input) in a slave mode sequence.
10	XPOS_SS	R/W	Setting this bit includes measurement of the X position (Y+ input) in a slave mode sequence.
11	YPOS_SS	R/W	Setting this bit includes measurement of the Y position (X+ input) in a slave mode sequence.

Register Name: Sequencer Register 1

Write Address: 1101 Read Address: 01101 Default Value: 000h

Bit	Name	Read/Write	Description
0	Not Used	R/W	This bit is not used.
1	Z1_MS	R/W	Setting this bit includes a touch pressure measurement (X+ input) in a master mode sequence.
2	TEMP2_MS	R/W	Setting this bit includes a temperature measurement using differential conversion in a master mode sequence.
3	TEMP1_MS	R/W	Setting this bit includes a temperature measurement using single-ended conversion in a master mode sequence.
4	BAT2_MS	R/W	Setting this bit includes measurement of battery monitor input 2 in a master mode sequence.
5	BAT1_MS	R/W	Setting this bit includes measurement of battery monitor input 1 in a master mode sequence.
6	AUX3_MS	R/W	Setting this bit includes measurement of auxiliary input 3 in a master mode sequence.
7	AUX2_MS	R/W	Setting this bit includes measurement of auxiliary input 2 in a master mode sequence.
8	AUX1_MS	R/W	Setting this bit includes measurement of auxiliary input 1 in a master mode sequence.
9	Z2_MS	R/W	Setting this bit includes a second touch pressure measurement (Y- input) in a master mode sequence.
10	XPOS_MS	R/W	Setting this bit includes measurement of the X position (Y+ input) in a master mode sequence.
11	YPOS_MS	R/W	Setting this bit includes measurement of the Y position (X+ input) in a master mode sequence.

Register Name: DAC Register

Write Address: 1110 Read Address: 01110 Default Value: 000h

Bit	Name	Read/Write	Description
0	RANGE	R/W	This bit sets the output range of the DAC in voltage mode. 0 = 0 to $V_{CC}/2$ 1 = 0 to V_{CC}
1	Not Used	R/W	This bit is not used.
2	V/I	R/W	This bit selects between voltage output and current output. 0 = Voltage 1 = Current
3	PD	R/W	This bit powers down the DAC. 0 = DAC on 1 = DAC powered down
4	DAC0		LSB of DAC data.
5	DAC1		Bit 1 of DAC data.
6	DAC2		Bit 2 of DAC data.
7	DAC3		Bit 3 of DAC data.
8	DAC4		Bit 4 of DAC data.
9	DAC5		Bit 5 of DAC data.
10	DAC6		Bit 6 of DAC data.
11	DAC7		MSB of DAC data.

Register Name: Y Position

Write Address: N/A Read Address: 10000 Default Value: 000h Type: Read Only

This register contains the 12-bit result of the measurement at the X+ input with Y layer excited (Y position measurement).

Register Name: X Position

Write Address: N/A Read Address: 10001 Default Value: 000h Type: Read Only

This register contains the 12-bit result of the measurement at the Y+ input with X layer excited (X position measurement).

Register Name: Z2

Write Address: N/A Read Address: 10010 Default Value: 000h Type: Read Only

This register contains the 12-bit result of the measurement at the Y- input with excitation voltage applied to Y+ and X- (used for touch pressure calculation).

Register Name: AUX1

Write Address: N/A Read Address: 10011 Default Value: 000h Type: Read Only

This register continues the 12-bit result of the measurement at Auxiliary Input 1.

Register Name: AUX2

Write Address: N/A Read Address: 10100 Default Value: 000h Type: Read Only

This register continues the 12-bit result of the measurement at Auxiliary Input 2.

Register Name: AUX3

Write Address: N/A Read Address: 10101 Default Value: 000h Type: Read Only

This register continues the 12-bit result of the measurement at Auxiliary Input 3.

Register Name: BAT1

Write Address: N/A Read Address: 10110 Default Value: 000h Type: Read Only

This register continues the 12-bit result of the measurement at Battery Monitor Input 1.

Register Name: BAT2

Write Address: N/A Read Address: 10111 Default Value: 000h Type: Read Only

This register continues the 12-bit result of the measurement at Battery Monitor Input 2.

Register Name: TEMP1

Write Address: N/A Read Address: 11000 Default Value: 000h Type: Read Only

This register continues the 12-bit result of a temperature measurement using single-ended conversion.

Register Name: TEMP2

Write Address: N/A Read Address: 11001 Default Value: 000h Type: Read Only

This register continues the 12-bit result of a temperature measurement using differential conversion.

Register Name: Z1

Write Address: N/A Read Address: 11010 Default Value: 000h Type: Read Only

This register continues the 12-bit result of a measurement at the X+ input with excitation voltage applied to Y+ and X- (used for touch pressure calculation).

GPIO REGISTERS

GPIO registers are written to using an extended 8-bit address. The first four bits of the data word are always 1111b to access the extended writing map. The next four bits are the register address. This leaves 8 bits for the GPIO data.

GPIO registers are read like all other registers, by writing a 5-bit address to Control Register 1, then reading DOUT.

Register Name: GPIO Control Register 1

Write Address: [1111] 0000 Read Address: 11011 Default Value: 000h

Bit	Name	Read/Write	Description
0	GPIO2_ALEN	R/W	If this bit is 1, GPIO2 is an interrupt source for the $\overline{\text{ALERT}}$ output. Clearing this bit masks out GPIO2 as an interrupt source for the $\overline{\text{ALERT}}$ output.
1	GPIO2_DIR	R/W	This bit sets the direction of GPIO2 (see notes). 0 = Output 1 = Input
2	GPIO2_POL	R/W	This bit determines if GPIO2 is active high or low (see notes). 0 = Active low 1 = Active high
3	GPIO2_EN	R/W	This bit selects the function of AUX2/GPIO2. 0 = AUX2 1 = GPIO2
4	GPIO1_ALEN	R/W	If this bit is 1, GPIO1 is an interrupt source for the $\overline{\text{ALERT}}$ output. Clearing this bit masks out GPIO1 as an interrupt source for the $\overline{\text{ALERT}}$ output.
5	GPIO1_DIR	R/W	This bit sets the direction of GPIO1 (see notes). 0 = Output 1 = Input
6	GPIO1_POL	R/W	This bit determines if GPIO1 is active high or low (see notes). 0 = Active low 1 = Active high
7	GPIO1_EN	R/W	This bit selects the function of AUX1/GPIO1. 0 = AUX1 1 = GPIO1

Register Name: GPIO Control Register 2

Write Address: [1111] 0001 Read Address: 11100 Default Value: 000h

Bit	Name	Read/Write	Description
0	GPIO4_ALEN	R/W	If this bit is 1, GPIO4 is an interrupt source for the ALERT output. Clearing this bit masks out GPIO3 as an interrupt source for the ALERT output.
1	GPIO4_DIR	R/W	This bit sets the direction of GPIO4 (see notes). 0 = Output 1 = Input
2	GPIO4_POL	R/W	This bit determines if GPIO4 is active high or low (see notes). 0 = Active low 1 = Active high
3	Not Used		This bit is not used.
4	GPIO3_ALEN	R/W	If this bit is 1, GPIO3 is an interrupt source for the ALERT output. Clearing this bit masks out GPIO4 as an interrupt source for the ALERT output.
5	GPIO3_DIR	R/W	This bit sets the direction of GPIO3(see notes). 0 = Output 1 = Input
6	GPIO3_POL	R/W	This bit determines if GPIO3 is active high or low (see notes). 0 = Active low 1 = Active high
7	GPIO3_EN	R/W	This bit selects the function of AUX3/GPIO3. 0 = AUX3 1 = GPIO3

Register Name: GPIO Data Register

Write Address: [1111] 0010 Read Address: 11101 Default Value: 000h

Bit	Name	Read/Write	Description
0	Not Used		This bit is not used.
1	Not Used		This bit is not used.
2	Not Used		This bit is not used.
3	Not Used		This bit is not used.
4	GPIO4_DAT	R/W	GPIO4 data bit.
5	GPIO3_DAT	R/W	GPIO3 data bit.
6	GPIO2_DAT	R/W	GPIO2 data bit.
7	GPIO1_DAT	R/W	GPIO1 data bit.

Notes:
See Table 2 in GPIO section for information on configuring the GPIOs.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

32 lead LFCSP
(CP-32)