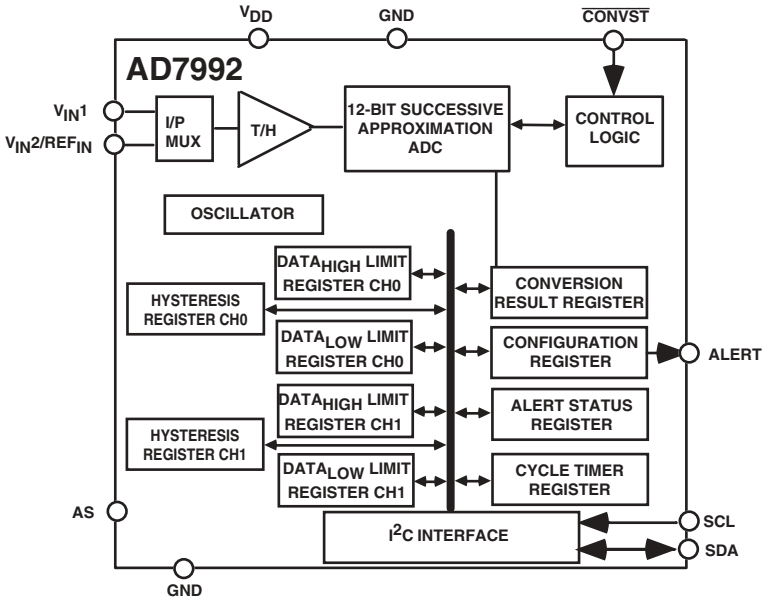
2 Channel, 12-Bit ADC with I²C Compatible Interface in 10-Lead MSOP

Preliminary Technical Data — AD7992

FEATURES

12-Bit ADC with Fast Conversion Time: 2 µs
Two Single-Ended Analog Input Channels
Specified for V_{DD} of 2.7 V to 5.5 V
Low Power Consumption
Fast Throughput Rate:- 188 KSPS
Sequencer Operation
Automatic Cycle Mode
I²C® Compatible Serial Interface
I²C® Interface supports:
Standard, Fast, and High-Speed Modes
Out of Range Indicator/ALERT Function
Pin-Selectable Addressing via AS
Two Versions Allow Five I²C Addresses
Shutdown Mode: 1µA max
10-Lead MSOP Package

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7992 is a 12-bit, high speed, low power, successive-approximation ADC. The part operates from a single 2.7 V to 5.5 V power supply and features a conversion time of 2 µs. The part contains a two channel multiplexer and track/hold amplifier which can handle input frequencies in excess of TBD kHz.

The AD7992 provides a two-wire serial interface which is compatible with I²C interfaces. The part comes in two versions, AD7992-0, and AD7992-1. Each version allows for a minimum of two different I²C addresses. The AD7992-0 supports Standard and Fast I²C interface Modes, while the AD7992-1 supports Standard, Fast, and two High-Speed I²C Interface Modes.

The AD7992 normally remains in a power-down state while not converting, powering up only to perform conversions. The conversion process can be controlled using the $\overline{\text{CONVST}}$ pin, an Automatic Conversion Cycle selected through software control, or a mode where conversions occur across read Address operations. The AD7992 uses advanced design techniques to achieve low power dissipation with a fast conversion time. There are no pipeline delays associated with the part.

The reference for the part is applied externally and can be in the range of 1.2V to V_{DD}. This allows the widest dynamic input range to the ADC.

On-chip registers can be programmed with high and low limits for the conversion result, and an open drain Out of Range Indicator output (ALERT), becomes active when the programmed high or low limits are violated. This output can be used as an interrupt.

PRODUCT HIGHLIGHTS

1. 2 µs Conversion time with low power consumption.
2. I²C Compatible Serial Interface with pin selectable addresses. Two AD7992 versions allow five AD7992 devices to be connected to the same serial bus.
3. The part features automatic shutdown while not converting to maximize power efficiency. Current consumption is 1µA max when in shutdown.
4. Reference can be driven up to the power supply.
5. Out of Range Indicator which can be software disabled/ enabled.
6. Oneshot and automatic conversion rates.
7. No Pipeline Delay
   The part features a standard successive-approximation ADC.

Part Number	No. of Bits	No. of Channels	Package
AD7998	12	8	20 TSSOP
AD7994	12	4	16 TSSOP
AD7997	10	8	20 TSSOP
AD7993	10	4	16 TSSOP

Table 1. Related Products

REV. PrF 04/03

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703 Analog Devices, Inc., 2002

AD7992–SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.5 V, unless otherwise noted ; REF_{IN} = 2.5 V; f_{SCL} = 3.4 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			F_{IN} = 10kHz Sine Wave
Signal to Noise + Distortion (SINAD)[2]	70	dB min	
Signal to Noise Ratio (SNR)[2]	71	dB min	
Total Harmonic Distortion (THD)[2]	-78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	-80	dB typ	
Intermodulation Distortion (IMD)[2]			fa = TBD kHz, fb = TBD kHz
Second Order Terms	-78	dB typ	
Third Order Terms	-78	dB typ	
Aperture Delay	10	ns max	
Aperture Jitter	10	ps typ	
Channel-to-Channel Isolation	TBD	dB typ	F_{IN} = TBD kHz
Full Power Bandwidth	TBD	kHz typ	@ 3 dB
	TBD	kHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[2]	±1	LSB max	
	±0.6	LSB typ	
Differential Nonlinearity[2]	+1.5/-0.9	LSB max	Guaranteed No Missed Codes to 12 Bits.
	±0.75	LSB typ	
Offset Error[2]	±1.5	LSB max	Single Channel Mode
Offset Error[2]	±1.5	LSB max	Dual Channel Mode
Offset Error Match[2]	±0.5	LSB max	
Gain Error[2]	±1.5	LSB max	Single Channel Mode
Gain Error[2]	±2	LSB max	Dual Channel Mode
Gain Error Match[2]	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to REF_{IN}	Volts	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage Range	1.2 to V_{DD}	V min/Vmax	
DC Leakage Current	±1	µA max	
Input Capacitance	TBD	pF max	
Input Impedance	TBD	kΩ typ	
LOGIC INPUTS (SDA, SCL)			
Input High Voltage, V_{INH}	0.7(V_{DD})	V min	
Input Low Voltage, V_{INL}	0.3(V_{DD})	V max	
Input Leakage Current, I_{IN}	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[2,3]	10	pF max	
Input Hysteresis, V_{HYST}	0.1(V_{DD})	V min	
LOGIC INPUTS ($\overline{CONVST}$)			
Input High Voltage, V_{INH}	2.4	V min	V_{DD} = 5V
	2.0	V min	V_{DD} = 3V
Input Low Voltage, V_{INL}	0.8	V max	V_{DD} = 5V
	0.4	V max	V_{DD} = 3V
Input Leakage Current, I_{IN}	± 1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS (OPEN DRAIN)			
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3mA
	0.6	V max	I_{SINK} = 6mA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[2,3]	TBD	pF max	
Output Coding	Straight (Natural) Binary		

AD7992–SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.5 V, unless otherwise noted ; REF_{IN} = 2.5 V; f_{SCL} = 3.4 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1]	Units	Test Conditions/Comments
CONVERSION RATE			See Interface Section
Conversion Time	2	µs typ	
Track/Hold Acquisition Time	TBD	ns max	Full-Scale step input
	TBD	ns max	Sine wave input <= 30 KHz
Throughput Rate	3.4	kSPS max	Standard mode 100 kHz
	13	kSPS max	Fast Mode 400 kHz
	79	kSPS max	High-Speed Mode 3.4 MHz
POWER REQUIREMENTS			
V_{DD}	2.7/5.5 V	min/max	
I_{DD}			Digital Inputs = 0 V or V_{DD}
Peak Current	TBD	µA max	Peak Current during conversion
Power Down Mode, Interface Inactive	0.2/0.6	µA max	V_{DD} = 3 / 5 V.
Interface Active	0.05/0.2	mA max	V_{DD} = 3 / 5 V. 400 kHz SCL
	0.3/0.8	mA max	V_{DD} = 3 / 5 V. 3.4 MHz SCL
Operating, Interface Inactive	0.2/0.8	mA max	V_{DD} = 3 / 5 V. 400 kHz SCL
	0.05/0.3	mA max	V_{DD} = 3 / 5 V. 3.4 MHz SCL
Interface Active	0.15/0.35	mA max	V_{DD} = 3 / 5 V. 400 kHz SCL
	0.6/1.4	mA max	V_{DD} = 3 / 5 V. 3.4 MHz SCL

NOTES
[1]Temperature ranges as follows: B Version: –40°C to +85°C.
[2]See Terminology.
[3]Sample tested @ +25°C to ensure compliance.
[4]See POWER VERSUS THROUGHPUT RATE section.
Specifications subject to change without notice.

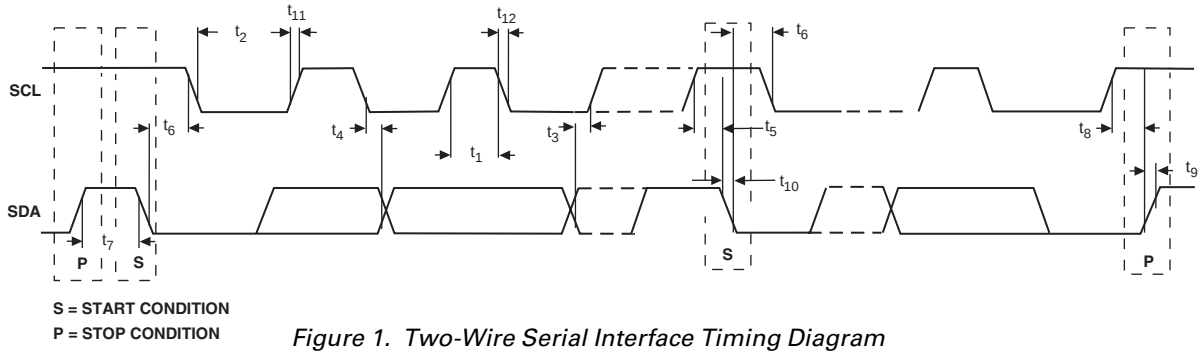


Figure 1. Two-Wire Serial Interface Timing Diagram

I²C TIMING SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.5 V, unless otherwise noted ; REF_{IN} = 2.5 V; unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. C_b refers to the Capacitive load on the bus line.)

Parameter	Conditions	AD7992 Limit at T_{MIN}, T_{MAX} MIN	MAX	Unit	Description
f_{SCL} [2]	Standard Mode		100	kHz	Serial Clock Frequency
	Fast Mode		400	kHz	
	High-Speed Mode, C_B = 100pF max		3.4	MHz	
	High-Speed Mode, C_B = 400pF max		1.7	MHz	
t_1	Standard Mode	4		µs	t_{HIGH}, SCL High Time
	Fast Mode	0.6		µs	
	High-Speed Mode, C_B = 100pF max	60		ns	
	High-Speed Mode, C_B = 400pF max	120		ns	
t_2	Standard Mode	4.7		µs	t_{LOW}, SCL Low Time
	Fast Mode	1.3		µs	
	High-Speed Mode, C_B = 100pF max	160		ns	
	High-Speed Mode, C_B = 400pF max	320		ns	
t_3	Standard Mode	250	-	ns	$t_{SU;DAT}$, Data Setup Time
	Fast Mode	100	-	ns	
	High-Speed Mode	10	-	ns	

I²C TIMING SPECIFICATIONS[1] (Continued.)

		AD7992 Limit at T_{MIN}, T_{MAX}			
Parameter	**Conditions**	**MIN**	**MAX**	**Unit**	**Description**
t_4	Standard Mode	0	3.45	µs	$t_{HD;DAT}$, Data Hold Time
	Fast Mode	0	0.9	µs	
	High-Speed Mode, C_B = 100pF max	0	70	ns	
	High-Speed Mode, C_B = 400pF max	0	150	ns	
t_5	Standard Mode	4.7		µs	$t_{SU;STA}$, Set-up Time for a repeated START Condition
	Fast Mode	0.6		µs	
	High-Speed Mode	160		ns	
t_6	Standard Mode	4		µs	$t_{HD;STA}$, Hold Time (repeated) START Condition
	Fast Mode	0.6		µs	
	High-Speed Mode	160		ns	
t_7	Standard Mode	4.7		µs	t_{BUF}, Bus Free Time Between a STOP and a START Condition.
	Fast Mode	1.3		µs	
t_8	Standard Mode	4		µs	$t_{SU;STO}$, Set-up Time for STOP Condition
	Fast Mode	0.6		µs	
	High-Speed Mode	160		ns	
t_9	Standard Mode	-	1000	ns	t_{RDA}, Rise time of SDA signal
	Fast Mode	20 + 0.1C_B	300	ns	
	High-Speed Mode, C_B = 100pF max	10	80	ns	
	High-Speed Mode, C_B = 400pF max	20	160	ns	
t_{10}	Standard Mode	-	300	ns	t_{FDA}, Fall time of SDA signal
	Fast Mode	20 + 0.1C_B	300	ns	
	High-Speed Mode, C_B = 100pF max	10	80	ns	
	High-Speed Mode, C_B = 400pF max	20	160	ns	
t_{11}	Standard Mode	-	1000	ns	t_{RCL}, Rise time of SCL signal
	Fast Mode	20 + 0.1C_B	300	ns	
	High-Speed Mode, C_B = 100pF max	10	40	ns	
	High-Speed Mode, C_B = 400pF max	20	80	ns	
t_{11A}	Standard Mode	-	1000	ns	t_{RCL1}, Rise time of SCL signal after a repeated START Condition and after an Acknowledge bit.
	Fast Mode	20 + 0.1C_B	300	ns	
	High-Speed Mode, C_B = 100pF max	10	80	ns	
	High-Speed Mode, C_B = 400pF max	20	160	ns	
t_{12}	Standard Mode	-	300	ns	t_{FCL}, Fall Time of SCL signal
	Fast Mode	20 + 0.1C_B	300	ns	
	High-Speed Mode, C_B = 100pF max	10	40	ns	
	High-Speed Mode, C_B = 400pF max	20	80	ns	
t_{SP}[4]	Fast Mode	0	50	ns	Pulsewidth of Spike Suppressed.
	High-Speed Mode	0	10	ns	
$t_{POWER-UP}$		1		µs	Power-up Time

NOTES

[1]See Figure 1. Hs-Mode timing specification apply to the AD7992-1 only, Standard, Fast Mode Timing specifications apply to both the AD7992-0 and AD7992-1. C_B refers tothe capacitance load on the bus line.

[2]The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on EMC behavior of the part.

[4]Input filtering on both the SCL and SDA inputs suppress noise spikes that are less than 50ns or 10ns for Fast Mode or High-Speed mode respectivley.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3 V to 7 V
Analog Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	-0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	–0.3 V to 7 V
Digital Output Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2]	±10 mA
Operating Temperature Range	
Commercial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
10-ld MSOP Package	
θ_{JA} Thermal Impedance	155 °C/W (MSOP)
θ_{JC} Thermal Impedance	40 °C/W (MSOP)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	+215°C
Infared (15 secs)	+220°C
ESD	TBD kV

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

ORDERING GUIDE

Model[1]	Range	Linearity Error[2](max)	Package Option[3]	Branding
AD7992BRM-0	-40°C to +85°C	±1 LSB	RM-10	C10
AD7992BRM-1	-40°C to +85°C	±1 LSB	RM-10	C11

NOTES
[1]The AD7992-0 supports Standard and Fast Mode I^2C. The AD7992-1 supports Standard, Fast and Hs-Mode I^2C.
[2]Linearity error here refers to integral nonlinearity
[3]RM = MSOP.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7992 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
1,2	AGND	Analog Ground. Ground reference point for all circuitry on the AD7992. All analog input signals should be referred to this GND voltage.
3	V_{DD}	Power Supply Input. The V_{DD} range for the AD7992 is from +2.7V to +5.5V.
4	$V_{IN}2/REF_{IN}$	Analog Input 2 / Voltage Reference Input. In single-channel mode, this pin becomes the reference voltage input, and an external reference should be applied at this pin. The external reference input range is 1.2V to V_{DD}. A 1 µF capacitor should be tied between this pin and AGND. If bit D6 is set to 1 in the Configuration Register the AD7992 will operate in single channel mode. In dual Channel mode, D6 in configuration register is 0, this pin provides the second analog input channel. The reference voltage for the AD7992 is taken from the power supply voltage in dual channel mode.
5	$V_{IN}1$	Analog Input 1. Single-ended analog input channel. The input range is 0V to REF_{IN}.
6	AS	Logic Input. Address Select input which selects one of three I^2C addresses for the AD7992 as shown in Table I.
7	$\overline{CONVST}$	Logic Input Signal. Convert Start Signal. This is an edge triggered logic input. The rising edge of this signal powers up the part. The power up time for the part is 1µs. The falling edge of $\overline{CONVST}$ places the track/hold into hold mode and initiates a conversion. A power up time of at least 1µs must be allowed for the $\overline{CONVST}$ high pulse, otherwise the conversion result will be invalid. (See Modes of Operation Section)
8	ALERT/BUSY	Digital Output, selectable as an ALERT or BUSY output function. When configured as an ALERT output, this pin acts as an Out of Range Indicator, and if enabled it becomes active when the conversion result violates the $DATA_{HIGH}$ or $DATA_{LOW}$ values. See Limit Registers section. When configured as a BUSY output, this pin becomes active when a conversion is in progress. Open-Drain Output. External pull-up resister required.
9	SDA	Digital I/O. Serial Bus Bi-directional Data. Open-drain output. External pull-up resistor required.
10	SCL	Digital Input. Serial Bus Clock. Open Drain. External pull-up resistor required.

AD7992 PIN CONFIGURATION MSOP

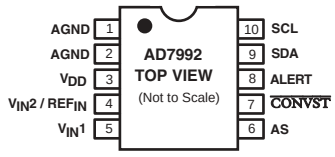


Table I. I^2C Address Selection

Part Number	AS Pin	I^2C Address
AD7992-0	GND	010 0001
AD7992-0	V_{DD}	010 0010
AD7992-1	GND	010 0011
AD7992-1	V_{DD}	010 0100
AD7992-X[1]	Float	010 0000

Note:-
[1] If the AS pin is left floating on any of the AD7992 parts the device address will be 010 0000. This will give each AD7992 device three different address options.

TERMINOLOGY

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise* + *Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 12-bit converter, this is 74 dB

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7992, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7992 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Channel-to-Channel Isolation

Channel-to-Channel Isolation is a measure of the level of crosstalk between channels. It is measured by applying a fullscale TBD kHz sine wave signal to the nonselected input channels and determining how much the TBD kHz signal is attenuated in the selected channel. This figure is given worse case across all channels

Aperture Delay

This is the measured interval between the leading edge of the sampling clock and the point at which the ADC actually takes the sample.

Aperture Jitter

This is the sample-to-sample variation in the effective point in time at which the sample is taken.

Full Power Bandwidth

The Full Power Bandwidth of an ADC is that input frequency at which the amplitude of the reconstructed Fundamental is reduced by 0.1 dB or 3 dB for a full-scale input

PSRR (Power Supply Rejection Ratio)

The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200 mV p-p sine wave applied to the ADC V_{DD} supply of frequency f_s.

PSRR (dB) = 10 *log (Pf/Pfs)*

Pf is the power at frequency f in the ADC output; *Pfs* is the power at frequency fs coupled onto the ADC V_{DD} supply.

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 1LSB

Offset Error Match

This is the difference in offset error between any two channels.

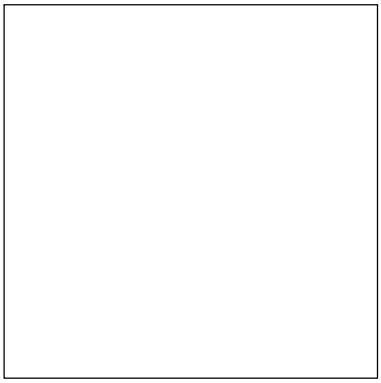
Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., REF_{IN} – 1 LSB) after the offset error has been adjusted out.

Gain Error Match

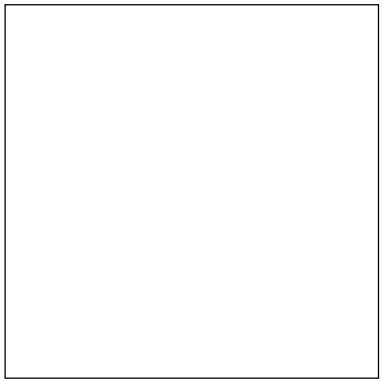
This is the difference in Gain error between any two channels.

AD7992 TYPICAL PERFORMANCE CURVES

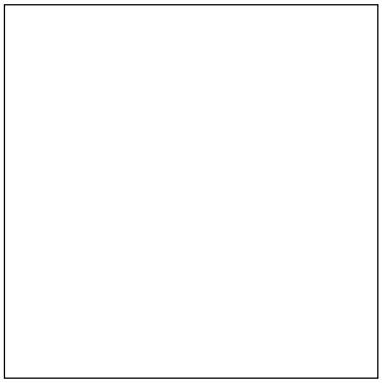
TPC 1 shows a typical FFT plot for the AD7992 at TBD kSPS sample rate and TBD kHz input frequency.



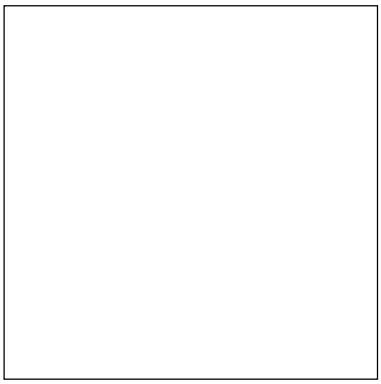
TPC 1. AD7992 Dynamic Performance at TBD ksps.



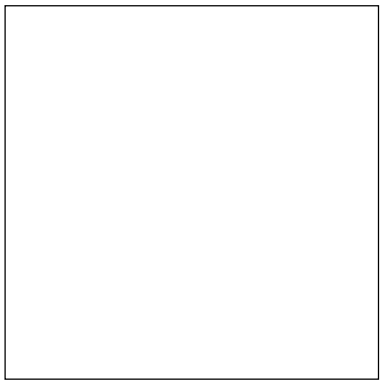
TPC 2. PSRR vs Supply Ripple Frequency.



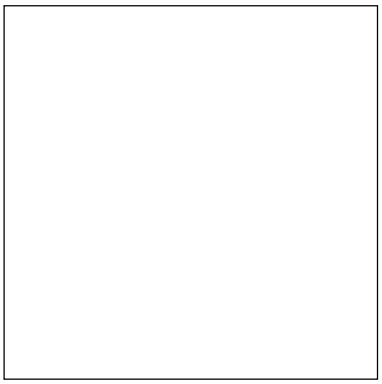
TPC 3. AD7992 SINAD vs Analog Input Frequency for Various Supply Voltages at TBD ksps.



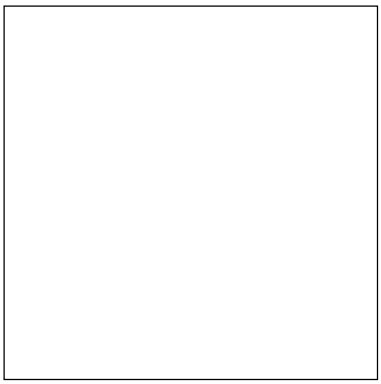
TPC 4. AD7992 Typical INL V_{DD} = 5V.



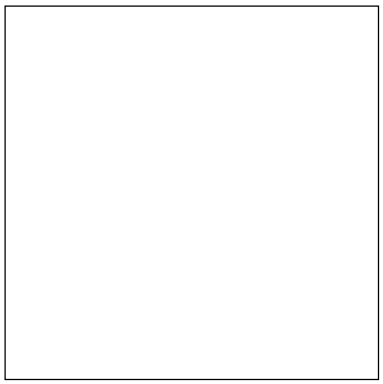
TPC 5. AD7992 Typical DNL V_{DD} = 5V.



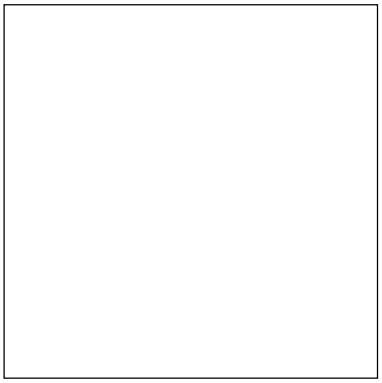
TPC 6. AD7992 Typical INL V_{DD} = 3V.



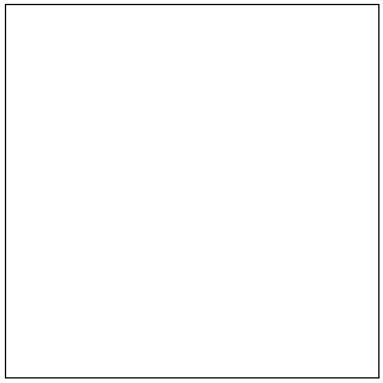
TPC 7. AD7992 Typical DNL V_{DD} = 3V.



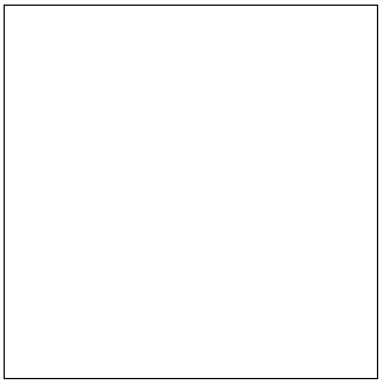
TPC 8. AD7992 Change in INLvs Reference Voltage V_{DD} = 5V.



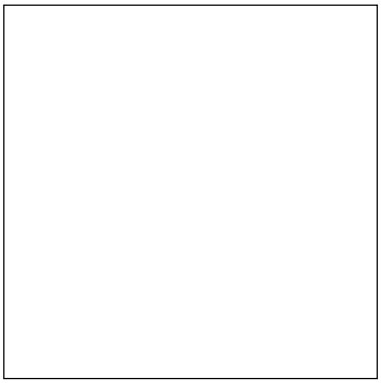
TPC 9. AD7992 Change in DNL vs Reference Voltage.



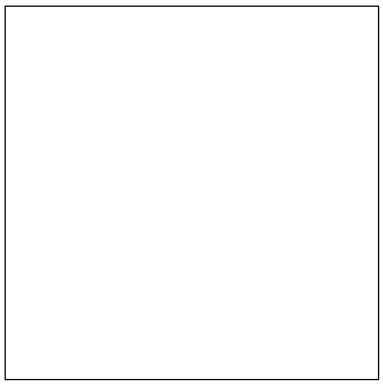
TPC 10. AD7992 Shutdown Current vs Supply Voltage, -40 , 25 and 85 °C.



TPC 11. AD7992 Supply Current vs I^2C Bus Rate for V_{DD} = 3V and 5V.



TPC 12. AD7992 Supply Current vs Supply Voltage for Various Temperatures.



TPC 13. AD7992 ENOB vs Reference Voltage, V_{DD} = 3V and V_{DD} = 5V.

CIRCUIT INFORMATION

The AD7992 is a fast, micro-power, 12-bit, single supply, 2 Channel A/D converter. The part can be operated from a 2.7 V to 5.5 V supply.

The AD7992 provides the user with a 2-channel multiplexer, an on-chip track/hold, A/D converter, an on-chip oscillator, internal data registers and an I^2C compatible serial interface, all housed in a 10-lead MSOP package, which offers the user considerable space saving advantages over alternative solutions. An external reference is required by the AD7992, and this reference can be in the range of 1.2 V to V_{DD}.

The AD7992 will normally remain in a shutdown state while not converting. When supplies are first applied the part will come up in a power-down state. Power-up is intitiated prior to a conversion and the device returns to power-down upon completion of the conversion. Conversions can be initiated on the AD7992 by either pulsing the $\overline{\text{CONVST}}$ signal, using an automatic cycling mode or using a mode where wake-up and conversion occur during the read function (see modes of Operation section). On completion of a conversion, the AD7992 will enter shutdown mode again. This automatic shutdown feature allows power saving between conversions. This means any read or write operations across the serial interface can occur while the device is in shutdown. The serial interface is I^2C compatible.

CONVERTER OPERATION

The AD7992 is a successive approximation analog-to - digital converter based around a charge redistribution DAC. Figures 2 and 3 show simplified schematics of the ADC. Figure 2 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

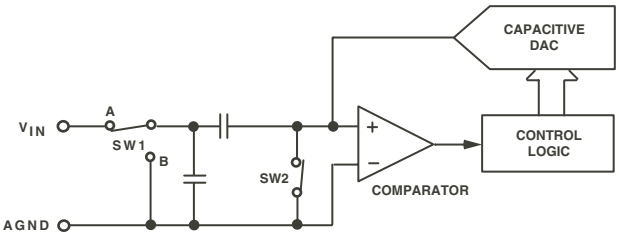


Figure 2. ADC Acquisition Phase

When the ADC starts a conversion, see Figure 3, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The Control Logic and the Charge Redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The Control Logic generates the ADC output code. Figure 4 shows the ADC transfer function.

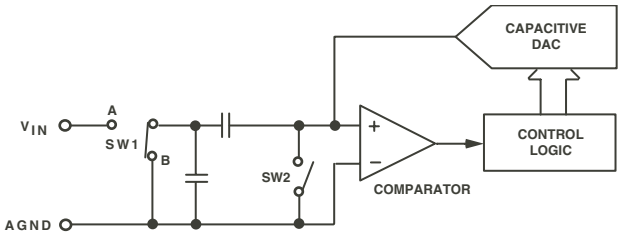


Figure 3. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7992 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1LSB, 2LSBs, etc.). The LSB size for the AD7992 is = $REF_{IN}/4096$. The ideal transfer characteristic for the AD7992 is shown in Figure 4 below.

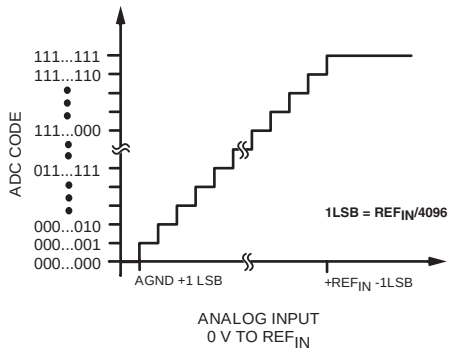


Figure 4. AD7992 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 5 shows the typical connection diagram for the AD7992. In Figure 5 the Address Select pin, AS, is tied to V_{DD}, however AS can also be either tied to GND or left floating, allowing the user to select up to three AD7992 devices on the same serial bus. An external reference must be applied to the AD7992. This reference can be in the range of 1.2 V to V_{DD}. A precision reference like the REF 19X family or the ADR421 can be used to supply the Reference Voltage to the ADC.

SDA and SCL form the two-wire I^2C/SMBus compatible interface. External Pull up resistors should be added to the SDA and SCL bus lines.

The AD7992-0 supports Standard and Fast I^2C Interface Modes. While the AD7992-1 supports Standard, Fast and Highspeed I^2C Interface Modes. Therefore if operating the AD7992 in either Standard or Fast Mode, five AD7992 (3 x AD7992-0 and 2 x AD7992-1 or 2 x AD7992-0 and 3 x AD7992-1) parts can be connected to the bus. When operating the AD7992 in Hs-Mode then up to three AD7992-1 can be connected to the bus.

Wake-up from power-down prior to a conversion is approximately 1µs while conversion time is approximately 2µs. The AD7992 enters power-down mode again after each conversion, this automatic powerdown feature will be useful in applications where power consumption is of concern.

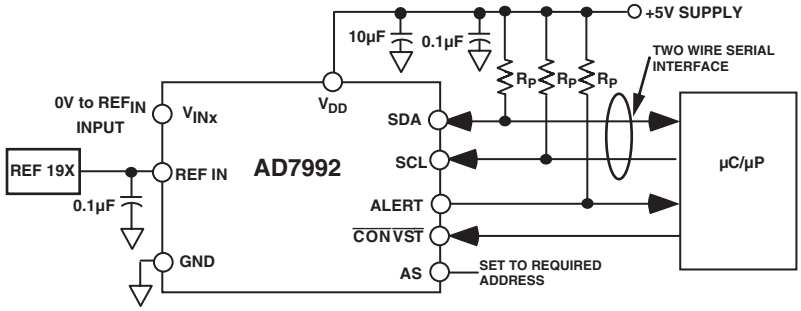


Figure 5 AD7992 Typical Connection Diagram

Analog Input

Figure 6 shows an equivalent circuit of the analog input sturcture of the AD7992. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300mV. This will cause these diodes to become forward biased and start conducting current into the substrate. 10 mA is the maximum current these diodes can conduct without causing irreversable damage to the part. The capacitor C1 in Figure 6 is typically about 4pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance (R_{ON}) of a switch (track and hold switch) and also includes the R_{ON} of the input multiplexer. This resistor is typically about 100Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 30 pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal to noise ratio are critical the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

When no amplifier is used to drive the analog input the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 7 shows a graph of the Total Harmonic Distortion vs. analog input signal frequency for different source impedances when using a supply voltage of 3V±10% and 5V ±10% and sampling at a rate of xkSPS. Figure 8 shows a graph of the total harmonic distortion versus analog input signal frequency for various supply voltages while sampling at xkSPS .

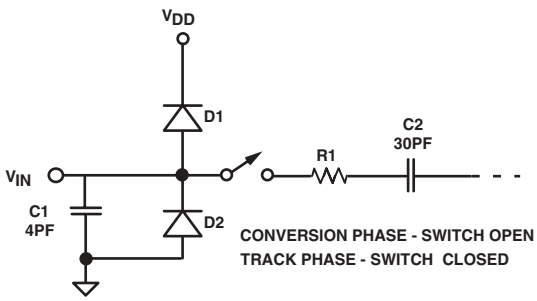


Figure 6. Equivalent Analog Input Circuit

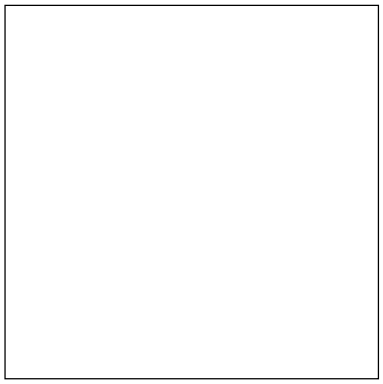


Figure 7. THD vs. Analog Input Frequency for Various Source Impedance for V_{DD}= 3V and 5V

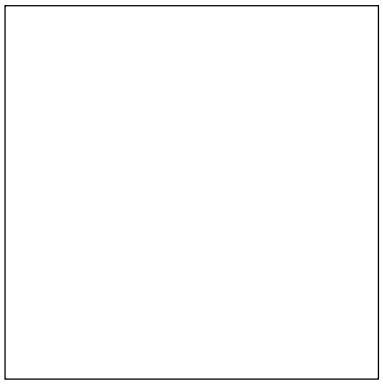


Figure 8. THD vs. Analog Input Frequency, Fs = xkSPS

INTERNAL REGISTER STRUCTURE

The AD7992 contains eleven internal registers, as shown in Figure 9, that are used to store conversion results, high and low conversion limits, and to configure and control the device. Ten are data registers and one is an address pointer register.

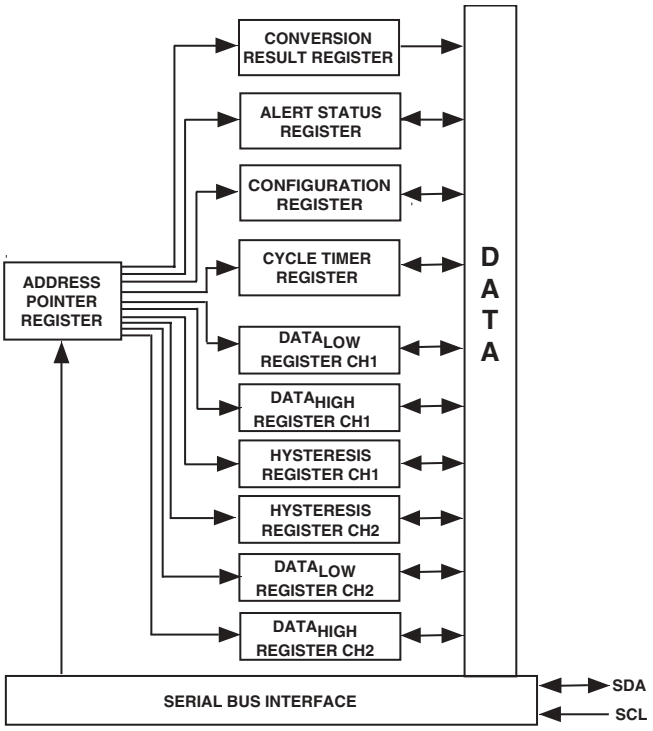


Figure 9. AD7992 Register Structure

Each data register has an address which is pointed to by the Address Pointer register when communicating with it. The Conversion Result Register is the only data register that is read only.

ADDRESS POINTER REGISTER

The Address Pointer register itself does not have, nor does it require, an address, as it is the register to which the first data byte of every Write operation is written automatically. The Address Pointer Register is an 8-bit register in which the four LSBs are used as pointer bits to store an address that points to one of the data registers of the AD7992, while the four MSBs are used as command bits when using Mode 2 (see Modes of Operation section). The first byte following each write address is the address of one of the data registers, which is stored in the Address Pointer Register, and selects the data register to which subsequent data bytes are written. Only the four LSBs of this register are used to select a data register. On Power up the Address Point register contains all 0's, therefore it is pointing to the Conversion Result Register.

Table II. Address Pointer Register

C4	C3	C2	C1	P3	P2	P1	P0
0	0	0	0	Register Select			

Table III. AD7992 Register Addresses

P3	P2	P1	P0	Registers
0	0	0	0	Conversion Result Register (Read)
0	0	0	1	Alert Status Register (Read/Write)
0	0	1	0	Configuration Register (Read/Write)
0	0	1	1	Cycle Timer Register (Read/Write)
0	1	0	0	$DATA_{LOW}$ Reg CH1 (Read/Write)
0	1	0	1	$DATA_{HIGH}$ Reg CH1 (Read/Write)
0	1	1	0	Hysteresis Reg CH1 (Read/Write)
0	1	1	1	$DATA_{LOW}$ Reg CH2 (Read/Write)
1	0	0	0	$DATA_{HIGH}$ Reg CH2 (Read/Write)
1	0	0	1	Hysteresis Reg CH2 (Read/Write)

CONFIGURATION REGISTER

The Configuration Register is an 8-bit read/write register that is used to set the operating modes of the AD7992. The MSB is used, and is a Don't Care bit. The bit functions are outlined in Table IV.

Table IV. Configuration Register Bit Function Description

D7	D6	D5	D4	D3	D2	D1	D0
DONTC	Single/Dual	CH2	CH1	FLTR	ALERT EN	BUSY/$\overline{ALERT}$	ALERT/BUSY POLARITY
0*	0*	0*	0*	1*	0*	0*	0*

*Default settings at Power-up

Bit	Mnemonic	Comment
D7	DONTCARE	
D6	Single/Dual	The value written to this bit determines the functionality of the $V_{IN}2/REF_{IN}$ pin. When this bit is 1 the pin takes on its Reference Input Function, REF_{IN}, making the AD7992 a single channel part. When this bit is a 0 the pin becomes a second analog input pin, $V_{IN}2$, making the AD7992 a Dual channel part..
D5, D4	CH2,CH1	These two channel address bits select which analog input channel is to be converted. A 1 in any of bits D5 or D4 selects a channel for conversion. If more than one channel bit is set this indicates that the alternating channel sequence is to be used. Table V shows how these two channel address bits are decoded. If D5 is selected the part will operate in Dual channel mode, with the Reference for the ADC being taken from the Supply voltage(D6 set to 0 for Dual channel mode).
D3	FLTR	The value written to this bit of the Control Register determines whether the filtering on SDA and SCL is enabled or to be bypassed. If this bit is a 1 then the the filtering is enabled, if it is a 0, then the filtering is bypassed.
D2	ALERT EN	The hardware ALERT function is enabled if this bit is set to 1 and disabled if set to 0. This bit is used in conjunction with the BUSY/ALERT bit to determine if the ALERT/BUSY pin will act as an ALERT or a BUSY function. (See Table VI.)
D1	BUSY/ALERT	This bit is used in conjunction with the ALERT EN bit to determine if the ALERT/BUSY output, pin 8, will act as an ALERT or BUSY function (see TABLE V1), or if pin 8 is configured as an ALERT output pin, if it is to be reset. When reading the Configuration registerD1 will always be a 0 when D2 is a 1.
D0	BUSY/ALERT POLARITY	This bit determines the active polarity of the ALERT/BUSY pin regardless of whether it is configured as an ALERT or BUSY output. It is active low if this bit is set to 0, and it is active high if set to 1.

Table V. Channel Selection

D5 CH2	D4 CH1	Analog Input Channel
0	0	No Conversion
0	1	Convert on $V_{IN}1$
1	0	Convert on $V_{IN}2$
1	1	Sequence between Channel 1 and Channel 2, beginning with Ch1

Table VI. ALERT/BUSY Function

D2	D1	ALERT/BUSY Pin Configuration
0	0	Pin does not provide any interrupt signal.
0	1	Pin configured as a BUSY output.
1	0	Pin configured as an ALERT output.
1	1	Resets ALERT output pin, Alert_Flag bit in Conversion Result Reg, and entire Alert Status Reg (if any active).

CONVERSION RESULT REGISTER

The Conversion Result Register is a 16-bit read-only register which stores the conversion reading from the ADC in Straight Binary format. A two Byte read operation is necessary to read data from this register. Table VIIa shows the contents of the first byte to be read while Table VIIb show the contents of the second byte to be read from AD7992.

Table VIIa. Conversion Value Register (First Read)

D15	D14	D13	D12	D11	D10	D9	D8
Alert_Flag	Zero	Zero	CH I.D.	MSB	B10	B9	B8

Table VIIb. Conversion Value Register (Second Read)

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

The AD7992 conversion result consists of an Alert_Flag bit, two leading zeros, a Channel Identifier bit and the 12 bit data result.

The Alert_Flag bit indicates whether the conversion result being read has violated a limit register associated with the channel. This is followed by two leading zeros and a Channel Indentifier bit indicating which channel the conversion result corresponds to. The 12-bit conversion result then follows MSB first.

LIMIT REGISTERS

The AD7992 has two pairs of limit registers, each to store high and low conversion limits for both analog input channels. Each pair of limit registers has an associated hysteresis register. All six registers are 16-bits wide, of which only the 12 LSBs of each are used. On power-up, the contents of the $DATA_{HIGH}$ register for each channel will be fullscale, while the contents of the $DATA_{LOW}$ registers will be zeroscale by default.

The Limit Registers can be used to monitor the conversion results on one or both channels. The AD7992 will signal an Alert (in either hardware or software or both depending on configuration) if the result moves outside the upper or lower limit set by the user.

$DATA_{HIGH}$ REGISTER CH1/CH2

The $DATA_{HIGH}$ Register for a channel is a 16-bit read/write register, of which only the 12 LSBs are used. The Register stores the upper limit that will activate the ALERT output and/or the Alert_Flag bit in the Conversion Result Register. If the value in the Conversion Result Register is greater than the value in the $DATA_{HIGH}$ Register, then the Alert_Flag bit is set to 1 and the ALERT pin is activated (the latter is true if ALERT is enabled in the Configuration Register). When the conversion result returns to a value at least N LSBs below the $DATA_{HIGH}$ Register value the ALERT output pin and Alert_Flag bit will be reset. The value of N is taken from the 12-bit Hysteresis register associated with that channel. The ALERT pin can also be reset by writing to bits D2,D1 in the Configuration Register.

Table VIIIa. $DATA_{HIGH}$ Register (First Read/Write)

D15	D14	D13	D12	D11	D10	D9	D8
Alert_Flag	0	0	0	B11	B10	B9	B8

Table VIIIb. $DATA_{HIGH}$ Register (Second Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

$DATA_{LOW}$ REGISTER CH0/CH1

The $DATA_{LOW}$ Register for a channel is a 16-bit read/write register, of which only the 12 LSBs are used. The Register stores the lower limit that will activate the ALERT output and/or the Alert_Flag bit in the conversion result register. If the value in the Conversion Result Register is less than the value in the $DATA_{LOW}$ Register, then the Alert_Flag bit is set to 1 and the ALERT pin is activated (the latter is true if ALERT is enabled in the Configuration Register). When the Conversion result returns to a value at least N LSBs above the $DATA_{LOW}$ Register value the ALERT ouput pin and Alert_Flag bit will be reset. The value of N is taken from the 12-bit Hysteresis register associated with that channel. The ALERT pin can also be reset by writing to bit D2,D1 in the Configuration Register.

Table IXa. $DATA_{LOW}$ Register (First Read/Write)

D15	D14	D13	D12	D11	D10	D9	D8
Alert_Flag	0	0	0	B11	B10	B9	B8

Table IXb. $DATA_{LOW}$ Register (Second Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

HYSTERESIS REGISTER (CH1/CH2)

The Hysteresis Register is a 16-bit read/write register, of which only the 12 LSBs of the Register are used. The Register stores the hysteresis value, N when using the limit registers. Each pair of Limit registers has a dedicated hysteresis register. The hysteresis value determines the reset point for the ALERT pin/Alert_Flag if a violation of the limits has occurred. If a hysteresis value of say 8 LSBs is required on the upper and lower limits of channel 1 then the 12 bit word, 0000 0000 0000 1000, should be written to Hysteresis Register CH1, the address of which is shown in Table III. On power up, the Hysteresis Registers will contain a value of 8 LSBs. If a different hysteresis value is required then that value must be written to the Hysteresis Register for the channel in question.

Table Xa. Hysteresis Register (First Read/Write)

D15	D14	D13	D12	D11	D10	D9	D8
Alert_Flag	0	0	0	B11	B10	B9	B8

Table Xb. Hysteresis Register (Second Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

Using the Limit Registers to Store Min/Max Conversion Results

If fullscale, i.e. all 1s, are written to the Hysteresis register for a channel then the $DATA_{HIGH}$ and $DATA_{LOW}$ Registers for that channel will no longer act as Limit registers as previously described, but instead they will act as storage registers for the maximum and minimum conversion results returned from conversions on a channel over any given period of time. This function is useful in applications where the widest span of actual conversion results is required rather than using the ALERT to signal an intervention is necessary, e.g. monitoring temperature extremes during refrigerated goods transportation.

It must be noted that on power-up, the contents of the $DATA_{HIGH}$ register for each channel will be fullscale, while the contents of the $DATA_{LOW}$ registers will be zeroscale by default so minimum and maximum conversion values being stored in this way will be lost if power is removed or cycled.

When using the limit registers to store the min and max conversion results, the Alert_Flag bit in the limit registers, D15, is used to indicate that an alert has happened on the other Input channel. If the Alert_Flag bit is set to 1, it will be reset when the Conversion result returns to a value at least N LSBs above the $DATA_{LOW}$ Register value or below the $DATA_{HIGH}$ Register value or if bits D2 and D1 of the Configuration Register are set to 1.

ALERT STATUS REGISTER

The Alert Status Register is a 8-bit read/write register, of which only the four LSBs are used. This register provides information on an Alert event. If a conversion results in activating the ALERT pin or the Alert_Flag bit in the Conversion Result Register, as described in the Limit Registers section, then the Alert Status Register may be read to gain further information. It contains 2 status bits per channel, one corresponding to the $DATA_{HIGH}$ limit and the other to the $DATA_{LOW}$ limit. Whichever bit has a status of 1 will show where the violation occured, i.e. on which channel and whether on upper or lower limit. If a second alert event occurs on the other channel between receiving the first alert and interrogating the Alert Status register then the corresponding bit for that Alert event will be set also.

The entire contents of the Alert Status register may be cleared by writing 1,1, to bits D2 and D1 in the Configuration register as shown in Table VI. This may also be acheived by 'writing' all 1's to the Alert Status Register itself. This means that if the Alert Status Register is addressed for a write which is all 1's, then the contents of the Alert Status Register will then be cleared or resest to all 0's. Alternatively, an individual active Alert bit(s) may be reset within the Alert Status Register by performing a write of '1' to that bit alone. The advantage of this is that once an Alert event has been serviced, that particular bit can be reset, e.g. $CH1_{LO}$, without clearing the entire contents of the Alert Status Register, thus preserving the status of any additional Alert, e.g. $CH2_{HI}$, which has occured while servicing the first. If it is not necessary to clear an Alert directly after servicing then obviously the Alert Status register may be read again immediately to look for any new Alerts, bearing in mind that the one just serviced will still be active.

Table XIa. Alert Status Register

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	$CH2_{HI}$	$CH2_{LO}$	$CH1_{HI}$	$CH1_{LO}$

Table XIb. Alert Status Register Bit Function Description

Bit	Mnemonic	Comment
D0	$CH1_{LO}$	Violation of $DATA_{LOW}$ limit on Channel 1 if this bit set to 1, no violation if 0.
D1	$CH1_{HI}$	Violation of $DATA_{HIGH}$ limit on Chan nel 1 if this bit set to 1, no violation if 0.
D2	$CH2_{LO}$	Violation of $DATA_{LOW}$ limit on Channel 2 if this bit set to 1, no violation if 0.
D3	$CH2_{HI}$	Violation of $DATA_{HIGH}$ limit on Chan nel 2 if this bit set to 1, no violation if 0.

CYCLE TIMER REGISTER

The Cycle Timer Register is a 8-bit read/write register, which stores the conversion interval value for the Automatic Cycle mode of the AD7992, see Modes of Operation section. Bits D3 - D5 of the Cycle Timer Register are unused and should contain 0's at all times. On power up, the Cycle Timer Register will contain all 0s, thus disabling the Automatic Cycle operation of the AD7992. To enable the Automatic Cycle Mode the user must write to the Cycle Timer Register, selecting the required conversion interval. Table XIIa shows the structure of the Cycle Timer register while Table XIIb shows how the bits in this register are decoded to provide various automatic sampling intervals.

Table XIIa. Cycle Timer Register

D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0	0	0	0*	0*	0*

Table XIIb. Cycle Timer Intervals

CYC Reg Value(D2,D1,D0)	Conversion Interval
000	Mode not selected
001	64 µs
010	128 µs
011	256 µs
100	512 µs
101	1.024 ms
110	2.048 ms
111	4.096 ms

It is recommended that no I^2C Bus activity occurs when a conversion is taking place. However if this is not possible, e.g. when operating in Mode 2, then in order to maintain the performance of the ADC, Bits D7 and D6 in the cycle timer register are used to delay critical sample intervals and bit trials from occurring while there is activity on the I^2C Bus. This may have the effect of increasing the Conversion time. When bits D7 and D6 are both 0, the bit trial and sample interval delaying mechanism will be implemented. The default setting of D7 and D6 is 0. However if bit trial delays extend longer than 1 µs the conversion will terminate. When D7 is 0 the Sampling instant delay will be implemented. When D6 is 0 the bit trial delay will be implemented. To turn off both set D7 and D6 to 1.

SERIAL INTERFACE

Control of the AD7992 is carried out via the I²C-compatible serial bus. The AD7992 is connected to this bus as a slave device, under the control of a master device, e.g. the processor.

SERIAL BUS ADDRESS

Like all I²C-compatible devices, the AD7992 has a 7-bit serial address. The three MSBs of this address for the AD7992 are set to 010. The AD7992 comes in two versions, the AD7992-0 to AD7992-1. The two versions have three different I²C addresses available which are selected by either tying the Address Select pin, AS, to GND, to V_{DD} or letting the pin float (see Table I). By giving different addresses for the two versions, up to five AD7992 devices can be connected to a single serial bus, or the addresses can be set to avoid conflicts with other devices on the bus.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA whilst the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit address (MSB first) plus a R/$\overline{W}$ bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device.

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle whilst the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0 then the master will write to the slave device. If the R/$\overline{W}$ bit is a 1 the master will read from the slave device.

2. Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge Bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will pull the data line high during the low period before the 9th clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

WRITING TO THE AD7992

Depending on the register being written to, there are two different writes for the AD7992.

Writing to the Address Pointer Register for a Subsequent Read

In order to read from a particular register, the Address Pointer register must first contain the address of that register. If it does not, the correct address must be written to the Address pointer register by performing a single-byte write operation, as shown in Figure 10. The write operation consists of the serial bus address followed by the address pointer byte. No data is written to any of the data registers. A read operation is subsequently performed to read the register of interest.

Writing a Single Byte of Data to the Configuration Register or Cycle Register

The Configuration Register and Cycle Register are both 8-bit registers, so only one byte of data can be written to each. Writing a single byte of data to one of these registers consists of the serial bus address, the chosen data register address written to the Address Pointer Register, followed by the data byte written to the selected data register. This is illustrated in Figure 11.

Writing a Single Byte of Data to a Limit Register

Each of the four Limit Registers are 12-bit registers, so two bytes of data are required to write a value to any one of them. Writing two bytes of data to one of these registers consists of the serial bus address, the chosen Limit Register address written to the Address Pointer Register, followed by two data bytes written to the selected data register. This is illustrated in Figure 12.

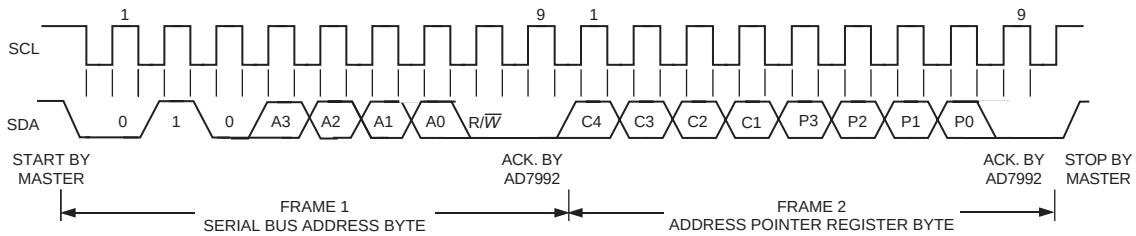


Figure 10. Writing to the Address Pointer Register to select a register for a subsequent Read operation

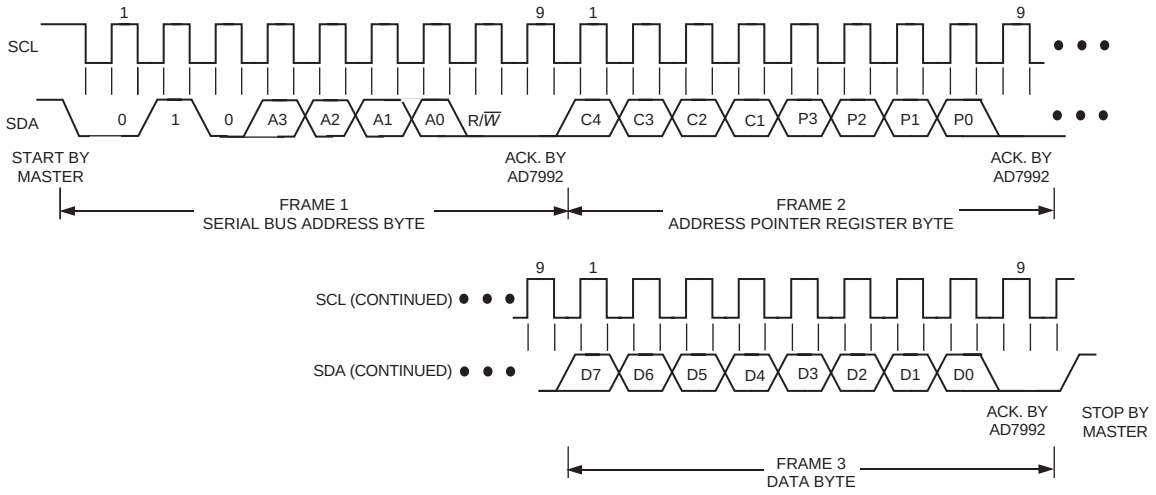


Figure 11. Single Byte Write Sequence

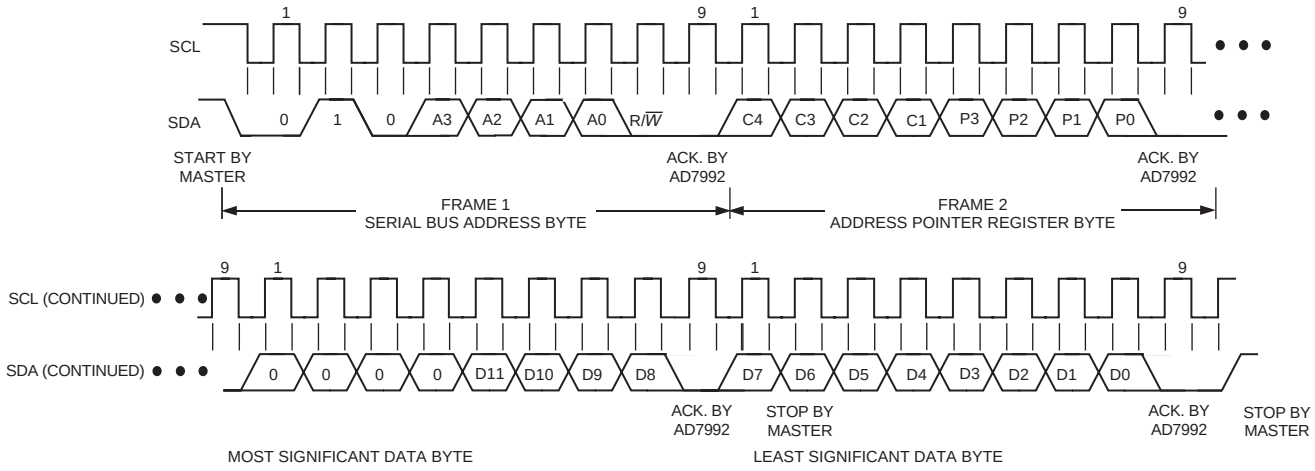


Figure 12. Two Byte Write Sequence

READING DATA FROM THE AD7992

Reading data from the AD7992 is a one or two byte operation. Reading back the contents of the Configuration Register, Alert Status Register or the Cycle Timer Register is a single byte read operation as shown in Figure 13. This assumes the particular register address has previously been set up by a single byte write operation to the Address Pointer Register, Figure 10. Once the register address has been set up, any number of reads can subsequently be performed from that particular register without having to write to the Address Pointer Register again. If a read from a different register is required, then the relevant register address will have to be written to the Address Pointer Register and again any number of reads from this register may then be performed.

Reading data from the Conversion Result Register, $DATA_{HIGH}$ Registers, $DATA_{LOW}$ Registers or Hysteresis Registers is a two byte operation as shown in Figure 14. The same rules apply for a two byte read as a single byte read.

ALERT/BUSY PIN

The ALERT/BUSY may be configured as an Alert or Busy ouput as shown in Table VI.

SMBus ALERT

The AD7992 ALERT output is an SMBus interrupt line for devices that want to trade their ability to master for an extra pin. The AD7992 is a slave only device and uses the

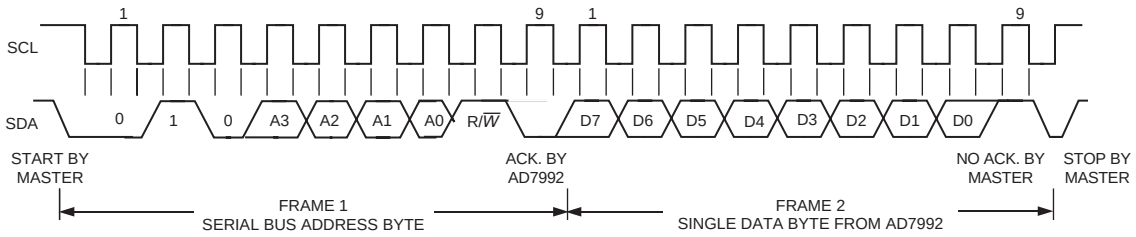


Figure 13. Reading a single byte of data from a selected register

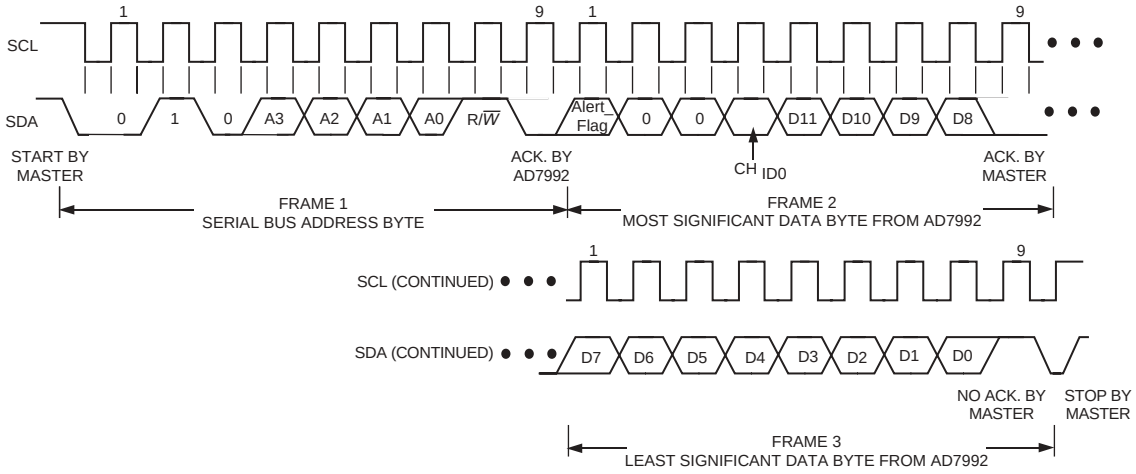


Figure 14. Reading two bytes of data from the Conversion Result Register

SMBus ALERT to signal the host device that it wants to talk. The SMBus ALERT on the AD7992 is used as an out of conversion range indicator.

The ALERT pin has an open-drain configuration which allows the ALERT outputs of several AD7992 devices to be wired-AND together when the ALERT pin is active low. D0 of the Configuration Register is used to set the active polarity of the ALERT output. The power-up default is active low. The ALERT function can be disabled or enabled by setting D2 of the Configuration Register to 1 or 0 respectively.

The host device can process the ALERT interrupt and simultaneously access all SMBus ALERT devices through the alert response address. Only the device which pulled the ALERT low will acknowledge the ARA (Alert Response Address). If more than one device pulls the ALERT pin low, the highest priority (lowest address) device will win communication rights via standard I^2C arbitration during the slave address transfer.

The ALERT output becomes active when the value in the Conversion Result Register exceeds the value in the $DATA_{HIGH}$ Register or falls below the value in the $DATA_{LOW}$ Register . It is reset when a write operation to the Configuration register sets D1 to a 1, or when the conversion result returns N LSBs below or above the value stored in the $DATA_{HIGH}$ Register or $DATA_{LOW}$ Register respectively. N is the value in the Hysteresis register. (See Limit Registers section)

The ALERT output requires an external pull-up resistor. This can be connected to a voltage different from V_{DD} provided the maximum voltage rating of the ALERT output pin is not exceeded. The value of the pull-up resistor depends on the application, but should be as large as possible to avoid excessive sink currents at the ALERT output.

Placing the AD7992-1 into High-speed Mode.

Hs-Mode communication commences after the master addresses all devices connected to the bus with the Master code, 00001XXX, to indicate that a High-Speed Mode transfer is to begin. No device connected to the bus is allowed to Acknowledge the High-Speed Master code, therefore the code is followed by a not-Acknowledge, Figure 15. The master must then issue a repeated start followed by the device Address with a R/$\overline{W}$ bit. The selected device will then acknowledge its address.

All devices continue to operate in Hs-Mode until such a time as the master issues a STOP condition. When the STOP condition is issued the devices all return to F/S Mode.

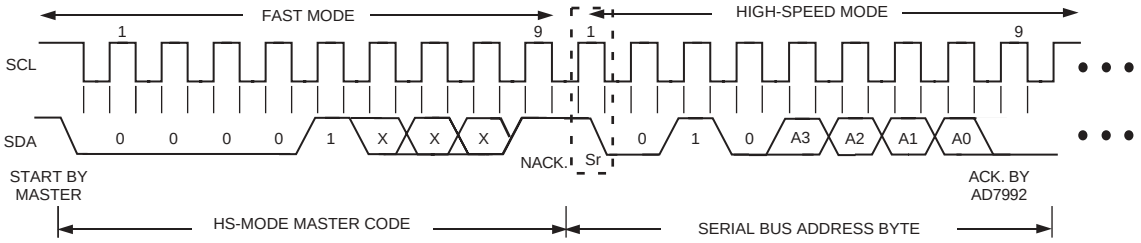


Figure 15. Placing the part into Hs-Mode

MODES OF OPERATION

When supplies are first applied to the AD7992, the ADC powers up in shutdown mode and will remain in this power-down state while not converting. There are three different methods of initiating a conversion on the AD7992.

Mode 1 - Using CONVST Pin.

A conversion can be initiated on the AD7992 by pulsing the $\overline{\text{CONVST}}$ signal. The conversion clock for the part is internally generated so no external clock is required, except when reading from, or writing to the serial port. On the rising edge of $\overline{\text{CONVST}}$ the AD7992 will begin to power up, see point A on Figure 16. The power up time from power-down mode for the AD7992 is approximately 1 us. The $\overline{\text{CONVST}}$ signal must remain high for 1 µs for the part to power up fully. Then $\overline{\text{CONVST}}$ can be brought low after 1 µs. The falling edge of the $\overline{\text{CONVST}}$ signal places the track and hold into hold mode and a conversion is also initiated at this point, see point B Figure 16. When the conversion is complete, approximately 2 us later, the part will return to shutdown (see point C Figure 16) and remain so until the next rising edge of $\overline{\text{CONVST}}$. The master can then read address the ADC to obtain the conversion result. The address point register must be pointing to the conversion result register in order to read back the conversion result.

If the $\overline{\text{CONVST}}$ pulse does not remain high for more than 1 µs, then the falling edge of $\overline{\text{CONVST}}$ will still initiate a conversion but the result will be invalid as the AD7992 will not be fully powered up when the conversion takes place. The $\overline{\text{CONVST}}$ pin should not be pulsed when reading from or writing to the serial port.

The Cycle Timer Register and the Command bits (C4 - C1) in the Address Pointer Register should contain all 0's to operate the AD7992 in this mode. The $\overline{\text{CONVST}}$ pin should be tied low for all other Modes of operation. Prior to initiating a conversion in this mode, a write to the Configuration Register is necessary to select the Channel for conversion. To select both input channels for conversion set D5 and D4 to 1 in the Configuration Register. The ADC will service each channel in the sequence with each $\overline{\text{CONVST}}$ pulse.

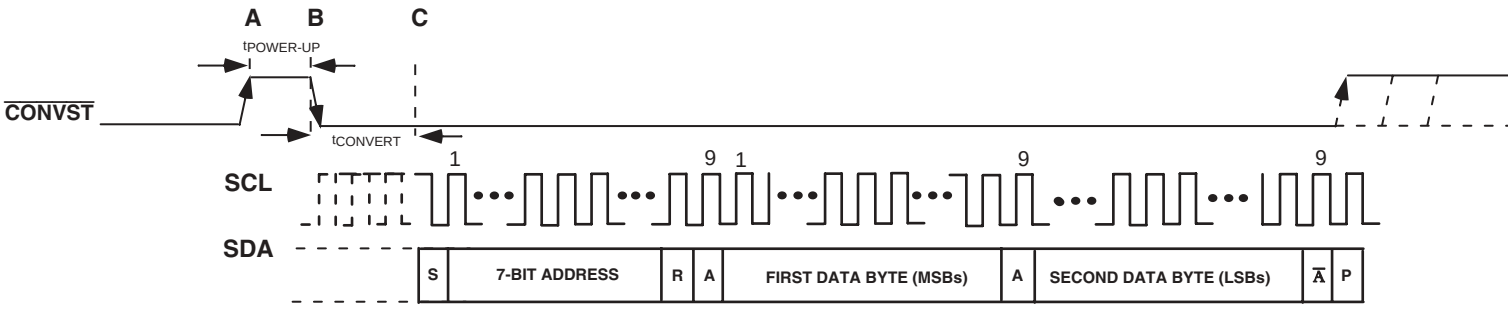


Figure 16. Mode 1 Operation

Mode 2 -

This mode allows a conversion to be automatically initiated anytime a read operation occurs. In order to use this mode the command bits C2 - C1 in the Address Pointer Register shown in Table II must be programmed. The command bits C4 and C3 are not used and should contain zeros at all times.

To select a channel for conversion in this mode, set the corresponding channel command bits in the Address Pointer byte, see Table XIII. To select both Analog inout channels for conversion in this mode set both C1 and C2 to 1. When all four command bits are 0 then this mode is not in use.

Figure 13 illustrates a two byte read operation from the Conversion Result Register. First ensure that the Address pointer is pointing to the conversion result register. When the contents of the Address Pointer Register are being loaded, if the command bits C2 or C1 are set then the AD7992 will begin to power up and convert upon the selected channel(s), power-up will begin on the fourth SCL rising edge of the Address Point Byte, see point A Figure 17. Table XIII shows the channel selection in this mode via the command bits, C1 and C2 in the Address Pointer Register. The wake-up and conversion time together should take approximately 3µs, and the conversion begins when the last Command bit, C1 has been clocked in midway through the write to the Address Pointer Register. Following this, the AD7992 must be addressed again to tell it that a read operation is required. The read then takes place from the Conversion Result register. This read will access the result from the conversion selected via the command bits. If the Command bits C2, C1 were set to 1,1, then a four byte read would be necessary. The first read accesses the data from the conversion on $V_{IN}1$. While this read takes place, a converion occurs on $V_{IN}2$. The second read will access this data from $V_{IN}2$. Figure 18 illustrates how this mode operates.

After the conversion result has been read and if further read bytes are issued the ADC will continuously convert on the selected input channel(s). This has the effect of increasing the overall throughput rate of the ADC.

When operating the AD7992-1 in Mode2 with Hs-Mode, 3.4 MHz SCL, the conversion may not be complete before the master tries to read the conversion result, if this is the case the AD7992-1 will hold the SCL line low after the read address during the ACK clock, until the conversion is complete. When the conversion is complete the AD7992-1 will release the SCL line and the master can then read the conversion result.

Table XIII. Channel Selection in Mode 2

C2	C1	Analog Input Channel
0	0	No Conversion
0	1	Conversion on $V_{IN}1$
1	0	Conversion on $V_{IN}2$
1	1	Conversion on $V_{IN}1$ followed by Converion on $V_{IN}2$

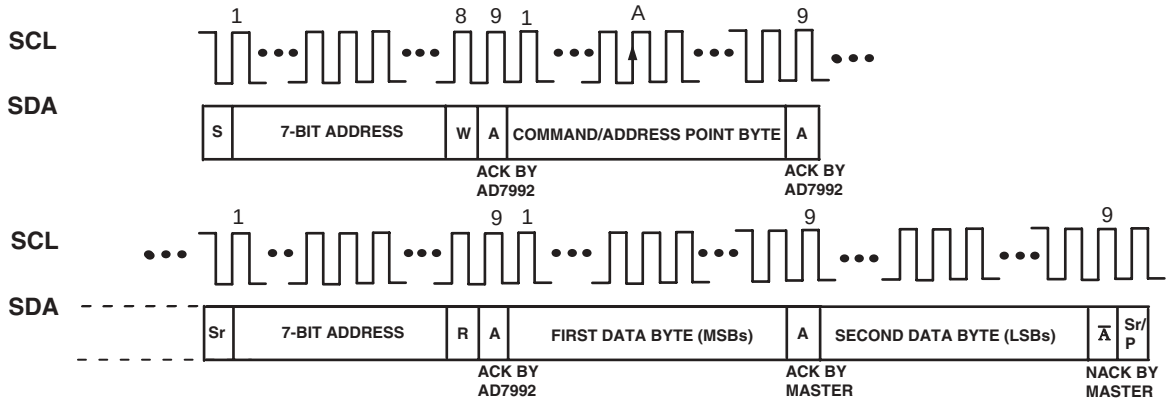


Figure 17. Mode 2 Operation

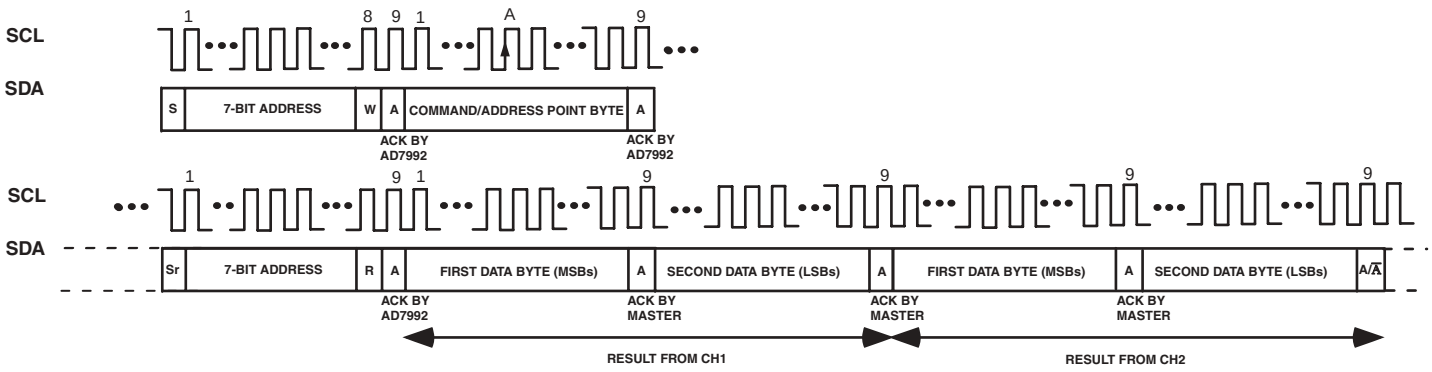


Figure 18. Mode 2 Sequence Operation

Mode 3 - Automatic Cycle Mode

An automatic conversion cycle can be selected and enabled by writing a value to the Cycle Timer Register. A conversion cycle interval can be set up on the AD7992 by programming the relevant bits in the 3-bit Cycle Timer Register as decoded in Table XIIb. When the Cycle Timer register is programmed with any configuration other than all 0's, a conversion will take place every X ms, depending on the configuration of these bits in the Cycle Timer Register. There are 7 different cycle time intervals to choose from as shown in Table XIIb. Once the conversion has taken place the part powers down again until the next conversion occurs. To exit this mode of operation the user must program the Cycle Timer Register to contain all 0's. For cycle interval options see Table XIIb Cycle Timer Intervals.

To select channel(s) for operation in the cycle mode set the corresponding channel(s) bits, D5 and D4, in the Configuration Register. If both D5 and D4 are set to 1 in the Configuration register, the ADC will automatically cycle through the Channels, starting with the lowest channel and working its way up through the sequence. Once the sequence is complete the ADC will start converting on the lowest channel again, continuing to loop through the sequence until the Cycle timer register contents are set to all 0's. This mode is useful for monitoring signals, e.g. battery voltage, temperature etc, alerting only when the limits are violated.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

10-Lead MSOP (RM-10)