ANALOG DEVICES

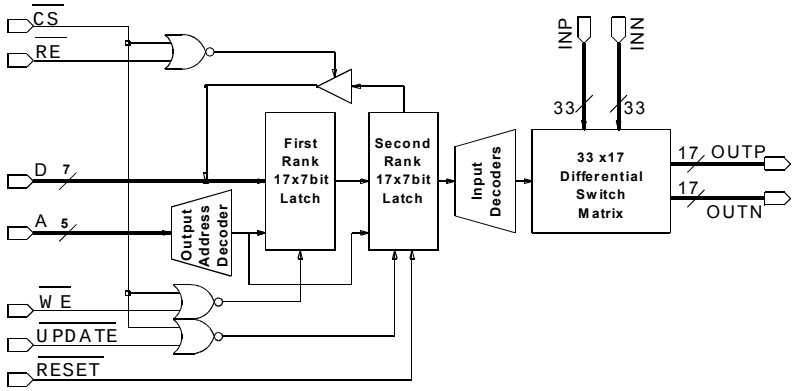
Xstream™ 33 x 17, 3.2Gb/s Digital Crosspoint Switch

Preliminary Technical Data

AD8151*

FEATURES
Low Cost
33 x 17, Fully Differential, Nonblocking Array
3.2 Gbps per Port NRZ Data Rate
Wide Power Supply Range: +5 V, +3.3 V, –3.3 V, –5 V
Low Power
1.5W, 450 mA (Outputs Enabled)
0.1W, 35mA (Outputs Disabled)
PECL and ECL Compatible
CMOS/TTL-Level Control Inputs: 3 V to 5 V
Low Jitter: TBD
No Heat Sinks Required
Drives a Backplane Directly
Programmable Output Current (5 to 25mA)
Optimize Termination Impedance
User-Controlled Voltage at the Load
Minimize Power Dissipation
Individual Output Disable for Busing and Building Larger Arrays
Double Row Latch
Buffered Inputs
Available in 184-Lead LQFP

APPLICATIONS
Fiber Optic Network Switching
High Speed Serial Backplane Routing to OC-48 with FEC



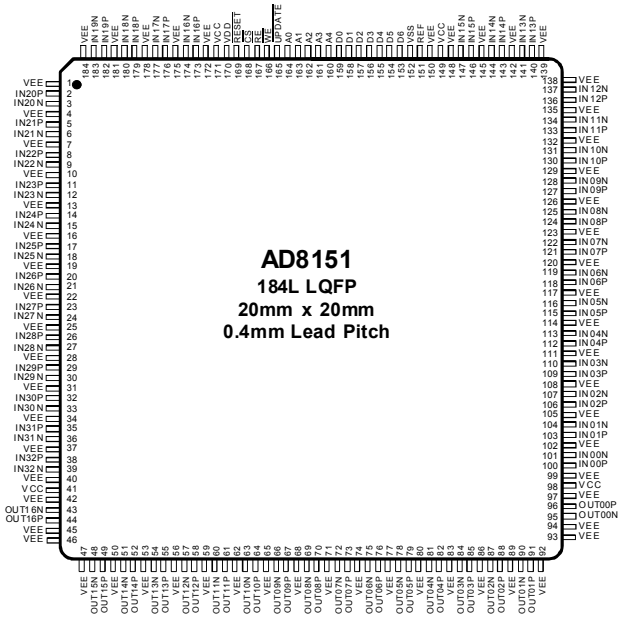
AD8151

PRODUCT DESCRIPTION

AD8151 is a member of the *X* stream line of products and is a breakthrough in digital switching, offering a large switch array (33 × 17) on very little power, typically less than 1.5 W. Additionally, it operates at data rates up to 3.2 Gbps per port, making it suitable for sonet OC-48 with Forward Error Correction (FEC). Further, the pricing of the AD8151 makes it affordable enough to be used for lower data rates as well.

The AD8151's flexible supply voltages allow the user to operate with either PECL or ECL data levels and will operate down to 3.3 V . The control interface is CMOS/TTL compatible (3 V to 5 V).

Its fully differential signal path reduces jitter and crosstalk while allowing the use of smaller single-ended voltage swings.
The AD8151 is offered in a 184-lead LQFP package that operates over the industrial temperature range of 0°C to 85°C.



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* Patent Pending. This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture of this product unless otherwise agreed to in writing.

SPECIFICATIONS

($@25°C$, V_{CC} = +3.3 V to +5 V, V_{EE} = 0V, R_L = 50Ω, I_{OUT} = 16mA, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Max Data Rate/Channel (NRZ)		2.5			Gbps
Channel Jitter	Data Rate < 3.2 Gbps		TBD		ps p-p
RMS Channel Jitter	V_{CC} = 5 V		TBD		ps
Propagation Delay	Input to Output		TBD		ps
Propagation Delay Match			50	100	ps
Output Rise/Fall Time	20% to 80%		100		ps
INPUT CHARACTERISTICS					
Input Voltage	Swing Differential	200		1000	mV p-p
Input Voltage Range	Common-Mode	V_{CC} – 2		V_{CC}	
Input Bias Current			2		µA
Input Capacitance			2		pF
Input V_{IN} High		V_{CC} – 1.2		V_{CC} – 0.2	V
Input V_{IN} Low		V_{CC} – 2.4		V_{CC} – 1.4	V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Differential (See Figure 22)		800		mV p-p
Output Voltage Range		V_{CC} – 1.8		V_{CC}	V
Output Current		5		25	mA
Output Capacitance			2		pF
POWER SUPPLY					
Operating Range					
PECL, V_{CC}	V_{EE} = 0 V	3.3		5	V
ECL, V_{EE}	V_{CC} = 0 V	–5		–3.3	V
V_{DD}		3		5	V
V_{SS}			0		V
Quiescent Current					
V_{DD}			2		mA
V_{EE}	All Outputs Enabled, IOUT = 16 mA		450		mA
	T_{MIN} to T_{MAX}			TBD	mA
	All Outputs Disabled		35		mA
THERMAL CHARACTERISTICS					
Operating Temperature Range		0		85	°C
θ_{JA}			30		°C/W
LOGIC INPUT CHARACTERISTICS	V_{DD} = 3 V dc to 5 V dc				
Input V_{IN} High		1.9	V_{DD}		V
Input V_{IN} Low		0	0.9		V

AD8151 Control Interface

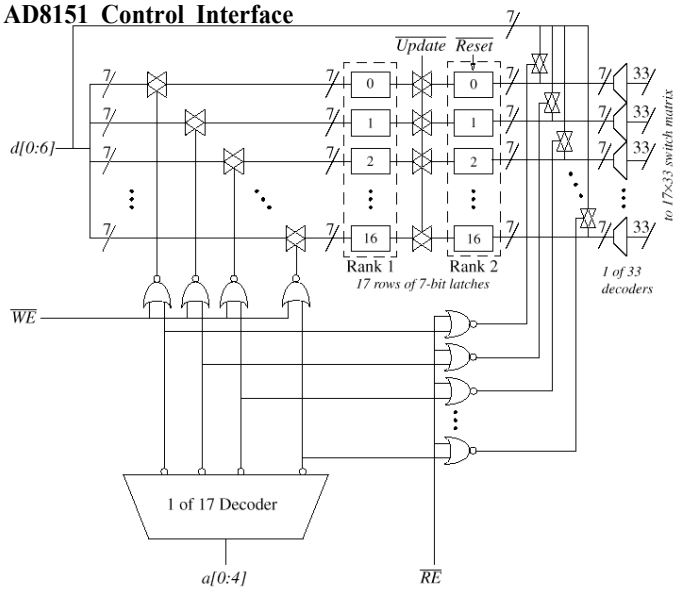


Fig. 1. AD8151 Control Interface (simplified schematic)

The AD8151control interface receives and stores the desired connection matrix for the 33 input and 17 output signal pairs. The interface consists of 17 rows of double-rank 7-bit latches, one for each output. The 7-bit data word stored in these latches indicates to which one (if any) of the 33 inputs the output will be connected.

One output at a time can be pre-programmed by addressing the output and writing the desired connection data into the first rank of latches. This process can be repeated until each of the desired output changes has been pre-programmed. Then, all output connections can be programmed at once by passing the data from the first rank of latches into the second rank. The output connections always reflect the data programmed into the second rank of latches, and do not change until the first rank of data is passed into the second rank.

If necessary for system verification, the data in the second rank of latches can be read back from the control interface.

At any time, a reset pulse can be applied to the control interface to globally reset the appropriate second rank data bits, disabling all 17 signal output pairs. This feature can be used to avoid output bus contention on system start-up. The contents of the first rank remain unchanged.

The control interface pins are connected via logic-level translators. These translators allow programming and readback of the control interface using logic levels different from those in the signal matrix.

In order to facilitate multiple chip address decoding, there is a chip-select pin. All logic signals except the reset pulse are ignored unless the chip select pin is active. The chip select pin

disables only the control logic interface, and does not change the operation of the signal matrix. The chip select pin does not power down any of the latches, so any data programmed in the latches is preserved.

All control pins are level sensitive, not edge-triggered.

Control Pin Description

A[4:0] inputs
Output address pins. The binary encoded address applied to these five input pins determines which one of the seventeen outputs is being programmed (or being read back). The most-significant bit is A4.

D[6:0] inputs/outputs
Input configuration data pins. In write mode, the binary encoded data applied to pins D[6:0] determine which 1 of 33 inputs is to be connected to the output specified with the A[4:0] pins. The most significant bit is D5, and the least significant bit is D0. Bit D6 is the enable bit, setting the specified output signal pair to an enabled state if D6 is logic HIGH, or disabled to a high-impedance state if D6 is logic LOW.

In readback mode, pins D[6:0] are low-impedance outputs indicating the data word stored in the second rank for the output specified with the A[4:0] pins. The readback drivers were designed to drive high impedances only, so external drivers connected to the D[6:0] should be disabled during read-back mode.

WE input
First rank write enable. Forcing this pin to logic LOW allows the data on pins D[6:0] to be stored in the first rank latch for the output specified by pins A[4:0]. The WE pin must be returned to a logic HIGH state after a write cycle to avoid overwriting the first rank data.

Update input
Second rank write enable. Forcing this pin to logic LOW allows the data stored in all 17 first rank latches to be transferred to the second rank latches. The signal connection matrix will be reprogrammed when the second rank data is changed. This is a global pin, transferring all 17 rows of data at once. It is not necessary to program the address pins. It should be noted that after initial power-up of the device, the first rank data is undefined. It may be desirable to pre-program all seventeen outputs before performing the first Update cycle.

RE input
Second rank read-enable. Forcing this pin to logic LOW enables the output drivers on the bi-directional D[6:0] pins, entering the read-back mode of operation. By selecting an output address with the A[4:0] pins and forcing RE to logic LOW, the 7-bit data stored in the second rank latch for that output address will be written to D[6:0] pins. Data should not be written to the D[6:0] pins externally while in read-back mode. The RE and WE pins are not exclusive, and may be used at the same time, but data should not be written to the D[6:0] pins from external sources while in read-back mode.

CS input
Chip-select. This pin must be forced to logic LOW in order to program or receive data from the logic interface, with the exception of the Reset pin, described below. This pin has no effect on the signal pairs and does not alter any of the stored control data.

Reset input
Global output disable pin. Forcing the Reset pin to logic LOW will reset the enable bit, D6, in all 17 second rank latches, regardless of the state of any other pins. This has the effect of immediately disabling the 17 output signal pairs in the matrix. It is useful to momentarily hold Reset at a logic LOW state when powering up the AD8151 in a system that has multiple output signal pairs connected together. Failure to do this may result in several signal outputs contending after power up. The Reset pin is not gated by the state of the chip select pin, CS. It should be noted that the Reset pin does not program the first rank, which will contain undefined data after power-up.

Control Interface Translators

The AD8151 control interface has two supply pins, Vdd and Vss. The potential between the positive logic supply Vdd and the negative logic supply Vss must be at least +3V and no more than +5V. Regardless of supply, the logic threshold is approximately 1.6V above Vss, allowing the interface to be used with most CMOS and TTL logic drivers.

The signal matrix supplies, Vcc and Vee, can be set independent of the voltage on Vdd and Vss, with the constraints that Vcc, Vss and (Vdd – Vee) ≤ 10V. These constraints will allow operation of the control interface on +3V or +5V while the signal matrix is operated on +3.3V or +5V PECL, or –3.3V or –5V ECL.

Control Interface Truth Tables

The following are truth tables for the control interface

Table 1: Basic Control Functions

Control Pins					*Function*
Reset	*CS*	*WE*	*RE*	*Update*	
0	X	X	X	X	**Global Reset**. Reset all second rank enable bits to zero (disable all outputs).
1	1	X	X	X	**Control disable.** Ignore all logic (but the signal matrix still functions as programmed). D[6:0] are high-impedance.
1	0	0	X	X	**Single Output Pre-program**. Write input configuration data from data bus D[6:0] into first rank of latches for the output selected by the output address bus A[4:0].
1	0	X	0	X	**Single Channel Readback**. Readback input confutation data from second rank of latches onto data bus D[6:0] for the single output selected by the output address bus A[4:0].
1	0	X	X	0	**Global Update**. Copy input configuration data from all 17 first rank latches into second rank of latches, updating signal matrix connections for all outputs.
1	0	0	0	1	**Rank Two to Rank One Copy example**. It is possible to simultaneously readback data from rank two and write it to rank one. This may be useful before a Global Reset to perform a "Mute" function, but all 17 outputs must be addressed one at a time.
1	0	0	1	0	**Transparent Write and Update example**. It is possible to write data directly onto rank two. This simplifies logic when synchronous signal matrix updating is not necessary.

Table 2: Address/Data Examples

Output Address Pins msb-lsb					*Enable Bit*	*Input Address Pins msb-lsb*						*Function*
A4	A3	A2	A1	A0	D6/E	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	X	0	0	0	0	0	0	**Lower Address/Data Range**. Connect output #00 (A[4:0] = 00000) to input #00 (D[5:0] = 000000)
1	0	0	0	0	X	1	0	0	0	0	0	**Upper Address/Data Range.** Connect output #16 (A[4:0] = 10000) to input #32 (D[5:0] = 100000)
<binary output number*>					1	< binary input number>						**Enable Output**.. Connect selected output (A[4:0] = 0 to 16) to designated input (D[5:0] = 0 to 32) and enable output (D6=1)
<binary output number*>					0	X	X	X	X	X	X	**Disable Output**. Disable specified output (D6 = 0)
1	0	0	0	1	X	< binary input number>						**Broadcast Connection**. Connect all 17 outputs to same designated input and set all 17 enable bits to the value of D6. Readback is not possible with the broadcast address.
1	0	0	1	0	X	1	0	0	0	0	1	**Reserved**. Any address or data code greater or equal to these are reserved for future expansion or for factory testing.

* the binary output number may also be the broadcast connection designator, 10001X.

Control Interface Timing Diagrams

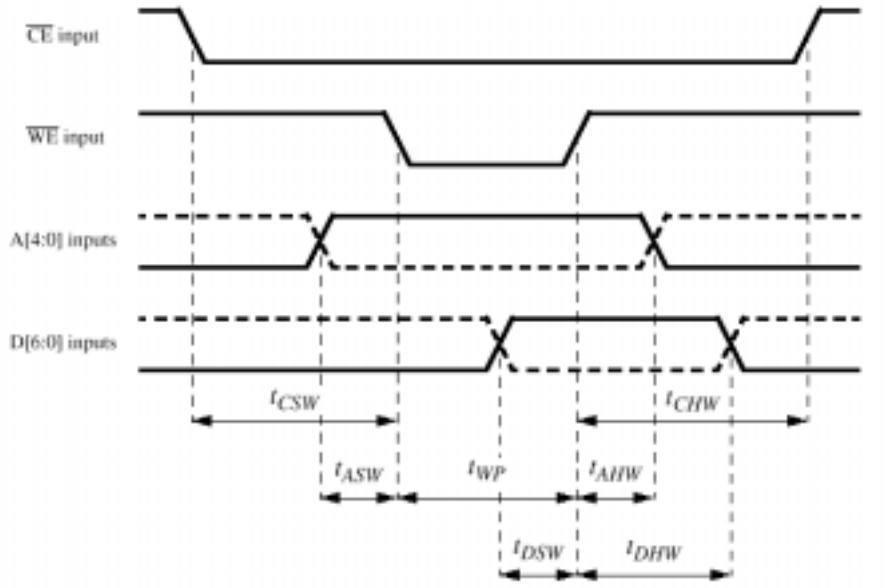


Figure 2. First Rank Write Cycle

Table 3: First Rank Write Cycle

Symbol	Parameter		Conditions	Min	Typ	Max	Units
t_{CSW}	Set-Up Time	Chip Select to Write Enable	T_A = 25°C V_{DD} =+5V V_{CC} = +5V	0			ns
t_{ASW}		Address to Write Enable		0			ns
t_{DSW}		Data to Write Enable		15			ns
t_{CHW}	Hold Time	Chip Select from Write Enable		0			ns
t_{AHW}		Address from Write Enable		0			ns
t_{DHW}		Data from Write Enable		0			ns
t_{WP}	Width of Write Enable Pulse			15			ns

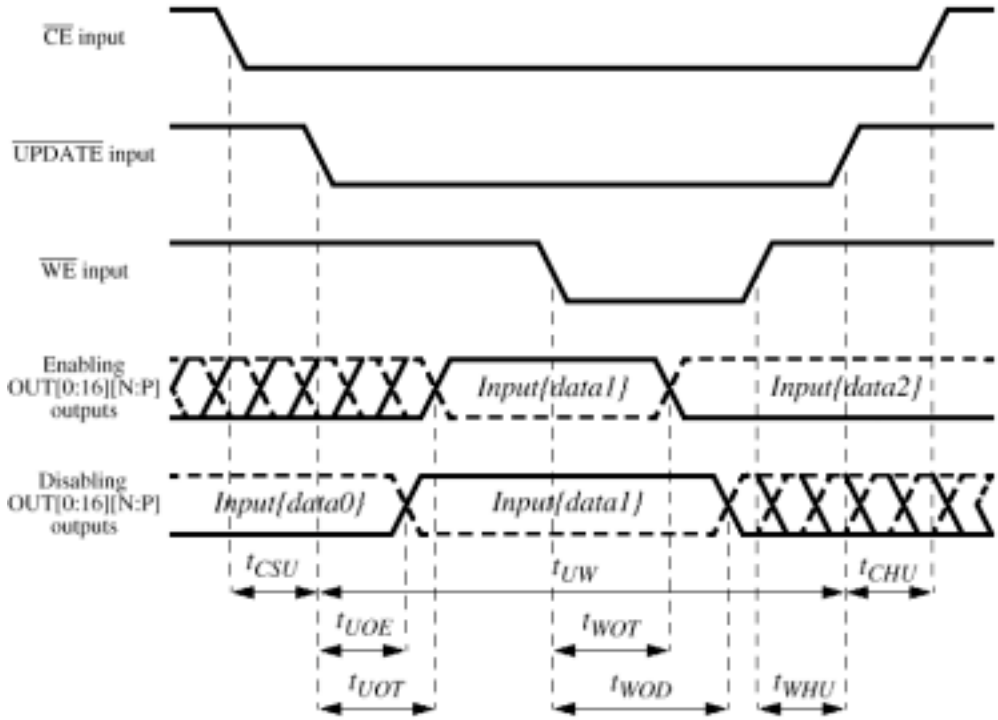


Figure 3. Second Rank Update Cycle

Table 4: Second Rank Update Cycle

Symbol	Parameter		Conditions	Min	Typ	Max	Units
t_{CSU}	Set-Up Time	Chip Select to Update	TA = 25°C VDD = +5V VCC = +5V	0			ns
t_{CHU}	Hold Time	Chip Select from Update		0			ns
t_{UOE}	Output Enable Times	Update to Output Enable		25	40		ns
t_{WOE} (not shown)		Write Enable to Output Enable		25	40		ns
t_{UOT}	Output Toggle Times	Update to Output Reprogram		25	30		ns
t_{WOT}		Write Enable to Output Reprogram		25	30		
t_{UOD} (not shown)	Output Disable Times	Update to Output Disabled		25	30		ns
t_{WOD}		Write Enable to Output Disabled		25	30		ns
t_{WHU}	Set-Up Time	Write Enable to Update		10	20		ns
t_{UW}	Width of Update Pulse			15			ns

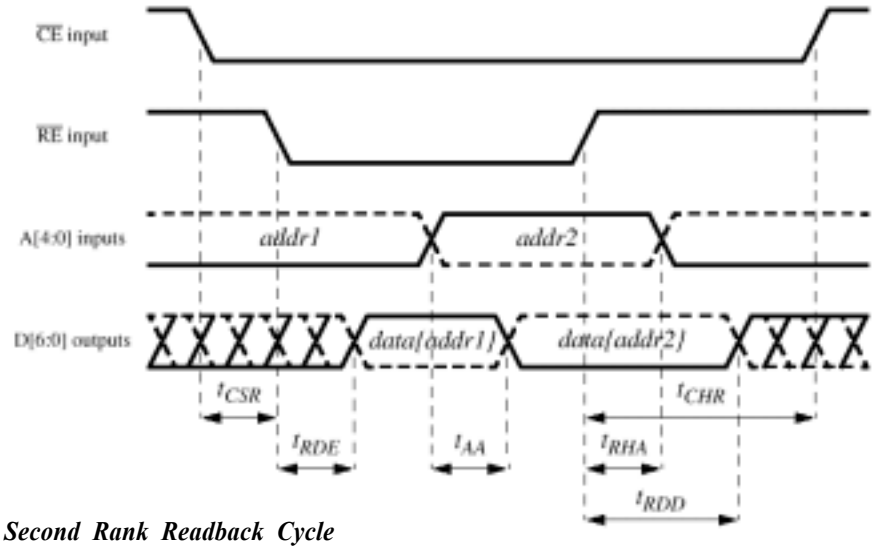


Figure 4. Second Rank Readback Cycle

Table 5: Second Rank ReadbackCycle

Symbol	Parameter		Conditions	Min	Typ	Max	Units
t_{CSR}	Set-Up Time	Chip Select to Read Enable	TA = 25°C VDD = +5V VCC = +5V	0			ns
t_{CHR}	Hold Time	Chip Select from Read Enable		0			ns
t_{RHA}		Address from Read Enable		5			ns
t_{RDE}	Enable Time	Data from Read Enable	10 kΩ, 20 pF on D[6:0] bus		15		ns
t_{AA}	Access Time	Data from Address			15		ns
t_{RDD}	Release Time	Data from Read Enable			15	30	ns

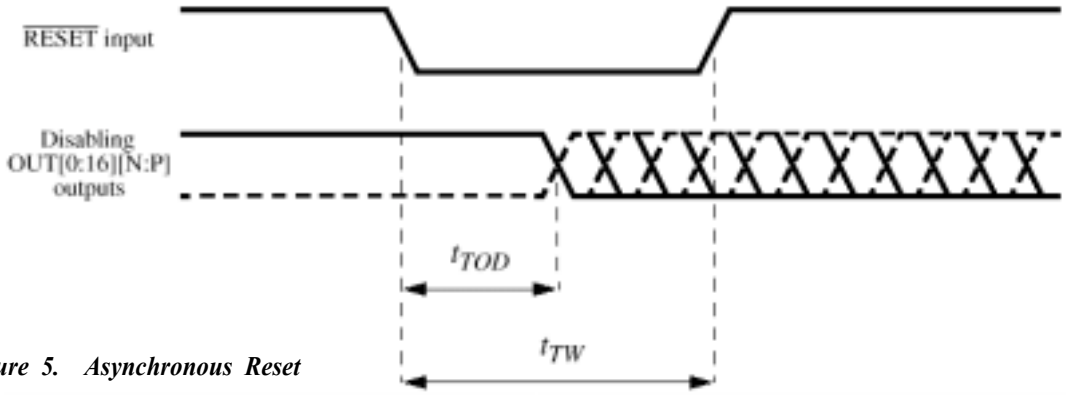


Figure 5. Asynchronous Reset

Table 6: Asynchronous Reset

Symbol	Parameter		Conditions	Min	Typ	Max	Units
t_{TOD}	Disable Time	Output Disable from Reset		25	30		ns
t_{TW}	Width of Reset Pulse			15			ns

Control Interface Programming Example

The following conservative pattern connects all outputs to input number 7, except output 16 which is connected to input number 32. The vector clock period, T_0, is 15ns. It is possible to accelerate the execution of this pattern by deleting vectors 1, 4, 7 and 9.

Table 7: Basic Test Pattern

Vector No.	Reset	CS	WE	RE	Update	A[4:0]	D[6:0]	Comments
0	0	1	1	1	1	xxxxx	xxxxxxx	Disable all outputs
1	1	1	1	1	1	xxxxx	xxxxxxx	
2	1	0	1	1	1	10001	1000111	All outputs to input #07
3	1	0	0	1	1	10001	1000111	Write to first rank
4	1	0	1	1	1	10001	1000111	
5	1	0	1	1	1	10000	1100000	Output #16 to Input #32
6	1	0	0	1	1	10000	1100000	Write to first rank
7	1	0	1	1	1	10000	1100000	
8	1	0	1	1	0	xxxxx	xxxxxxx	Transfer to second rank
9	1	0	1	1	1	xxxxx	xxxxxxx	
10	1	1	1	1	1	xxxxx	xxxxxxx	Disable interface

Circuit Description

The AD8151 is a high-speed 33x17 differential crosspoint switch designed for data rates up to 3.2 Gb/s per channel. The AD8151 supports PECL-compatible input and output levels when operated from a +5V supply (V_{CC} = +5V, V_{EE} = GND) or ECL-compatible levels when operated from a -5V supply (V_{CC} = GND, V_{EE} = -5V). To save power, the AD8151 can run from a +3.3V supply to interface with low-voltage PECL circuits or a -3.3V supply to interface with low-voltage ECL circuits. The AD8151 utilizes differential current mode outputs with individual disable control, which facilitates bussing together the outputs of multiple AD8151's to assemble larger switch arrays. This feature also reduces system crosstalk and can greatly reduce power dissipation in a large switch array. A single external resistor programs the current for all enabled output stages, allowing for user control over output levels with different output termination schemes and transmission line characteristic impedances.

High-Speed Data Inputs (INxxP, INxxN):
The AD8151 has 33 pairs of differential voltage-mode inputs. The common-mode input range extends from the positive supply voltage (V_{CC}) down to include standard ECL or PECL input levels (V_{CC} - 2V). The minimum differential input voltage is less than 300mV. Unused inputs may be connected directly to any level within the allowed common-mode input range. A simplified schematic of the input circuit is shown in Fig. 6, below.

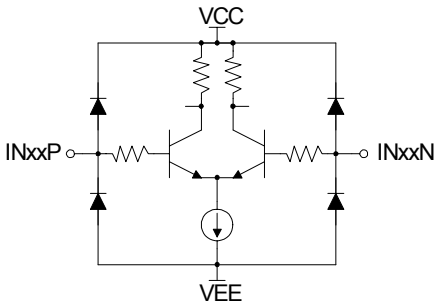


Fig. 6 - AD8151 simplified input circuit.

In order to maintain signal fidelity at the high data rates supported by the AD8151, the input transmission lines should be terminated as close to the input pins as possible. The preferred input termination structure will depend primarily on the application and the output circuit of the data source. Standard ECL components have open emitter outputs that require pulldown resistors. Three input termination networks suitable for this type of source are shown in Fig. 7. The characteristic impedance of the transmission line is shown as Z_o. The resistors, R_1 and R_2, in the Thevenin termination are chosen to synthesize a V_{TT} source with an output resistance of Z_o and an open-circuit output voltage equal to V_{CC} - 2V. The load resistors (R_L) in the differential termination scheme are needed to bias the emitter followers of the ECL source.

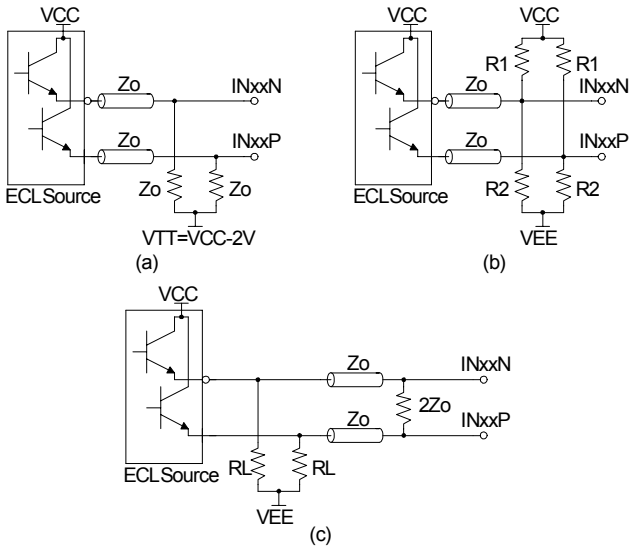


Fig. 7 - AD8151 input termination from ECL/PECL sources: a) Parallel termination using VTT supply, b) Thevenin equivalent termination, c) differential termination.

If the AD8151 is driven from another current mode output stage such as another AD8151, the input termination should be chosen to accommodate that type of source, as explained in the following section.

High-Speed Data Outputs (OUTyyP, OUTyyN):
The AD8151 has 17 pairs of differential current-mode outputs. The output circuit, shown in Fig. 8, is an open-collector NPN current switch with resistor-programmable tail current and output compliance extending from the positive supply voltage (V_{CC}) down to standard ECL or PECL output levels (V_{CC} - 2V). The outputs may be disabled individually to permit outputs from multiple AD8151's to be connected directly. Since the output currents of multiple enabled output stages connected in this way sum, care should be taken to ensure that the output compliance limit is not exceeded at any time; this can be achieved by disabling the active output driver before enabling any inactive driver.

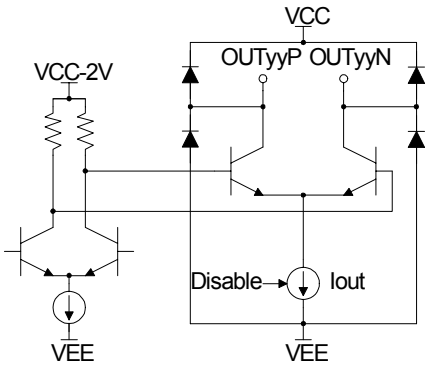


Fig. 8 - AD8151 simplified output circuit.

To ensure proper operation, all outputs (including unused output) must be pulled high using external pullup networks to a level within the output compliance range. If outputs from multiple AD8151's are wired together, a single pullup network may be used for each output bus. The pullup network should be chosen to keep the output voltage levels within the output compliance range at all times. Recommended pullup networks to produce PECL/ECL 100K and 10K compatible outputs are shown in Fig. 9. Alternatively a seperate supply can be used to provide V_{COM}, R_{COM} and D_{COM} if necessary.

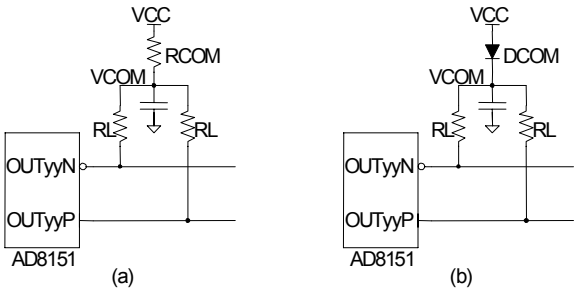


Fig. 9 -AD8151 output pullup networks:
a) ECL 100K, b) ECL 10K.

The output levels are simply:

$$V_{OH} = V_{COM}$$

$$V_{OL} = V_{COM} - I_{OUT}R_L$$

$$V_{SWING} = V_{OH} - V_{OL} = I_{OUT}R_L$$

$$V_{COM} = V_{CC} - I_{OUT}R_{COM} \text{ (100K mode)}$$

$$V_{COM} = V_{CC} - V(D_{COM}) \text{ (10K mode)}$$

The common-mode adjustment element (R_{COM} or D_{COM}) may be omitted if the input range of the receiver includes the positive supply voltage. The bypass capacitors reduce common-mode perturbations by providing an ac short from the common nodes (V_{COM}) to ground.

When bussing together the outputs of multiple AD8151's or when running at high data rates, double termination of its outputs is recommended to mitigate the impact of reflections due to open transmission line stubs and the lumped capacitance of the AD8151 output pins. A possible connection is shown in Fig. 10 below; the bypass capacitors provide an ac short from the common nodes of the termination resistors to ground. To maintain signal fidelity at high data rates, the stubs connecting the output pins to the output transmission lines or load resistors should be as short as possible.

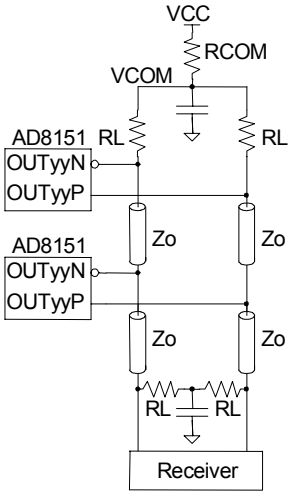


Fig. 10 - Double termination of AD8151 outputs.

In this case, the output levels are:

$$V_{OH} = V_{COM} - (1/4)I_{OUT}R_L$$

$$V_{OL} = V_{COM} - (3/4)I_{OUT}R_L$$

$$V_{SWING} = V_{OH} - V_{OL} = (1/2)I_{OUT}R_L$$

Output Current Set Pin (REF):

A simplified schematic of the reference circuit is shown in Fig. 11. A single external resistor connected between the REF pin and VEE determines the output current for all output stages. This feature allows a choice of pull-up networks and transmission line characteristic impedances while still achieving a nominal output swing of 800 mV. At low data rates, substantial power savings can be achieved by using lower output swings and higher load resistances.

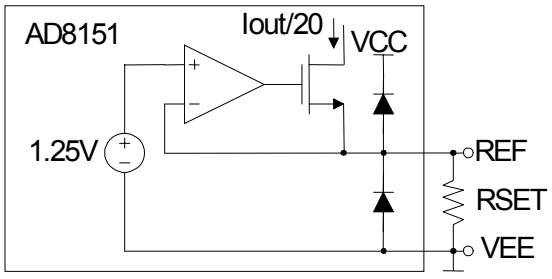


Fig. 11 - AD8151 simplified reference circuit.

The nominal output current is given by the following expression:

$$I_{OUT} = 20\left(\frac{1.25V}{R_{SET}}\right)$$

The minimum set resistor is $R_{SET,min}$ = 1kΩ resulting in $I_{OUT,max}$ = 25mA. The maximum set resistor is $R_{SET,max}$ = 5kΩ resulting in $I_{OUT,min}$ = 5mA. Nominal 800 mV output swings can be achieved in a 50Ω load using R_{SET} = 1.56kΩ (I_{OUT} = 16mA) or in a doubly-terminated 75Ω load using R_{SET} = 1.17kΩ (I_{OUT} = 21.3mA).

To minimize stray capacitance and avoid the pickup of unwanted signals, the external set resistor should be located close to the REF pin. Bypassing the set resistor is not recommended.

Power Supplies

There are several options for the power supply voltages for the AD8151, as there are two separate sections of the chip that require power supplies. These are the control logic and the high-speed data paths. Depending on the system architecture, the voltage levels of these supplies can vary.

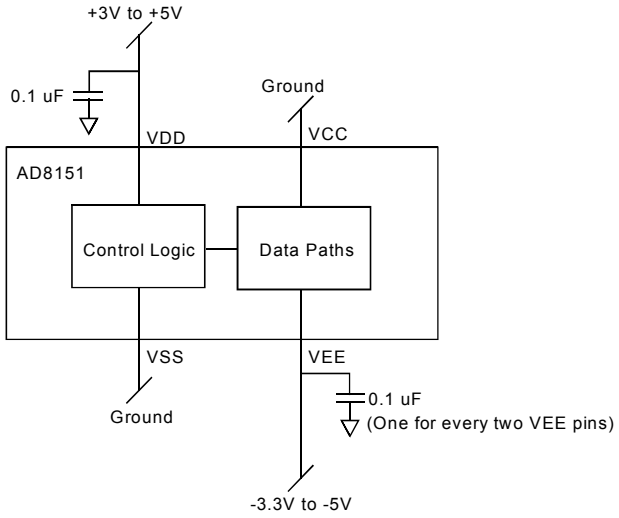
Logic Supplies

The control (programming) logic is CMOS and is designed to interface with any of the various standard single-ended logic families (CMOS or TTL). Its supply voltage pins are VDD (pin 170, logic positive) and VSS (pin 152, logic ground). In all cases the logic ground should be connected to the system digital ground. VDD should be supplied at between +3.3V to +5V to match the supply voltage of the logic family that is used to drive the logic inputs. VCC should be bypassed to ground with a 0.1 uF ceramic capacitor. The absolute maximum voltage from VDD to VSS is 5.5V.

Data Path Supplies

The data path supplies have more options for their voltage levels. The choices here will affect several other areas, like power dissipation, bypassing, and common mode levels of the inputs and outputs. The more positive voltage supply for the data paths is VCC (pins 41, 98, 149 and 171). The more negative supply is VEE, which appears on many pins that will not be listed here. The maximum allowable voltage across these supplies is 5.5V.

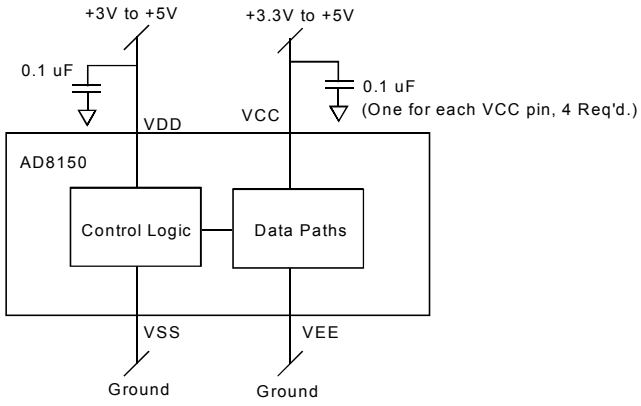
The first choice in the data path power supplies is to decide whether to run the device as ECL (Emitter-Coupled Logic) or PECL (Positive ECL). For ECL operation, VCC will be at ground potential, while VEE will be at a negative supply between –3.3V to –5V. This will make the common-mode voltage of the inputs and outputs at a negative voltage. See ECL Power Supply and Bypassing figure.



PowerSupplies and Bypassing for ECL Operation

If the data paths are to be dc-coupled to other ECL logic devices that run with ground as the most positive supply and a negative voltage for VEE, then this is the proper way to run. However, if the part is to be ac coupled, it is not necessary to have the input/output common mode at the same level as the other system circuits, but it will probably be more convenient to use the same supply rails for all devices.

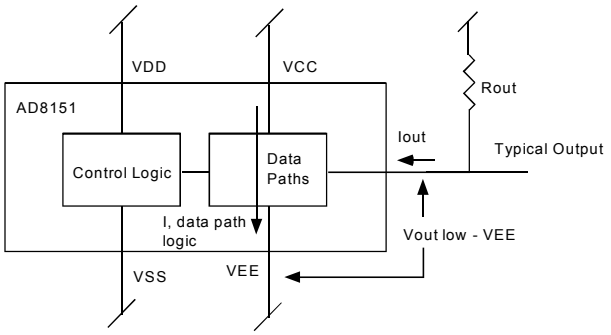
For PECL operation, VEE will be at ground potential and VCC will be a positive voltage from +3.3V to +5V. Thus, the common mode of the inputs and outputs will be at a positive voltage. These can then be dc coupled to other PECL operated devices. If the data paths are ac coupled, then the common mode levels do not matter. See PECL Power Supply and Bypassing figure.



PowerSupplies and Bypassing for PECL Operation

Power Dissipation

For analysis, the power dissipation of the AD8151 can be divided into three separate parts. These are the control logic, the data path circuits and the (ECL or PECL) outputs, which are part of the data path circuits, but can be dealt with separately. The first of these, the control logic, is CMOS technology and does not dissipate a significant amount of power. This power will, of course, be greater when the logic supply is +5V rather than +3V, but overall it is not a significant amount of power and can be ignored for thermal analysis.



Major Power Consumption Paths

The data path circuits operate between the supplies VCC and VEE. As described in the power supply section, this voltage can range from 3.3V to 5V. The current consumed by this section will be constant, so operating at a lower voltage can save about 40 percent in power dissipation.

The power dissipated in the data path outputs is affected by several factors. The first is whether the outputs are enabled or disabled. The worst case occurs when all of the outputs are enabled.

The current consumed by the data path logic can be approximated by:

$$Icc = 35mA + [4.5\ mA + (Iout/20\ mA * 3\ mA)] * (\#\ of\ outputs\ enabled)$$

This says that there will always be a minimum of 35 mA flowing. Icc will increase by a factor that is proportional to both the number of enabled outputs and the programmed output current.

The power dissipated in this circuit section will simply be the voltage of this section (VCC – VEE) times the current. For a worst case, assume that VCC-VEE is 5.0V, all outputs are enabled and the programmed output current is 25 mA. The power dissipated by the data path logic will be:

$$P = 5.0V\ \{35mA + [4.5\ mA + (25\ mA/20\ mA * 3\ mA)] * 17\} = 876\ mW$$

The power dissipated by the output current depends on several factors. These are the programmed output current, the voltage drop from a logic low output to V_{EE} and the number of enabled outputs. A simplifying assumption is that one of each (enabled) differential output pair will be low and draw the full output current (and dissipate most of the power for that output), while the complementary output of the pair will be high and draw insignificant current. Thus, its power dissipation of the high output can be ignored and the output power dissipation for each output can be assumed to occur in a single static low output that sinks the full output-programmed current.

The voltage across which this current flows can also vary, depending on the output circuit design and the supplies that are used for the data path circuitry. In general, however, there will be a voltage difference between a logic low signal and VEE. This is the drop across which the output current flows. For a worst case, this voltage can be as high as 3.5V. Thus, for all outputs enabled and the programmed output current set to 25 mA, the power dissipated by the outputs :

$$P = 3.5V\ (25\ mA) * 17 = 1.49\ W$$

Heat Sinking

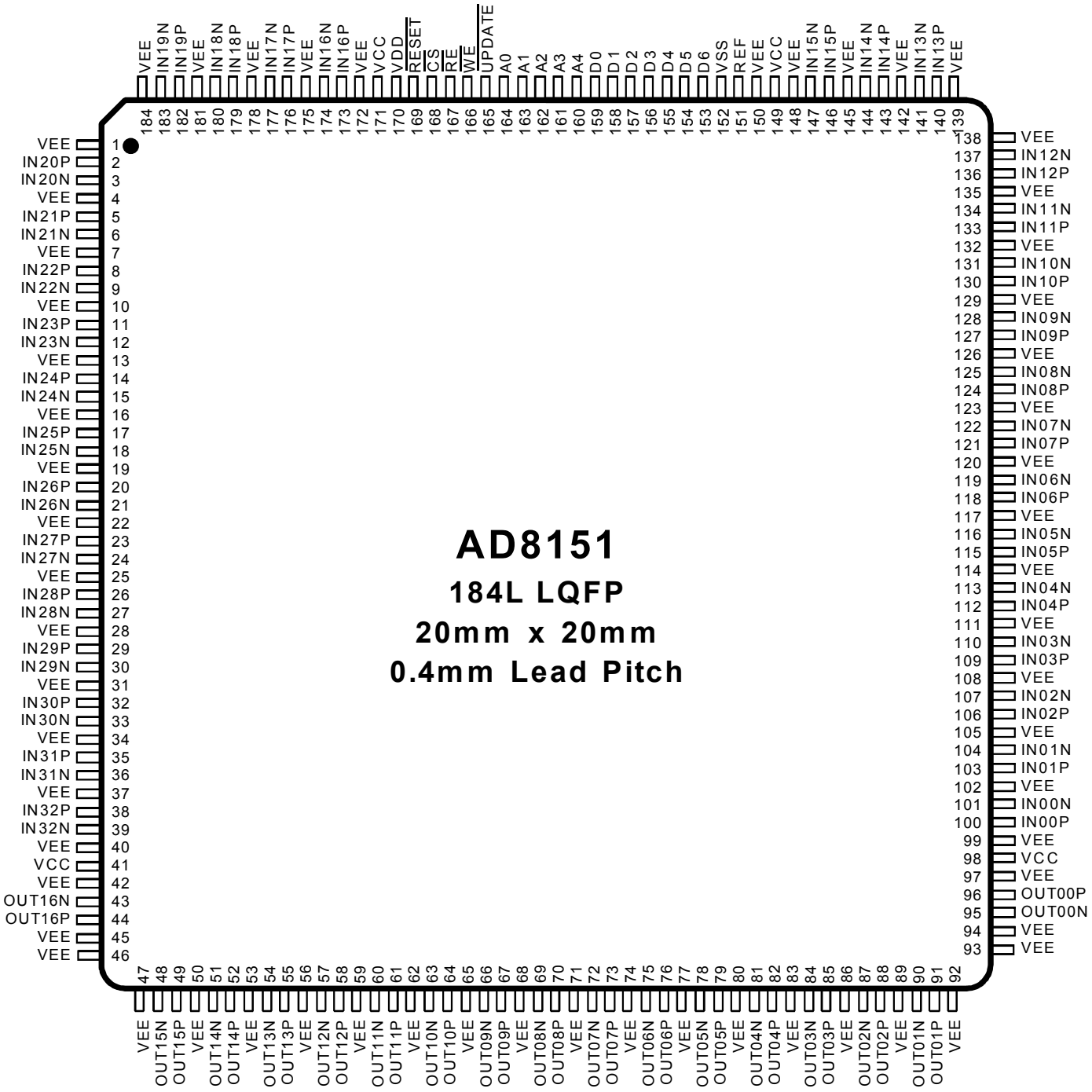
Depending on several factors in its operation, the AD8151 can dissipate upwards of 2 watts or more. The part is designed to operate without the need for an explicit external heatsink. However, the package design offers enhanced heat removal via some of the package pins to the pc board traces.

The VEE pins on the Input sides of the package (pins 1 to 46 and pins 93 to 138) have “finger” extensions inside the package that connect the “paddle” upon which the IC chip is mounted. These pins provide a lower thermal resistance from the IC to the VEE pins than other pins that just have a bond wire. As a result these pins can be used to enhance the heat removal process from the IC to the circuit board and ultimately to the ambient.

The VEE pins described above should be connected to a large area of circuit board trace material in order to take most advantage their lower thermal resistance. If there is a large area available on an inner layer that is at VEE potential, then vias can be provided from the package pin traces to this layer. There should be no thermal-relief pattern when connecting the vias to the inner layers for these VEE pins. Additional vias in parallel and close to the pin leads can provide an even lower thermal resistive path. If possible to use, 2 oz. copper foil will provide better heat removal than 1 oz.

The AD8151 package has a specified thermal impedance Θja of 30°C per watt. This is the worst case, still-air value that can be expected when the circuit board does not significantly enhance the heat removal from the package. By using the concept described above or by using forced-air circulation, the thermal impedance can be lowered.

For an extreme worst case analysis, the junction rise above the ambient can be calculated assuming 2 W of power dissipation and Θja of 30°C /Watt to yield a 60 deg C rise above the ambient. There are many techniques described above that can mitigate this situation. Most actual circuits will not result in this high a rise of the junction temperature above the ambient.


AD8151
184L LQFP
20mm x 20mm
0.4mm Lead Pitch
1 VEE
2 IN20P
3 IN20N
4 VEE
5 IN21P
6 IN21N
7 VEE
8 IN22P
9 IN22N
10 VEE
11 IN23P
12 IN23N
13 VEE
14 IN24P
15 IN24N
16 VEE
17 IN25P
18 IN25N
19 VEE
20 IN26P
21 IN26N
22 VEE
23 IN27P
24 IN27N
25 VEE
26 IN28P
27 IN28N
28 VEE
29 IN29P
30 IN29N
31 VEE
32 IN30P
33 IN30N
34 VEE
35 IN31P
36 IN31N
37 VEE
38 IN32P
39 IN32N
40 VEE
41 VCC
42 VEE
43 OUT16N
44 OUT16P
45 VEE
46 VEE
47 VEE
48 OUT15N
49 OUT15P
50 VEE
51 OUT14N
52 OUT14P
53 VEE
54 OUT13N
55 OUT13P
56 VEE
57 OUT12N
58 OUT12P
59 VEE
60 OUT11N
61 OUT11P
62 VEE
63 OUT10N
64 OUT10P
65 VEE
66 OUT09N
67 OUT09P
68 VEE
69 OUT08N
70 OUT08P
71 VEE
72 OUT07N
73 OUT07P
74 VEE
75 OUT06N
76 OUT06P
77 VEE
78 OUT05N
79 OUT05P
80 VEE
81 OUT04N
82 OUT04P
83 VEE
84 OUT03N
85 OUT03P
86 VEE
87 OUT02N
88 OUT02P
89 VEE
90 OUT01N
91 OUT01P
92 VEE
93 VEE
94 VEE
95 OUT00N
96 OUT00P
97 VEE
98 VCC
99 VEE
100 IN00P
101 IN00N
102 VEE
103 IN01P
104 IN01N
105 VEE
106 IN02P
107 IN02N
108 VEE
109 IN03P
110 IN03N
111 VEE
112 IN04P
113 IN04N
114 VEE
115 IN05P
116 IN05N
117 VEE
118 IN06P
119 IN06N
120 VEE
121 IN07P
122 IN07N
123 VEE
124 IN08P
125 IN08N
126 VEE
127 IN09P
128 IN09N
129 VEE
130 IN10P
131 IN10N
132 VEE
133 IN11P
134 IN11N
135 VEE
136 IN12P
137 IN12N
138 VEE
139 VEE
140 IN13P
141 IN13N
142 VEE
143 IN14P
144 IN14N
145 VEE
146 IN15P
147 IN15N
148 VEE
149 VCC
150 VEE
151 REF
152 VSS
153 D6
154 D5
155 D4
156 D3
157 D2
158 D1
159 D0
160 A4
161 A3
162 A2
163 A1
164 A0
165 UPDATE
166 WE
167 RE
168 CS
169 RESET
170 VDD
171 VCC
172 VEE
173 IN16P
174 IN16N
175 VEE
176 IN17P
177 IN17N
178 VEE
179 IN18P
180 IN18N
181 VEE
182 IN19P
183 IN19N
184 VEE

Signal	Type	Pin No.	Description
VEE	Power Supply	1	Most Negative PECL Supply (Common with other points labeled VEE)
IN20P	PECL	2	High speed input
IN20N	PECL	3	High speed input compliment
VEE	Power Supply	4	Most Negative PECL Supply (Common with other points labeled VEE)
IN21P	PECL	5	High speed input
IN21N	PECL	6	High speed input compliment
VEE	Power Supply	7	Most Negative PECL Supply (Common with other points labeled VEE)
IN22P	PECL	8	High speed input
IN22N	PECL	9	High speed input compliment
VEE	Power Supply	10	Most Negative PECL Supply (Common with other points labeled VEE)
IN23P	PECL	11	High speed input
IN23N	PECL	12	High speed input compliment
VEE	Power Supply	13	Most Negative PECL Supply (Common with other points labeled VEE)
IN24P	PECL	14	High speed input
IN24N	PECL	15	High speed input compliment
VEE	Power Supply	16	Most Negative PECL Supply (Common with other points labeled VEE)
IN25P	PECL	17	High speed input
IN25N	PECL	18	High speed input compliment
VEE	Power Supply	19	Most Negative PECL Supply (Common with other points labeled VEE)
IN26P	PECL	20	High speed input
IN26N	PECL	21	High speed input compliment
VEE	Power Supply	22	Most Negative PECL Supply (Common with other points labeled VEE)
IN27P	PECL	23	High speed input
IN27N	PECL	24	High speed input compliment
VEE	Power Supply	25	Most Negative PECL Supply (Common with other points labeled VEE)
IN28P	PECL	26	High speed input
IN28N	PECL	27	High speed input compliment
VEE	Power Supply	28	Most Negative PECL Supply (Common with other points labeled VEE)
IN29P	PECL	29	High speed input
IN29N	PECL	30	High speed input compliment

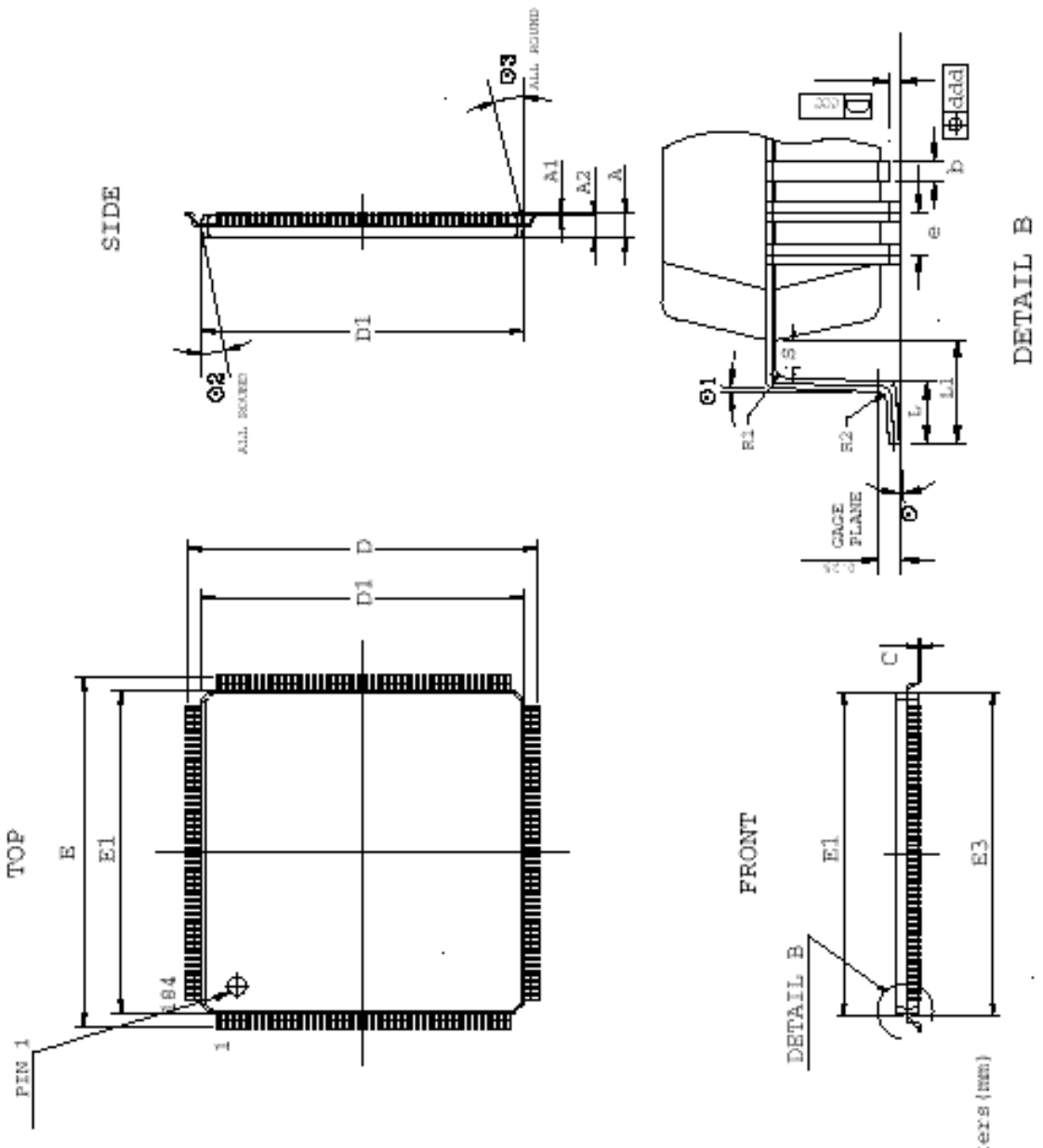
Signal	Type	Pin No.	Description
VEE	Power Supply	31	Most Negative PECL Supply (Common with other points labeled VEE)
IN30P	PECL	32	High speed input
IN30N	PECL	33	High speed input compliment
VEE	Power Supply	34	Most Negative PECL Supply (Common with other points labeled VEE)
IN31P	PECL	35	High speed input
IN31N	PECL	36	High speed input compliment
VEE	Power Supply	37	Most Negative PECL Supply (Common with other points labeled VEE)
IN32P	PECL	38	High speed input
IN32N	PECL	39	High speed input compliment
VEE	Power Supply	40	Most Negative PECL Supply (Common with other points labeled VEE)
VCC	Power Supply	41	Most Positive PECL Supply (Common with other points labeled VCC)
VEE	Power Supply	42	Most Negative PECL Supply (Common with other points labeled VEE)
OUT16N	PECL	43	High speed output
OUT16P	PECL	44	High speed output compliment
VEEA16	Power Supply	45	Most Negative PECL Supply (unique to this output)
VEE	Power Supply	46	Most Negative PECL Supply (Common with other points labeled VEE)
VEE	Power Supply	47	Most Negative PECL Supply (Common with other points labeled VEE)
OUT15N	PECL	48	High speed output compliment
OUT15P	PECL	49	High speed output
VEEA15	Power Supply	50	Most Negative PECL Supply (unique to this output)
OUIT14N	PECL	51	High speed output compliment
OUT14P	PECL	52	High speed output
VEEA14	Power Supply	53	Most Negative PECL Supply (unique to this output)
OUT13N	PECL	54	High speed output compliment
OUT13P	PECL	55	High speed output
VEEA13	Power Supply	56	Most Negative PECL Supply (unique to this output)
OUT12N	PECL	57	High speed output compliment
OUT12P	PECL	58	High speed output
VEEA12	Power Supply	59	Most Negative PECL Supply (unique to this output)
OUT11N	PECL	60	High speed output compliment
OUT11P	PECL	61	High speed output

Signal	Type	Pin No.	Description
VEEA11	Power Supply	62	Most Negative PECL Supply (unique to this output)
OUT10N	PECL	63	High speed output compliment
OUT10P	PECL	64	High speed output
VEEA10	Power Supply	65	Most Negative PECL Supply (unique to this output)
OUT9N	PECL	66	High speed output compliment
OUT9P	PECL	67	High speed output
VEEA9	Power Supply	68	Most Negative PECL Supply (unique to this output)
OUT8N	PECL	69	High speed output compliment
OUT8P	PECL	70	High speed output
VEEA8	Power Supply	71	Most Negative PECL Supply (unique to this output)
OUT7N	PECL	72	High speed output compliment
OUT7P	PECL	73	High speed output
VEEA7	Power Supply	74	Most Negative PECL Supply (unique to this output)
OUT6N	PECL	75	High speed output compliment
OUT6P	PECL	76	High speed output
VEEA6	Power Supply	77	Most Negative PECL Supply (unique to this output)
OUT5N	PECL	78	High speed output compliment
OUT5P	PECL	79	High speed output
VEEA5	Power Supply	80	Most Negative PECL Supply (unique to this output)
OUT4N	PECL	81	High speed output compliment
OUT4P	PECL	82	High speed output
VEEA4	Power Supply	83	Most Negative PECL Supply (unique to this output)
OUT3N	PECL	84	High speed output compliment
OUT3P	PECL	85	High speed output
VEEA3	Power Supply	86	Most Negative PECL Supply (unique to this output)
OUT2N	PECL	87	High speed output compliment
OUT2P	PECL	88	High speed output
VEEA2	Power Supply	89	Most Negative PECL Supply (unique to this output)
OUT1N	PECL	90	High speed output compliment
OUT1P	PECL	91	High speed output
VEE	Power Supply	92	Most Negative PECL Supply (Common with other points labeled VEE)
VEE	Power Supply	93	Most Negative PECL Supply (Common with other points labeled VEE)
VEEA1	Power Supply	94	Most Negative PECL Supply (unique to this output)
OUT0N	PECL	95	High speed output compliment
OUT0P	PECL	96	High speed output

Signal	Type	Pin No.	Description
VEEA0	Power Supply	97	Most Negative PECL Supply (unique to this output)
VCC	Power Supply	98	Most Positive PECL Supply (Common with other points labeled VCC)
VEE	Power Supply	99	Most Negative PECL Supply (Common with other points labeled VEE)
IN0P	PECL	100	High speed input
IN0N	PECL	101	High speed input compliment
VEE	Power Supply	102	Most Negative PECL Supply (Common with other points labeled VEE)
IN1P	PECL	103	High speed input
IN1N	PECL	104	High speed input compliment
VEE	Power Supply	105	Most Negative PECL Supply (Common with other points labeled VEE)
IN2P	PECL	106	High speed input
IN2N	PECL	107	High speed input compliment
VEE	Power Supply	108	Most Negative PECL Supply (Common with other points labeled VEE)
IN3P	PECL	109	High speed input
IN3N	PECL	110	High speed input compliment
VEE	Power Supply	111	Most Negative PECL Supply (Common with other points labeled VEE)
IN4P	PECL	112	High speed input
IN4N	PECL	113	High speed input compliment
VEE	Power Supply	114	Most Negative PECL Supply (Common with other points labeled VEE)
IN5P	PECL	115	High speed input
IN5N	PECL	116	High speed input compliment
VEE	Power Supply	117	Most Negative PECL Supply (Common with other points labeled VEE)
IN6P	PECL	118	High speed input
IN6N	PECL	119	High speed input compliment
VEE	Power Supply	120	Most Negative PECL Supply (Common with other points labeled VEE)
IN7P	PECL	121	High speed input
IN7N	PECL	122	High speed input compliment
VEE	Power Supply	123	Most Negative PECL Supply (Common with other points labeled VEE)
IN8P	PECL	124	High speed input
IN8N	PECL	125	High speed input compliment
VEE	Power Supply	126	Most Negative PECL Supply (Common with other points

Signal	Type	Pin No.	Description
IN9P	PECL	127	High speed input
IN9N	PECL	128	High speed input compliment
VEE	Power Supply	129	Most Negative PECL Supply (Common with other points labeled VEE)
IN10P	PECL	130	High speed input
IN10N	PECL	131	High speed input compliment
VEE	Power Supply	132	Most Negative PECL Supply (Common with other points labeled VEE)
IN11P	PECL	133	High speed input
IN11N	PECL	134	High speed input compliment
VEE	Power Supply	135	Most Negative PECL Supply (Common with other points labeled VEE)
IN12P	PECL	136	High speed input
IN12N	PECL	137	High speed input compliment
VEE	Power Supply	138	Most Negative PECL Supply (Common with other points labeled VEE)
VEE	Power Supply	139	Most Negative PECL Supply (Common with other points labeled VEE)
IN13P	PECL	140	High speed input
IN13N	PECL	141	High speed input compliment
VEE	Power Supply	142	Most Negative PECL Supply (Common with other points labeled VEE)
IN14P	PECL	143	High speed input
IN14N	PECL	144	High speed input compliment
VEE	Power Supply	145	Most Negative PECL Supply (Common with other points labeled VEE)
IN15P	PECL	146	High speed input
IN15N	PECL	147	High speed input compliment
VEE	Power Supply	148	Most Negative PECL Supply (Common with other points labeled VEE)
VCC	Power Supply	149	Most Positive PECL Supply (Common with other points labeled VCC)
VEE REF	R-Program	150	Connection point for output logic pull-down programming resistor(must be connected to VEE)
REF	R-Program	151	Connection point for output logic pull-down programming resistor
VSS	Power Supply	152	Most Negative Control Logic Supply
D6	TTL	153	Enable/Disable Output
D5	TTL	154	(32) MSB Input select
D4	TTL	155	(16)
D3	TTL	156	(8)
D2	TTL	157	(4)
D1	TTL	158	(2)
D0	TTL	159	(1) LSB Input select
A4	TTL	160	(16) MSB Output select
A3	TTL	161	(8)
A2	TTL	162	(4)
D0	TTL	159	(1) LSB Input select
A4	TTL	160	(16) MSB Output select
A3	TTL	161	(8)
A2	TTL	162	(4)
A1	TTL	163	(2)
A0	TTL	164	(1) LSB Output select
UPDATE	TTL	165	Outputs programmed
WRITE	TTL	166	accept data in latch
READ	TTL	167	make latched data available
CHIP SELECT	TTL	168	Enable chip to accept programming
RESET	TTL	169	Disable all outputs (Hi-Z)
VDD	Power Supply	170	Most Positive Control Logic Supply
VCC	Power Supply	171	Most Positive PECL Supply (Common with other points labeled VCC)
VEE	Power Supply	172	Most Negative PECL Supply (Common with other points labeled VEE)
IN16P	PECL	173	High speed input
IN16N	PECL	174	High speed input compliment
VEE	Power Supply	175	Most Negative PECL Supply (Common with other points labeled VEE)
IN17P	PECL	176	High speed input
IN17N	PECL	177	High speed input compliment
VEE	Power Supply	178	Most Negative PECL Supply (Common with other points labeled VEE)
IN18P	PECL	179	High speed input
IN18N	PECL	180	High speed input compliment
VEE	Power Supply	181	Most Negative PECL Supply (Common with other points labeled VEE)
IN19P	PECL	182	High speed input
IN19N	PECL	183	High speed input compliment
VEE	Power Supply	184	Most Negative PECL Supply (Common with other points labeled VEE)

AD8151



Dim	Min.	Nom.	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
e		0.40 BSC	
D		22.00 BSC	
D1		20.00 BSC	
E		22.00 BSC	
E1		20.00 BSC	
ccc		0.08	
ddd		0.08	
aaa		0.20	
bbb		0.20	
θ	0°	3.5°	7°
θ1	0°		
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09		0.20
R1	0.08		
R2	0.08		0.20
S	0.20		
L	0.45	0.60	0.75
L1		1.00 REF	

NOTES:

1.Controlling Dimensions are in Millimeters(mm)